Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	49
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p54l3beaby

Contents

1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the SPC56xP54x/SPC56xP60x series of microcontroller units (MCUs). It also describes the device features and highlights important electrical and physical characteristics. For functional characteristics, refer to the device reference manual.

1.2 Description

This 32-bit system-on-chip (SoC) automotive microcontroller family is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address chassis applications specifically the airbag application.

This family is one of a series of next-generation integrated automotive microcontrollers based on the Power Architecture technology.

The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category. It operates up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

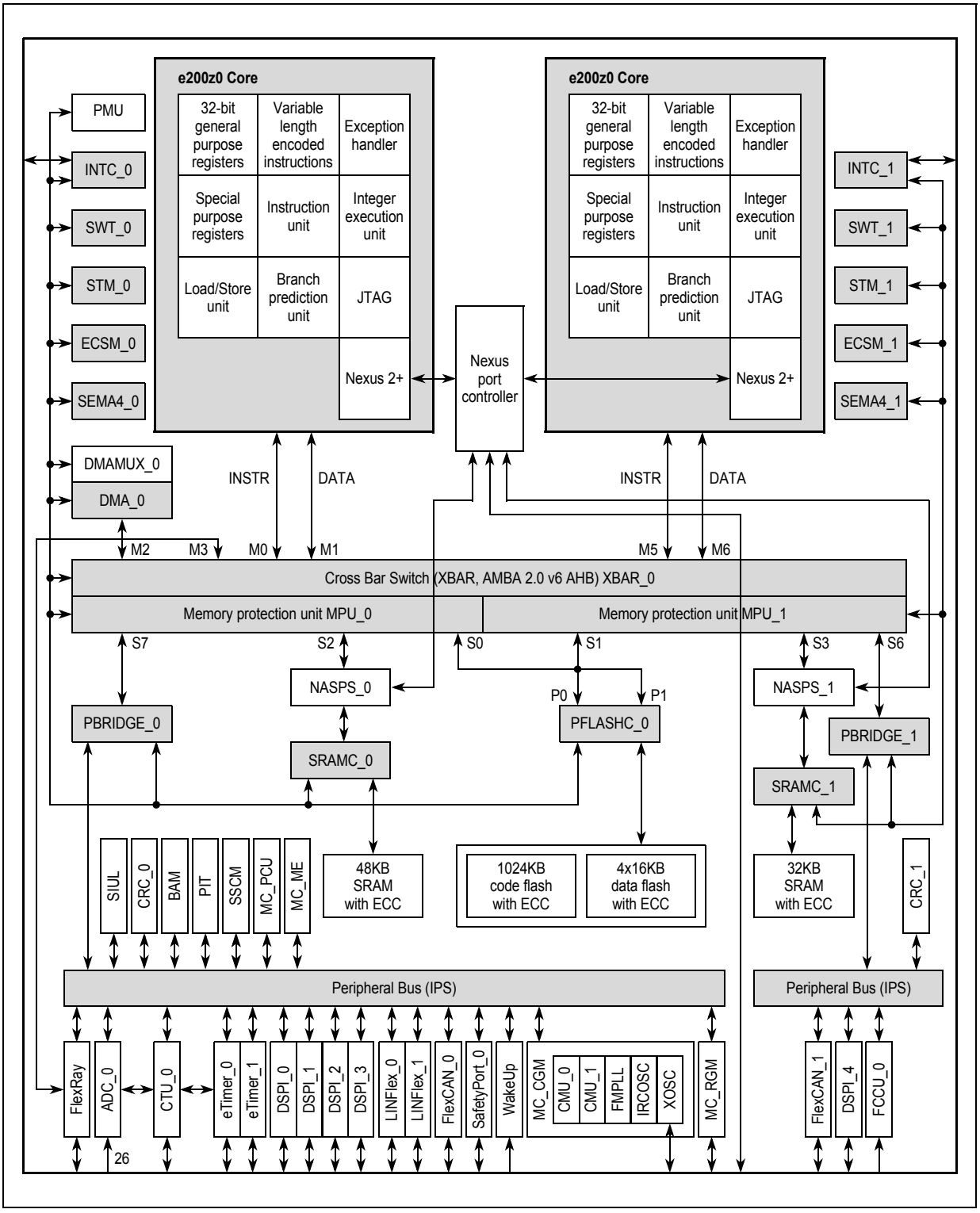
1.3 Device comparison

Table 2 provides a summary of different members of the SPC56xP54x/SPC56xP60x family and their features—relative to Full-featured version—to enable a comparison among the family members and an understanding of the range of functionality offered within this family.

Table 2. SPC56xP54x/SPC56xP60x device comparison

Feature	SPC560P54	SPC560P60	SPC56AP54	SPC56AP60
Code Flash memory (with ECC)	768 KB	1 MB	768 KB	1 MB
Data Flash / EE (with ECC)	64 KB			
SRAM (with ECC)	64 KB	80 KB	64 KB	80 KB
Processor core	32-bit e200z0h		32-bit Dual e200z0h	
Instruction set	VLE			
CPU performance	0-64 MHz			
FMPLL (frequency-modulated phase-locked loop) modules	1			
INTC (interrupt controller) channels	148			
PIT (periodic interrupt timer)	1 (includes four 32-bit timers)			

Figure 1. SPC56xP54x/SPC56xP60x block diagram



1.5.13 Software watchdog timer (SWT)

The SWT has the following features:

- Fault tolerant output
- Safe internal RC oscillator as reference clock
- Windowed watchdog
- Program flow control monitor with 16-bit pseudorandom key generation

The SWT module is replicated for each processor.

1.5.14 Fault collection and control unit (FCCU)

The FCCU provides an independent fault reporting mechanism even if the CPU is exhibiting unstable behaviors. The FCCU module has the following features:

- Redundant collection of hardware checker results
- Redundant collection of error information and latch of faults from critical modules on the device
- Collection of self-test results
- Configurable and graded fault control
  - Internal reactions (no internal reaction, IRQ)
  - External reaction (failure is reported to the external/surrounding system via configurable output pins)

1.5.15 System integration unit (SIUL)

The SPC56xP54x/SPC56xP60x SIUL controls MCU pad configuration, external interrupts, general purpose I/O (GPIO) pin configuration, and internal peripheral multiplexing.

The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU.

The SIUL provides the following features:

- Centralized general purpose input output (GPIO) control of input/output pins and analog input-only pads (package dependent)
- All GPIO pins can be independently configured to support pull-up, pull down, or no pull
- Reading and writing to GPIO supported both as individual pins and 16-bit wide ports
- All peripheral pins (except ADC channels) can be alternatively configured as both general purpose input or output pins
- ADC channels support alternative configuration as general purpose inputs
- Direct readback of the pin value is supported on all pins through the SIU
- Configurable digital input filter that can be applied to some general purpose input pins for noise elimination
  - Up to 4 internal functions can be multiplexed onto one pin

1.5.16 Boot and censorship

Different booting modes are available in the SPC56xP54x/SPC56xP60x:

- From internal flash memory
- Via a serial link

1.5.24 Analog-to-digital converter (ADC)

The ADC module provides the following features:

Analog part:

- 1 on-chip analog-to-digital converter
- 10-bit AD resolution
- 1 sample and hold unit per ADC
- Conversion time, including sampling time, less than 1 μs (at full precision)
- Typical sampling time is 150 ns min. (at full precision)
- Differential non-linearity error (DNL) ±1 LSB
- Integral non-linearity error (INL) ±1.5 LSB
- Total unadjusted error (TUE) <3 LSB
- Single-ended input signal range from 0 to 3.3 V / 5.0 V
- ADC and its reference can be supplied with a voltage independent from V_{DDIO}
- ADC supply can be equal or higher than V_{DDIO}
- ADC supply and the ADC reference are not independent from each other (they are internally bonded to the same pad)
- Sample times of 2 (default), 8, 64, or 128 ADC clock cycles

Digital part:

- 27 input channels (26 + 1 internally connected)
- 4 analog watchdogs to compare ADC results against predefined levels (low, high, range) before results are stored
- 2 operating modes: Normal mode and CTU control mode
- Normal mode features
  - Register-based interface with the CPU: control register, status register, 1 result register per channel
  - ADC state machine managing 3 request flows: regular command, hardware injected command, and software injected command
  - Selectable priority between software and hardware injected commands
  - DMA compatible interface
- CTU control mode features
  - Triggered mode only
  - 4 independent result queues (2 × 16 entries, 2 × 4 entries)
  - Result alignment circuitry (left justified; right justified)
  - 32-bit read mode allows to have channel ID on one of the 16-bit part
  - DMA compatible interfaces

1.5.25 Cross triggering unit (CTU)

The Cross Triggering Unit (CTU) allows automatic generation of ADC conversion requests on user selected conditions with minimized CPU load for dynamic configuration.

Table 5. Supply pins (continued)

Supply		Pin		
Symbol	**Description**	**LQFP 100**	**LQFP 144**	**LQFP 176(1)**
$V_{DD\_HV\_REG}$ (3.3 V or 5.0 V)	Voltage regulator supply voltage	50	72	86
$V_{DD\_LV\_REGCOR}$	1.2 V decoupling(2) pins for core logic supply and voltage regulator feedback. Decoupling capacitor must be connected between this pins and $V_{SS\_LV\_REGCOR}$.	48	70	82
$V_{SS\_LV\_REGCOR}$	1.2 V decoupling(2) pins for core logic GND and voltage regulator feedback. Decoupling capacitor must be connected between this pins and $V_{DD\_LV\_REGCOR}$.	49	71	85
ADC0 reference and supply voltage				
$V_{DD\_HV\_AD}$	ADC supply and high reference voltage	39	56	64
$V_{SS\_HV\_AD}$	ADC ground and low reference voltage	40	57	65
Power supply pins (3.3 V or 5.0 V)				
$V_{DD\_HV\_IO0}$	Input/Output supply voltage	—	6	14
$V_{SS\_HV\_IO0}$	Input/Output ground	—	7	15
$V_{DD\_HV\_IO1}$	Input/Output supply voltage	13	21	29
$V_{SS\_HV\_IO1}$	Input/Output ground	14	22	30
$V_{DD\_HV\_IO2}$	Input/Output supply voltage	63	91	115
$V_{SS\_HV\_IO2}$	Input/Output ground	62	90	114
$V_{DD\_HV\_IO3}$	Input/Output supply voltage	87	126	150
$V_{SS\_HV\_IO3}$	Input/Output ground	88	127	151
$V_{DD\_HV\_IO4}$	Input/Output supply voltage	—	—	169
$V_{SS\_HV\_IO4}$	Input/Output ground	—	—	170
$V_{DD\_HV\_IO5}$	Input/Output supply voltage	—	—	5
$V_{SS\_HV\_IO5}$	Input/Output ground	—	—	6
$V_{DD\_HV\_IO6}$	Input/Output supply voltage	—	—	108
$V_{SS\_HV\_IO6}$	Input/Output ground	—	—	109
$V_{DD\_HV\_FL}$	Code and data flash supply voltage	69	97	121
$V_{SS\_HV\_FL}$	Code and data flash supply ground	68	96	120
$V_{DD\_HV\_OSC}$	Crystal oscillator amplifier supply voltage	16	27	35
$V_{SS\_HV\_OSC}$	Crystal oscillator amplifier ground	17	28	36
Power supply pins (1.2 V)				
$V_{DD\_LV\_COR0}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR0}$ pin.	12	18	26

2. LQFP176 available only as development package.
3. In this pin there is an internal pull; refer to JTAGC chapter in the device reference manual for pull direction.
4. Its configuration can be set up by the PCR[108] register inside the SIU module. See SIUL chapter in the device reference manual.

2.2.3 Pin muxing

Table 7 defines the pin list and muxing for the SPC56xP54x/SPC56xP60x devices relative to Full-featured version.

Each row of *Table 7* shows all the possible ways of configuring each pin, via “alternate functions”. The default function assigned to each pin after reset is the ALT0 function.

Pins marked as external interrupt capable can also be used to resume from STOP and HALT mode.

SPC56xP54x/SPC56xP60x devices provide four main I/O pad types depending on the associated functions:

- *Slow pads* are the most common, providing a compromise between transition time and low electromagnetic emission.
- *Medium pads* provide fast enough transition for serial communication channels with controlled current to reduce electromagnetic emission.
- *Fast pads* provide maximum speed. They are used for improved NEXUS debugging capability.
- *Symmetric pads* are designed to meet FlexRay requirements.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance.

Table 7. Pin muxing(1)

Port pin	PCR No.	Alternate function(2), (3)	Functions	Peripheral (4)	I/O direction (5)	Pad speed(6)		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176(7)
Port A										
A[0]	PCR[0]	ALT0 ALT1 ALT2 ALT3 —	GPIO[0] ETC[0] SCK_2 F[0] EIRQ[0]	SIUL eTimer_0 DSPI_2 FCCU SIUL	I/O I/O I/O O I	Slow	Medium	51	73	89
A[1]	PCR[1]	ALT0 ALT1 ALT2 ALT3 —	GPIO[1] ETC[1] SOUT_2 F[1] EIRQ[1]	SIUL eTimer_0 DSPI_2 FCCU SIUL	I/O I/O O O I	Slow	Medium	52	74	90

Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
Port B										
B[0]	PCR[16]	ALT0 ALT1 ALT2 ALT3 —	GPIO[16] TXD ETC[2] DEBUG[0] EIRQ[15]	SIUL FlexCAN_0 eTimer_1 SSCM SIUL	I/O O I/O — I	Slow	Medium	76	109	133
B[1]	PCR[17]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[17] CS7_1 ETC[3] DEBUG[1] RXD EIRQ[16]	SIUL DSPI_1 eTimer_1 SSCM FlexCAN_0 SIUL	I/O O I/O — I I	Slow	Medium	77	110	134
B[2]	PCR[18]	ALT0 ALT1 ALT2 ALT3 —	GPIO[18] TXD SOUT_4 DEBUG[2] EIRQ[17]	SIUL LINFlex_0 DSPI_4 SSCM SIUL	I/O O I/O — I	Slow	Medium	79	114	138
B[3]	PCR[19]	ALT0 ALT1 ALT2 ALT3 —	GPIO[19] — SCK_4 DEBUG[3] RXD	SIUL — DSPI_4 SSCM LINFlex_0	I/O — I/O — I	Slow	Medium	80	116	140
B[6]	PCR[22]	ALT0 ALT1 ALT2 ALT3 —	GPIO[22] clk_out CS2_2 clk_out_div256 EIRQ[18]	SIUL MC_CGL DSPI_2 MC_CGL SIUL	I/O O O O I	Slow	Medium	96	138	162
B[7]	PCR[23]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[23] — — — AN[0] RXD	SIUL — — — ADC_0 LINFlex_0	Input Only	—	—	29	43	51
B[8]	PCR[24]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[24] — — — AN[1] ETC[5]	SIUL — — — ADC_0 eTimer_0	Input Only	—	—	31	47	55

Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
D[7]	PCR[55]	ALT0 ALT1 ALT2 ALT3 —	GPIO[55] CS3_1 — CS4_0 SIN_3	SIUL DSPI_1 — DSPI_0 DSPI_3	I/O O — O I	Slow	Medium	26	37	45
D[8]	PCR[56]	ALT0 ALT1 ALT2 ALT3	GPIO[56] CS2_1 RDY CS5_0	SIUL DSPI_1 nexus_0 DSPI_0	I/O O O O	Slow	Medium	21	32	40
D[9]	PCR[57]	ALT0 ALT1 ALT2 ALT3	GPIO[57] — TXD CS6_1	SIUL — LINFlex_1 DSPI_1	I/O — O O	Slow	Medium	15	26	34
D[10]	PCR[58]	ALT0 ALT1 ALT2 ALT3	GPIO[58] — CS0_3 —	SIUL — DSPI_3 —	I/O — I/O —	Slow	Medium	53	76	92
D[11]	PCR[59]	ALT0 ALT1 ALT2 ALT3	GPIO[59] — CS1_3 SCK_3	SIUL — DSPI_3 DSPI_3	I/O — O I/O	Slow	Medium	54	78	94
D[12]	PCR[60]	ALT0 ALT1 ALT2 ALT3 —	GPIO[60] — — CS7_1 RXD	SIUL — — DSPI_1 LINFlex_1	I/O — — O I	Slow	Medium	70	99	123
D[13]	PCR[61]	ALT0 ALT1 ALT2 ALT3	GPIO[61] — CS2_3 SOUT_3	SIUL — DSPI_3 DSPI_3	I/O — O O	Slow	Medium	67	95	119
D[14]	PCR[62]	ALT0 ALT1 ALT2 ALT3 —	GPIO[62] — CS3_3 — SIN_3	SIUL — DSPI_3 — DSPI_3	I/O — O — I	Slow	Medium	73	105	129
D[15]	PCR[63]	ALT0 ALT1 ALT2 ALT3 —	GPIO[63] — — — AN[20]	SIUL — — — ADC_0	Input Only	—	—	41	58	66

Table 7. Pin muxing[1] (continued)

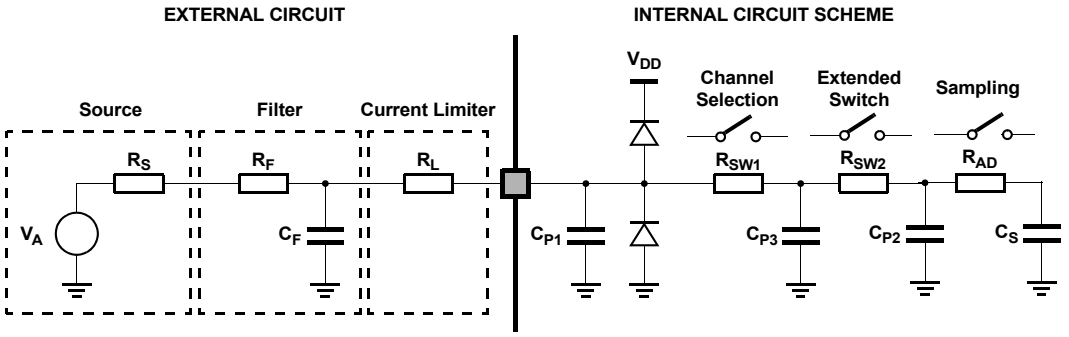
Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
Port G										
G[0]	PCR[96]	ALT0 ALT1 ALT2 ALT3 —	GPIO[96] F[0] — — EIRQ[30]	SIUL FCCU — — SIUL	I/O O — — I	Slow	Medium	—	38	46
G[1]	PCR[97]	ALT0 ALT1 ALT2 ALT3 —	GPIO[97] F[1] — — EIRQ[31]	SIUL FCCU — — SIUL	I/O O — — I	Slow	Medium	—	141	173
G[2]	PCR[98]	ALT0 ALT1 ALT2 ALT3 —	GPIO[98] — — — SIN_4	SIUL — — — DSPI_4	I/O — — — I	Slow	Medium	—	102	126
G[3]	PCR[99]	ALT0 ALT1 ALT2 ALT3	GPIO[99] — SOUT_4 —	SIUL — DSPI_4 —	I/O — O —	Slow	Medium	—	104	128
G[4]	PCR[100]	ALT0 ALT1 ALT2 ALT3	GPIO[100] — SCK_4 —	SIUL — DSPI_4 —	I/O — I/O —	Slow	Medium	—	100	124
G[5]	PCR[101]	ALT0 ALT1 ALT2 ALT3	GPIO[101] — CS0_4 —	SIUL — DSPI_4 —	I/O — I/O —	Slow	Medium	—	85	103
G[6]	PCR[102]	ALT0 ALT1 ALT2 ALT3	GPIO[102] — CS1_4 —	SIUL — DSPI_4 —	I/O — O —	Slow	Medium	—	98	122
G[7]	PCR[103]	ALT0 ALT1 ALT2 ALT3	GPIO[103] — CS2_4 —	SIUL — DSPI_4 —	I/O — O —	Slow	Medium	—	83	101

Table 24. Peripherals supply current (5 V and 3.3 V)(1)

Symbol		Parameter	Conditions		Value		Unit
					Typ	Max	
$I_{DD\_HV(CAN)}$	T	CAN (FlexCAN) supply current on VDD_HV_REG	500 Kbyte/s	Total (static + dynamic) consumption: – FlexCAN in loop-back mode – XTAL@ 8 MHz used as CAN engine clock source – Message sending period is 580 µs	21.6 * f_{periph}	28.1* f_{periph}	µA
$I_{DD\_HV(SCI)}$	T	SCI (LINFlex) supply current on VDD_HV_REG	Total (static + dynamic) consumption: – LIN mode – Baudrate: 115.2 Kbyte/s		10.8 * f_{periph}	14.1 * f_{periph}	
$I_{DD\_HV(SPI)}$	T	SPI (DSPI) supply current on VDD_HV_REG	Ballast dynamic consumption (continuous communication): – Baudrate: 2 Mbit/s – Transmission every 8 µs – Frame: 16 bits		4.8 * f_{periph}	6.3 * f_{periph}	
$I_{DD\_HV(ADC)}$	T	ADC supply current on VDD_HV_REG	VDD = 5.5 V	Ballast dynamic consumption (continuous conversion)	120 * f_{periph}	156 * f_{periph}	
$I_{DD\_HV\_ADC(ADC)}$	T	ADC supply current on VDD_HV_ADC	VDD = 5.5 V	Analog dynamic consumption (continuous conversion)	0.005 * f_{periph} + 2.8	0.007 * f_{periph} + 3.4	mA
$I_{DD\_HV(eTimer)}$	T	eTimer supply current on VDD_HV_REG	PWM signals generation on all 1 channel @10kHz	Dynamic consumption does not change varying the frequency	1.8	2.4	mA
$I_{DD\_HV(FlexRay)}$	T	FlexRay supply current on VDD_HV_REG	Static consumption		4.2 * f_{periph}	5.5 * f_{periph}	µA

1. Operating conditions: f_{periph} = 8 MHz to 64 MHz

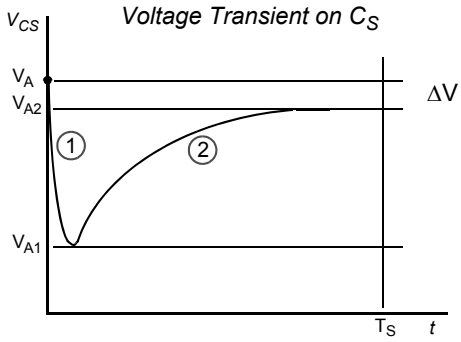
Figure 17. Input equivalent circuit (extended channels)



R_S: Source impedance
R_F: Filter resistance
C_F: Filter capacitance
R_L: Current limiter resistance
R_{SW1}: Channel selection switch impedance (two contributions, R_{SW1} and R_{SW2})
R_{AD}: Sampling switch impedance
C_P: Pin capacitance (two contributions, C_{P1}, C_{P2} and C_{P3})
C_S: Sampling capacitance

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in *Figure 16*): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

Figure 18. Transient behavior during sampling phase



$\Delta V < 0.5$ LSB

$\tau_1 < (R_{SW} + R_{AD})\, C_S << T_S$

$\tau_2 = R_L\,(C_S + C_{P1} + C_{P2})$

3.15.2 ADC conversion characteristics

Table 32. ADC conversion characteristics

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
V_{INAN}	SR	Analog input voltage[2]	—	$V_{SS\_HV\_AD}$ – 0.3	—	$V_{SS\_HV\_AD}$ + 0.3	V
f_{CK}	SR	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_clk[3] frequency)	—	3[4]	—	60	MHz
f_s	SR	Sampling frequency	—	—	—	1.53	MHz
t_{ADC_S}	D	Sample time[5]	f_{ADC} = 20 MHz, INPSAMP = 3	125	—	—	ns
			f_{ADC} = 9 MHz, INPSAMP = 255	—	—	28.2	µs
t_{ADC_C}	P	Conversion time[6]	f_{ADC} = 20 MHz[7], INPCMP = 1	0.650	—	—	µs
C_S[8]	D	ADC input sampling capacitance	—	—	—	2.5	pF
C_{P1}[8]	D	ADC input pin capacitance 1	—	—	—	3	pF
C_{P2}[8]	D	ADC input pin capacitance 2	—	—	—	1	pF
C_{P3}[8]	D	ADC input pin capacitance 3	—	—	—	1	pF
R_{SW1}[8]	D	Internal resistance of analog source	$V_{DD\_HV\_AD}$ = 5 V ±10%	—	—	0.6	kΩ
			$V_{DD\_HV\_AD}$ = 3.3 V ±10%	—	—	3	kΩ
R_{SW2}[8]	D	Internal resistance of analog source	$V_{DD\_HV\_AD}$ = 5 V ±10%	—	—	2.15	kΩ
			$V_{DD\_HV\_AD}$ = 3.3 V ±10%	—	—	3.6	kΩ
R_{AD}[8]	D	Internal resistance of analog source	—	—	—	2	kΩ
I_{INJ}	T	Input current injection	Current injection on one ADC input, different from the converted one. Remains within TUE spec.	–5	—	5	mA
INL	P	Integral Non Linearity	No overload	—	±1.5	—	LSB
DNL	P	Differential Non Linearity	No overload	–1.0	—	1.0	LSB
OFS	T	Offset error	—	—	±1	—	LSB
GNE	T	Gain error	—	—	±1	—	LSB
TUE	P	Total unadjusted error without current injection	16 precision channels	–2.5	—	2.5	LSB

3. The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
4. Actual hardware programming times. This does not include software overhead.
5. Typical bank programming time assumes that all cells are programmed in a single pulse. In reality some cells will require more than one pulse, adding a small overhead to total bank programming time (see Initial Max column).
6. Time between erase suspend resume and next erase suspend.

Table 34. Flash memory module life

Symbol		Parameter	Conditions	Value		Unit
				Min	Typ	
P/E	C	Number of program/erase cycles per block for 16 KB blocks over the operating temperature range (T_J)	—	100000	100000	cycles
P/E	C	Number of program/erase cycles per block for 32 KB blocks over the operating temperature range (T_J)	—	10000	100000	cycles
P/E	C	Number of program/erase cycles per block for 64 KB blocks over the operating temperature range (T_J)	—	10000	100000	cycles
P/E	C	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	—	1000	100000	cycles
Retention	C	Minimum data retention at 85 °C average ambient temperature(1)	Blocks with 0 – 1000 P/E cycles	20	—	years
			Blocks with 10000 P/E cycles	10	—	years
			Blocks with 100000 P/E cycles	5	—	years

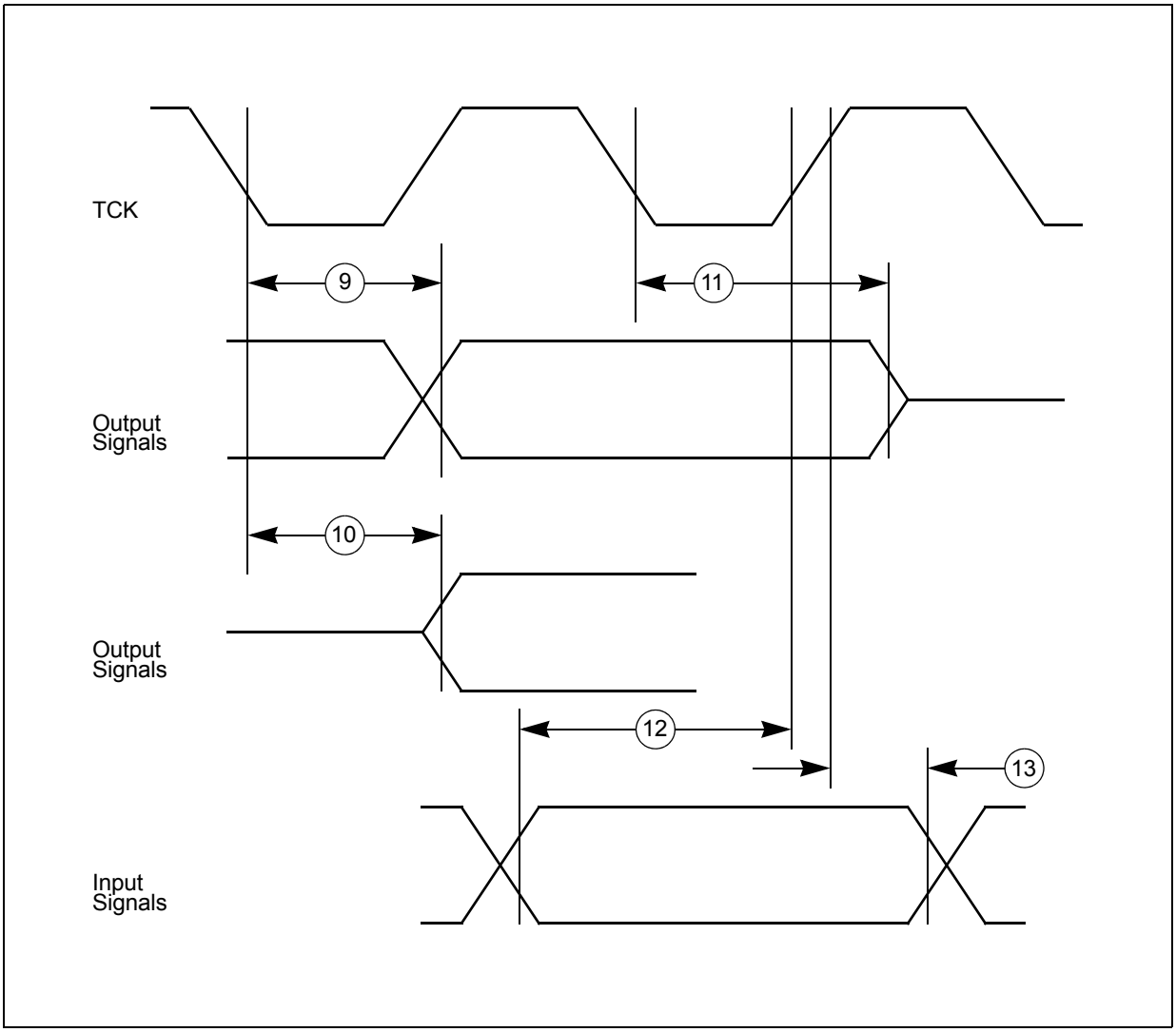
1. Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

Table 35. Flash read access timing

Symbol	C	Parameter	Conditions(1)	Max	Unit
Fmax	C	Maximum working frequency for Code Flash at given number of WS in worst conditions	2 wait states	66	MHz
			0 wait states	22	
Fmax	C	Maximum working frequency for Data Flash at given number of WS in worst conditions	8 wait states	66	MHz

1. VDD = 3.3 V ± 10% / 5.0 V ± 10%, TA = –40 to 125 °C, unless otherwise specified.

Figure 24. JTAG boundary scan timing



3.18.3 Nexus timing

Table 39. Nexus debug port timing(1)

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{MCYC}	CC	D	MCKO cycle time	32	—	—	ns
2	t_{MDOV}	CC	D	MCKO edge to MDO data valid	–0.1 × t_{MCYC}	—	0.25 × t_{MCYC}	ns
3	t_{MSEOV}	CC	D	MCKO edge to $\overline{\text{MSEO}}$ data valid	–0.1 × t_{MCYC}	—	0.25 × t_{MCYC}	ns
4	t_{EVTOV}	CC	D	MCKO edge to $\overline{\text{EVTO}}$ data valid	–0.1 × t_{MCYC}	—	0.25 × t_{MCYC}	ns
5	t_{TCYC}	CC	D	TCK cycle time	64(2)	—	—	ns

4.2.2 LQFP100 mechanical outline drawing

Figure 39. LQFP100 package mechanical drawing

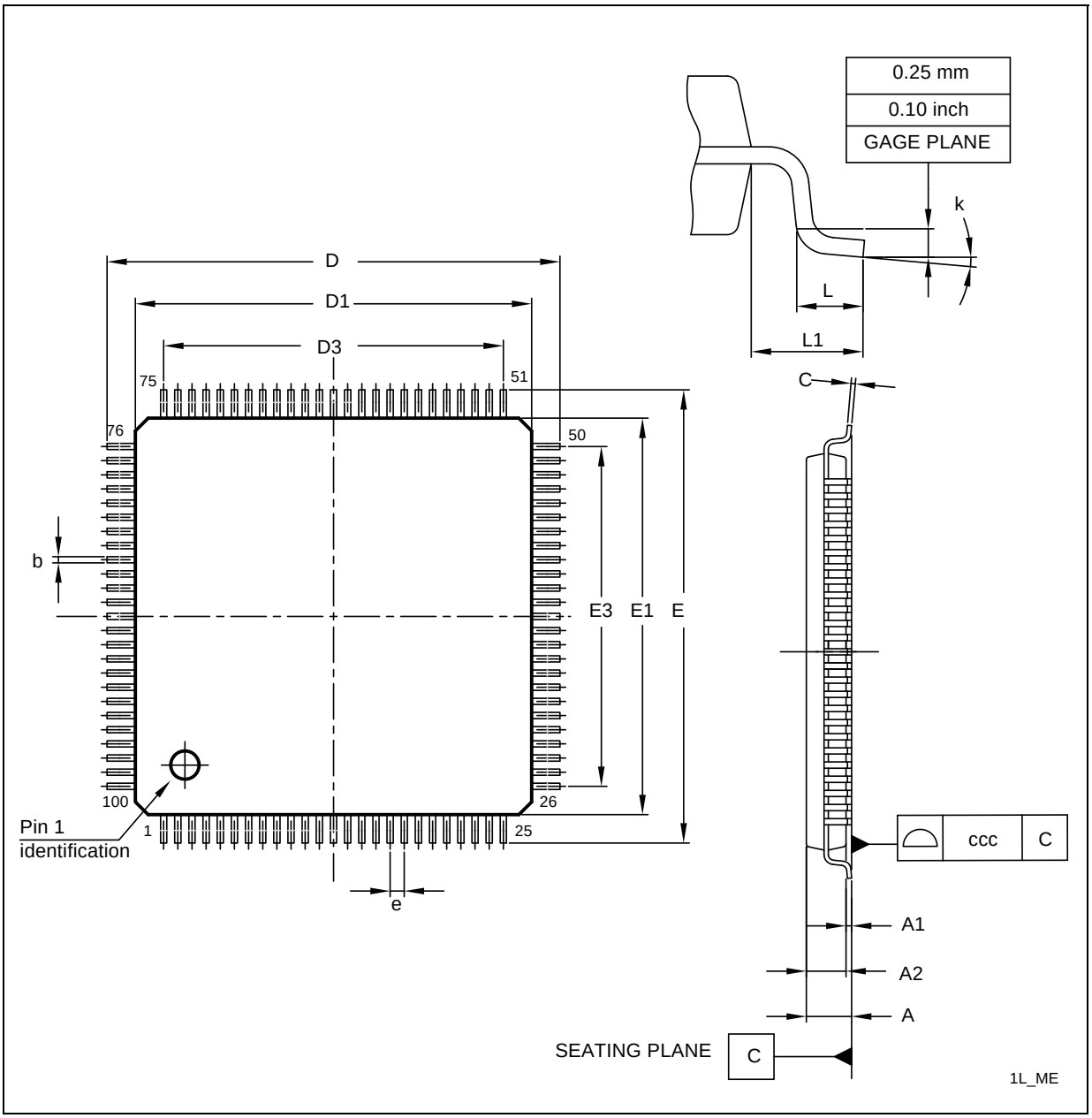


Table 43. LQFP100 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571

Table 43. LQFP100 mechanical data (continued)

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	—	12.000	—	—	0.4724	—
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	—	12.000	—	—	0.4724	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0 °	0.0 °	3.5 °	7.0 °
ccc[2]	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Tolerance.

Table 44. Document revision history (continued)

Date	Revision	Substantive changes
15-May-2012	3	Removed “Enhanced Full-featured” version. In the cover page, added “(1 × Master/Slave, 1 × Master Only)“ at the end of the bullet “2 LINFlex modules (LIN 2.1)” *Table 2: SPC56xP54x/SPC56xP60x device comparison*, updated the value of “LINFLEX module” to “2 (1 × Master/Slave, 1 × Master only)” *Section 1.5.4: On-chip flash memory with ECC* replaced two occurrences of “3 wait states” to “2 wait states” replaced 60 MHz to 64 MHz *Section 1.5.21: Serial communication interface module (LINFlex)*, updated first bullet to “Supports LIN Master mode (on both modules), LIN Slave mode (on one module) and UART mode” *Section 1.5.24: Analog-to-digital converter (ADC)*, removed bullet concerning the analog watchdogs from Normal mode features. *Table 5: Supply pins*, removed V_{REG_BYPASS} row. *Table 6: System pins*: added V_{REG_BYPASS} row added a footnote about $\overline{RESET}$ *Table 9: Absolute maximum ratings*: changed typical value of TV_{DD} to 0.25 and added a footnote added V_{INAN} entry Updated *Section 3.8.1: Voltage regulator electrical characteristics* Updated *Table 14: EMI testing specifications* *Table 18: Low voltage monitor electrical characteristics*, changed maximum value of $V_{MLVDDOK\_H}$ to 1.15 *Table 20: DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V]=0)*, added IPU and IPD rows for $\overline{RESET}$ pin. *Table 21: Supply current (5.0 V, NVUSRO[PAD3V5V]=0)*: added maximum values of $I_{DD\_LV\_CORE}$ for: RUN, HALT, and STOP mode updated values and parameter classification of I_{DD_FLASH} *Table 22: DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V]=1)*, added IPU and IPD rows for $\overline{RESET}$ pin. *Table 23: Supply current (3.3 V, NVUSRO[PAD3V5V]=1)*: added maximum values of $I_{DD\_LV\_CORE}$ for: RUN, HALT, and STOP mode updated values and parameter classification of I_{DD_FLASH} Added *Table 26: I/O consumption* *Table 31: 16 MHz RC oscillator electrical characteristics*, changed minimum and maximum values of Δ_{RCMVAR} respectively to -6 and 6. Renamed *Figure 16: Input equivalent circuit (precise channels)* (was “Input equivalent circuit”) Added *Figure 17: Input equivalent circuit (extended channels)* *Section 3.15.1: Input impedance and ADC accuracy*, updated *Equation 4* and *Equation 10* *Table 32: ADC conversion characteristics*, added V_{INAN}, C_{P3} and R_{SW2} rows

Table 44. Document revision history (continued)

Date	Revision	Substantive changes
21-Nov-2012	4	In the cover page, replaced “64 MHz, dual issue, 32-bit CPU core complex” with “64 MHz, single issue, 32-bit CPU core complex” *Table 9: Absolute maximum ratings*, updated TV_{DD} entry *Table 22: DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V]=1)*: Updated conditions value of V_{OL_F} to 11 mA Updated conditions value of V_{OH_F} to – 11 mA *Table 24: Peripherals supply current (5 V and 3.3 V)*: Replaced all occurrences of I_{DD_BV} in this table with I_{DD_HV} Replaced all occurrences of VDD_BV in this table with VDD_HV_REG. *Figure 40: Ordering information scheme*, fixed typo in the footnote.
18-Sep-2013	5	Updated Disclaimer.
15-Jun-2016	6	Added “AEC-Q10x qualified” in *Features* section. In *Table 2: SPC56xP54x/SPC56xP60x device comparison* added footnote “LinFlex_1 is Master Only.” related to row “LINFlex modules” Updated *Table 3: SPC56xP54x/SPC56xP60x device configuration difference* *Figure 2: LQFP176 pinout (top view)*: – Changed PB[4] to TDO – Changed PB[5] to TDI – Changed pins 71,72 to NC – Changed pins 87,88 to NC In *Section 1.5.27: Nexus development interface (NDI)*, added note “At least one TCK clock is necessary for the EVTI signal to be recognized by the MCU.” for EVTI pin. In *Table 7: Pin muxing*: – Replaced “PCR register” with “PCR No.” – Updated “CS3” with “CS3_4” function related to A[2] port pin – In column “I/O direction”, added “O” for “DSPI_1” peripheral – In “Functions” column related to D[12] port pin, changed DS7_1 to CS7_1