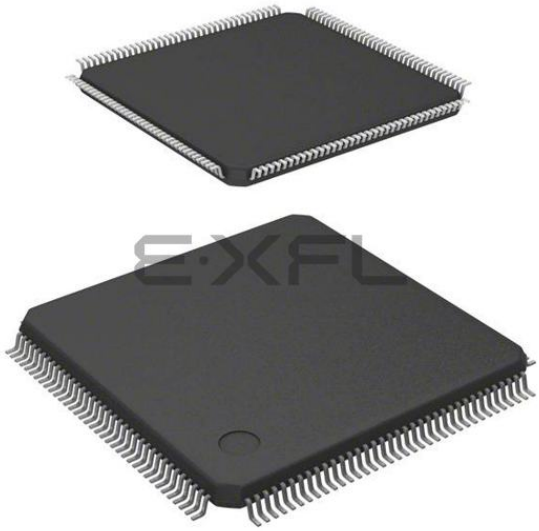

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 26x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p54l5beabr

1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the SPC56xP54x/SPC56xP60x series of microcontroller units (MCUs). It also describes the device features and highlights important electrical and physical characteristics. For functional characteristics, refer to the device reference manual.

1.2 Description

This 32-bit system-on-chip (SoC) automotive microcontroller family is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address chassis applications specifically the airbag application.

This family is one of a series of next-generation integrated automotive microcontrollers based on the Power Architecture technology.

The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category. It operates up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

1.3 Device comparison

Table 2 provides a summary of different members of the SPC56xP54x/SPC56xP60x family and their features—relative to Full-featured version—to enable a comparison among the family members and an understanding of the range of functionality offered within this family.

Table 2. SPC56xP54x/SPC56xP60x device comparison

Feature	SPC560P54	SPC560P60	SPC56AP54	SPC56AP60
Code Flash memory (with ECC)	768 KB	1 MB	768 KB	1 MB
Data Flash / EE (with ECC)	64 KB			
SRAM (with ECC)	64 KB	80 KB	64 KB	80 KB
Processor core	32-bit e200z0h		32-bit Dual e200z0h	
Instruction set	VLE			
CPU performance	0-64 MHz			
FMPLL (frequency-modulated phase-locked loop) modules	1			
INTC (interrupt controller) channels	148			
PIT (periodic interrupt timer)	1 (includes four 32-bit timers)			

Table 2. SPC56xP54x/SPC56xP60x device comparison (continued)

Feature		SPC560P54	SPC560P60	SPC56AP54	SPC56AP60
Enhanced DMA (direct memory access) channels		16			
FlexRay		Yes (64 message buffer)			
FlexCAN (controller area network)		3(1),(2)			
Safety port		Yes (via third FlexCAN module)			
FCCU (fault collection and control unit)		Yes(3)			
CTU (cross triggering unit)		Yes			
eTimer channels		2 × 6			
FlexPWM (pulse-width modulation) channels		No			
Analog-to-digital converters (ADC)		One (10-bit, 27-channel)(4)			
LINFlex modules		2 (1 × Master/Slave, 1 × Master only)(5)			
DSPI (deserial serial peripheral interface) modules		5(6)			
CRC (cyclic redundancy check) units		2(7)			
JTAG interface		Yes			
Nexus port controller (NPC)		Yes (Level 2+)(8)			
Supply	Digital power supply(9)	3.3 V or 5 V single supply with external transistor			
	Analog power supply	3.3 V or 5 V			
	Internal RC oscillator	16 MHz			
	External crystal oscillator	4–40 MHz			
Packages		LQFP100 LQFP144			LQFP100 LQFP144 LQFP176(10)
Temperature	Standard ambient temperature	–40 to 125 °C			

1. Each FlexCAN module has 32 message buffers.
2. One FlexCAN module can act as a Safety Port with a bit rate as high as 7.5 Mbit/s.
3. Enhanced FCCU version.
4. Same amount of ADC channels as on SPC560P44/50 not considering the internally connected ones. 26 channels on LQFP144 and 16 channels on LQFP100.
5. LinFlex_1 is Master Only.
6. Increased number of CS for DSPI_1.
7. Upgraded specification with addition of 8-bits polynomial (CRC-8 VDA CAN) support and 3rd context.
8. Improved debugging capability with data trace capability and increased Nexus throughput available on emulation package.
9. 3.3 V range and 5 V range correspond to different orderable parts.
10. Software development package only. Not available for production.

- Triangle wave modulation
- Programmable modulation depth (±0.25% to ±4% deviation from center frequency)
  - Programmable modulation frequency dependent on reference frequency
- Self-clocked mode (SCM) operation

1.5.9 Main oscillator

The main oscillator provides these features:

- Input frequency range 4 MHz to 40 MHz
- Crystal input mode or Oscillator input mode
- PLL reference

1.5.10 Internal RC oscillator

This device has an RC ladder phase-shift oscillator. The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared by the stable bandgap reference voltage.

The RC Oscillator provides these features:

- Nominal frequency 16 MHz
- ±6% variation over voltage and temperature after process trim
- Clock output of the RC oscillator serves as system clock source in case loss of lock or loss of clock is detected by the PLL
- RC oscillator is used as the default system clock during startup

1.5.11 Periodic interrupt timer (PIT)

The PIT module implements these features:

- Up to four general purpose interrupt timers
- 32-bit counter resolution
- Clocked by system clock frequency
- Each channel can be used as trigger for a DMA request

1.5.12 System timer module (STM)

The STM module implements these features:

- 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

The STM module is replicated for each processor.

1.5.21 Serial communication interface module (LINFlex)

The LINFlex on the SPC56xP54x/SPC56xP60x features the following:

- Supports LIN Master mode (on both modules), LIN Slave mode (on one module) and UART mode
- LIN state machine compliant to LIN1.3, 2.0, and 2.1 Specifications
- Handles LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store Identifier and up to 8 data bytes
  - Supports message length as long as 64 bytes
  - Detection and flagging of LIN errors: Sync field; Delimiter; ID parity; Bit; Framing; Checksum and Time-out errors
  - Classic or extended checksum calculation
  - Configurable Break duration as long as 36-bit times
  - Programmable Baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features: Loop back; Self Test; LIN bus stuck dominant detection
  - Interrupt-driven operation with 16 interrupt sources
- LIN slave mode features
  - Autonomous LIN header handling
  - Autonomous LIN response handling
- UART mode
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit or 9-bit words)
  - Error detection and flagging
  - Parity, Noise and Framing errors
  - Interrupt-driven operation with four interrupt sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - 2 receiver wake-up methods

1.5.22 Deserial serial peripheral interface (DSPI)

The deserial serial peripheral interface (DSPI) module provides a synchronous serial interface for communication between the SPC56xP54x/SPC56xP60x MCU and external devices.

  - Watchpoint triggering, watchpoint triggers program tracing
  - DDR
- Auxiliary Output Port
  - 4 MDO (Message Data Out) pins
  - MCKO (Message Clock Out) pin
  - 2 $\overline{\text{MSEO}}$ (Message Start/End Out) pins
  - $\overline{\text{EVTO}}$ (Event Out) pin
- Auxiliary Input Port
  - $\overline{\text{EVTI}}$ (Event In) pin[a]

1.5.28 IEEE 1149.1 (JTAG) controller

The JTAG controller (JTAGC) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE standard.

The JTAG controller provides the following features:

- IEEE Test Access Port (TAP) interface with four pins (TDI, TMS, TCK, TDO)
- Selectable modes of operation include JTAGC/debug or normal system operation.
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD
- A 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC, ACCESS_AUX_TAP_CORE0, ACCESS_AUX_TAP_CORE1, ACCESS_AUX_TAP_NASPS_0, ACCESS_AUX_TAP_NASPS_1
- Three test data registers: a bypass register, a boundary scan register, and a device identification register.
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry.

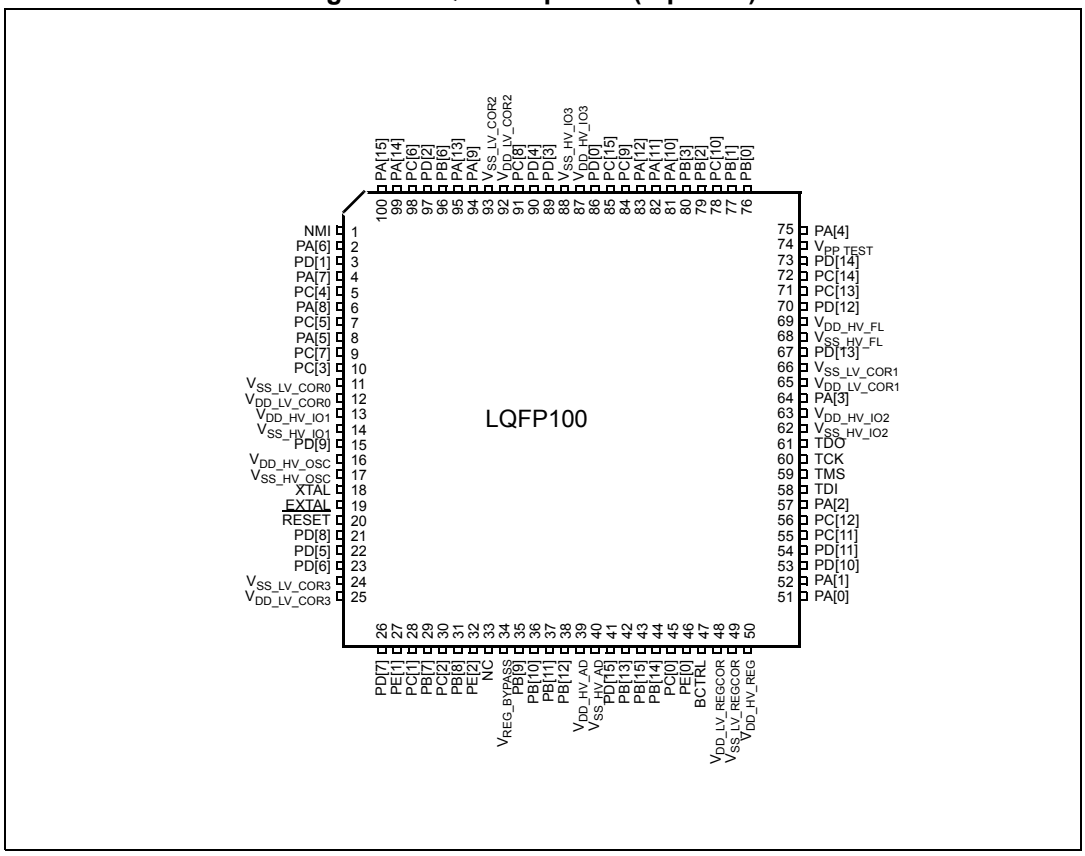
1.5.29 On-chip voltage regulator (VREG)

The on-chip voltage regulator module provides the following features:

- Uses external NPN transistor
- Regulates external 3.3 V to 5.0 V down to 1.2 V for the core logic
- Low voltage detection on the internal 1.2 V and I/O voltage 3.3 V

a. At least one TCK clock is necessary for the EVTI signal to be recognized by the MCU.

Figure 4. LQFP100 pinout (top view)[d]



2.2 Pin descriptions

The following sections provide signal descriptions and related information about the functionality and configuration of the SPC56xP54x/SPC56xP60x devices.

2.2.1 Power supply and reference voltage pins

Table 5 lists the power supply and reference voltage for the SPC56xP54x/SPC56xP60x devices.

Table 5. Supply pins

Supply		Pin		
Symbol	**Description**	**LQFP 100**	**LQFP 144**	**LQFP 176[1]**
VREG control and power supply pins				
BCTRL	Voltage regulator external NPN Ballast base control pin	47	69	81

d. Availability of port pin alternate functions depends on product selection.

Table 5. Supply pins (continued)

Supply		Pin		
Symbol	**Description**	**LQFP 100**	**LQFP 144**	**LQFP 176(1)**
$V_{DD\_HV\_REG}$ (3.3 V or 5.0 V)	Voltage regulator supply voltage	50	72	86
$V_{DD\_LV\_REGCOR}$	1.2 V decoupling(2) pins for core logic supply and voltage regulator feedback. Decoupling capacitor must be connected between this pins and $V_{SS\_LV\_REGCOR}$.	48	70	82
$V_{SS\_LV\_REGCOR}$	1.2 V decoupling(2) pins for core logic GND and voltage regulator feedback. Decoupling capacitor must be connected between this pins and $V_{DD\_LV\_REGCOR}$.	49	71	85
ADC0 reference and supply voltage				
$V_{DD\_HV\_AD}$	ADC supply and high reference voltage	39	56	64
$V_{SS\_HV\_AD}$	ADC ground and low reference voltage	40	57	65
Power supply pins (3.3 V or 5.0 V)				
$V_{DD\_HV\_IO0}$	Input/Output supply voltage	—	6	14
$V_{SS\_HV\_IO0}$	Input/Output ground	—	7	15
$V_{DD\_HV\_IO1}$	Input/Output supply voltage	13	21	29
$V_{SS\_HV\_IO1}$	Input/Output ground	14	22	30
$V_{DD\_HV\_IO2}$	Input/Output supply voltage	63	91	115
$V_{SS\_HV\_IO2}$	Input/Output ground	62	90	114
$V_{DD\_HV\_IO3}$	Input/Output supply voltage	87	126	150
$V_{SS\_HV\_IO3}$	Input/Output ground	88	127	151
$V_{DD\_HV\_IO4}$	Input/Output supply voltage	—	—	169
$V_{SS\_HV\_IO4}$	Input/Output ground	—	—	170
$V_{DD\_HV\_IO5}$	Input/Output supply voltage	—	—	5
$V_{SS\_HV\_IO5}$	Input/Output ground	—	—	6
$V_{DD\_HV\_IO6}$	Input/Output supply voltage	—	—	108
$V_{SS\_HV\_IO6}$	Input/Output ground	—	—	109
$V_{DD\_HV\_FL}$	Code and data flash supply voltage	69	97	121
$V_{SS\_HV\_FL}$	Code and data flash supply ground	68	96	120
$V_{DD\_HV\_OSC}$	Crystal oscillator amplifier supply voltage	16	27	35
$V_{SS\_HV\_OSC}$	Crystal oscillator amplifier ground	17	28	36
Power supply pins (1.2 V)				
$V_{DD\_LV\_COR0}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR0}$ pin.	12	18	26

Table 5. Supply pins (continued)

Supply		Pin		
Symbol	Description	LQFP 100	LQFP 144	LQFP 176[1]
$V_{SS\_LV\_COR0}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR0}$ pin.	11	17	25
$V_{DD\_LV\_COR1}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR1}$ pin.	65	93	117
$V_{SS\_LV\_COR1}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR1}$ pin.	66	94	118
$V_{DD\_LV\_COR2}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR2}$ pin.	92	131	155
$V_{SS\_LV\_COR2}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR\ 2}$ pin.	93	132	156
$V_{DD\_LV\_COR3}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR3}$ pin.	25	36	44
$V_{SS\_LV\_COR3}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR\ 3}$ pin.	24	35	43

1. LQFP176 available only as development package.
2. See datasheet Voltage Regulator Electrical Characteristics section for more details.

2.2.2 System pins

Table 6 and *Table 7* contain information on pin functions for the SPC56xP54x/SPC56xP60x devices. The pins listed in *Table 6* are single-function pins. The pins shown in *Table 7* are multi-function pins, programmable via their respective Pad Configuration Register (PCR) values.

Table 6. System pins

Symbol	Description	Direction	Pad Speed[1]		Pin		
			SRC=0	SRC=1	LQFP 100	LQFP 144	LQFP 176[2]
Dedicated pins							
MDO0	Nexus Message Data Output—line 0	Output Only	Fast		—	9	17
MDO4	Nexus Message Data Output—line 4	Output Only	Fast		—	—	7

Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
A[2] [8]	PCR[2]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[2] ETC[2] CS3_4 — SIN_2 ABS[0] EIRQ[2]	SIUL eTimer_0 DSPI_4 — DSPI_2 MC_RGM SIUL	I/O I/O O — I I I	Slow	Medium	57	84	102
A[3] [8]	PCR[3]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[3] ETC[3] CS0_2 — ABS[1] EIRQ[3]	SIUL eTimer_0 DSPI_2 — MC_RGM SIUL	I/O I/O I/O — I I	Slow	Medium	64	92	116
A[4] [8]	PCR[4]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[4] ETC[0] CS1_2 ETC[4] FAB EIRQ[4]	SIUL eTimer_1 DSPI_2 eTimer_0 MC_RGM SIUL	I/O I/O O I/O I I	Slow	Medium	75	108	132
A[5]	PCR[5]	ALT0 ALT1 ALT2 ALT3 —	GPIO[5] CS0_1 ETC[5] CS7_0 EIRQ[5]	SIUL DSPI_1 eTimer_1 DSPI_0 SIUL	I/O I/O I/O O I	Slow	Medium	8	14	22
A[6]	PCR[6]	ALT0 ALT1 ALT2 ALT3 —	GPIO[6] SCK_1 CS2_4 — EIRQ[6]	SIUL DSPI_1 DSPI_4 — SIUL	I/O I/O I/O — I	Slow	Medium	2	2	2
A[7]	PCR[7]	ALT0 ALT1 ALT2 ALT3 —	GPIO[7] SOUT_1 CS1_4 — EIRQ[7]	SIUL DSPI_1 DSPI_4 — SIUL	I/O O I/O — I	Slow	Medium	4	10	18
A[8]	PCR[8]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[8] — CS0_4 — SIN_1 EIRQ[8]	SIUL — DSPI_4 — DSPI_1 SIUL	I/O — I/O — I I	Slow	Medium	6	12	20

Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
Port B										
B[0]	PCR[16]	ALT0 ALT1 ALT2 ALT3 —	GPIO[16] TXD ETC[2] DEBUG[0] EIRQ[15]	SIUL FlexCAN_0 eTimer_1 SSCM SIUL	I/O O I/O — I	Slow	Medium	76	109	133
B[1]	PCR[17]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[17] CS7_1 ETC[3] DEBUG[1] RXD EIRQ[16]	SIUL DSPI_1 eTimer_1 SSCM FlexCAN_0 SIUL	I/O O I/O — I I	Slow	Medium	77	110	134
B[2]	PCR[18]	ALT0 ALT1 ALT2 ALT3 —	GPIO[18] TXD SOUT_4 DEBUG[2] EIRQ[17]	SIUL LINFlex_0 DSPI_4 SSCM SIUL	I/O O I/O — I	Slow	Medium	79	114	138
B[3]	PCR[19]	ALT0 ALT1 ALT2 ALT3 —	GPIO[19] — SCK_4 DEBUG[3] RXD	SIUL — DSPI_4 SSCM LINFlex_0	I/O — I/O — I	Slow	Medium	80	116	140
B[6]	PCR[22]	ALT0 ALT1 ALT2 ALT3 —	GPIO[22] clk_out CS2_2 clk_out_div256 EIRQ[18]	SIUL MC_CGL DSPI_2 MC_CGL SIUL	I/O O O O I	Slow	Medium	96	138	162
B[7]	PCR[23]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[23] — — — AN[0] RXD	SIUL — — — ADC_0 LINFlex_0	Input Only	—	—	29	43	51
B[8]	PCR[24]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[24] — — — AN[1] ETC[5]	SIUL — — — ADC_0 eTimer_0	Input Only	—	—	31	47	55

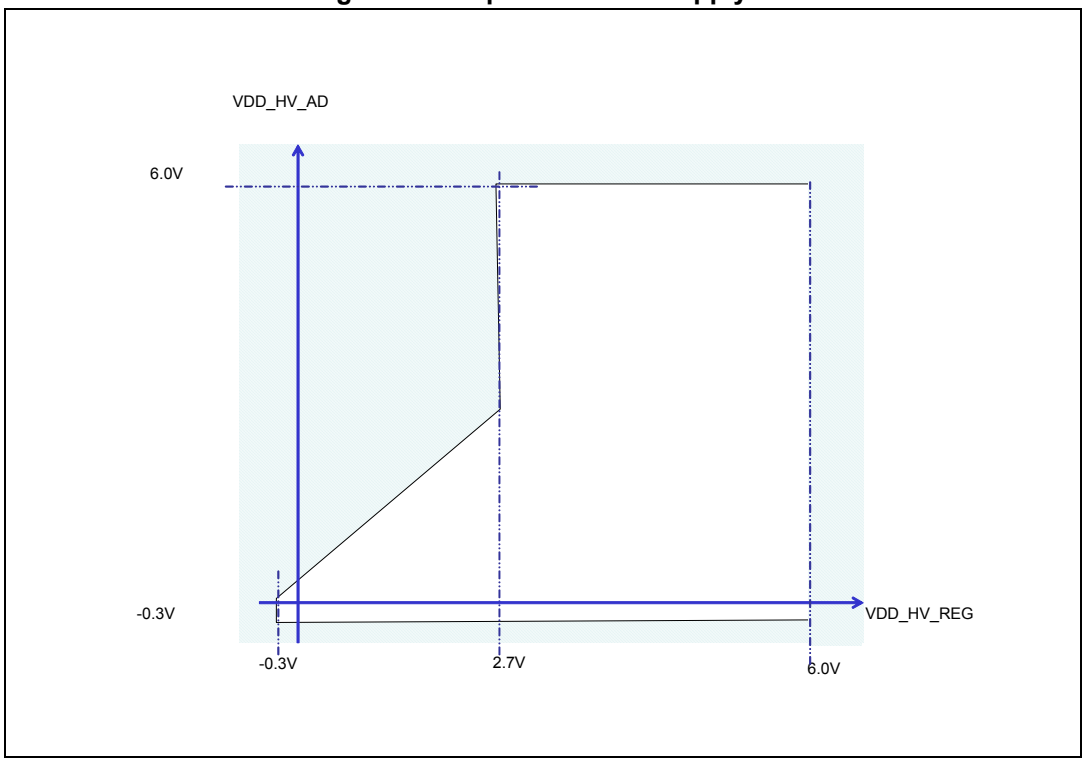
Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
D[7]	PCR[55]	ALT0 ALT1 ALT2 ALT3 —	GPIO[55] CS3_1 — CS4_0 SIN_3	SIUL DSPI_1 — DSPI_0 DSPI_3	I/O O — O I	Slow	Medium	26	37	45
D[8]	PCR[56]	ALT0 ALT1 ALT2 ALT3	GPIO[56] CS2_1 RDY CS5_0	SIUL DSPI_1 nexus_0 DSPI_0	I/O O O O	Slow	Medium	21	32	40
D[9]	PCR[57]	ALT0 ALT1 ALT2 ALT3	GPIO[57] — TXD CS6_1	SIUL — LINFlex_1 DSPI_1	I/O — O O	Slow	Medium	15	26	34
D[10]	PCR[58]	ALT0 ALT1 ALT2 ALT3	GPIO[58] — CS0_3 —	SIUL — DSPI_3 —	I/O — I/O —	Slow	Medium	53	76	92
D[11]	PCR[59]	ALT0 ALT1 ALT2 ALT3	GPIO[59] — CS1_3 SCK_3	SIUL — DSPI_3 DSPI_3	I/O — O I/O	Slow	Medium	54	78	94
D[12]	PCR[60]	ALT0 ALT1 ALT2 ALT3 —	GPIO[60] — — CS7_1 RXD	SIUL — — DSPI_1 LINFlex_1	I/O — — O I	Slow	Medium	70	99	123
D[13]	PCR[61]	ALT0 ALT1 ALT2 ALT3	GPIO[61] — CS2_3 SOUT_3	SIUL — DSPI_3 DSPI_3	I/O — O O	Slow	Medium	67	95	119
D[14]	PCR[62]	ALT0 ALT1 ALT2 ALT3 —	GPIO[62] — CS3_3 — SIN_3	SIUL — DSPI_3 — DSPI_3	I/O — O — I	Slow	Medium	73	105	129
D[15]	PCR[63]	ALT0 ALT1 ALT2 ALT3 —	GPIO[63] — — — AN[20]	SIUL — — — ADC_0	Input Only	—	—	41	58	66

Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
Port E										
E[0]	PCR[64]	ALT0 ALT1 ALT2 ALT3 —	GPIO[64] — — — AN[21]	SIUL — — — ADC_0	Input Only	—	—	46	68	80
E[1]	PCR[65]	ALT0 ALT1 ALT2 ALT3 —	GPIO[65] — — — AN[4]	SIUL — — — ADC_0	Input Only	—	—	27	39	47
E[2]	PCR[66]	ALT0 ALT1 ALT2 ALT3 —	GPIO[66] — — — AN[5]	SIUL — — — ADC_0	Input Only	—	—	32	49	57
E[3]	PCR[67]	ALT0 ALT1 ALT2 ALT3 —	GPIO[67] — — — AN[6]	SIUL — — — ADC_0	Input Only	—	—	—	40	48
E[4]	PCR[68]	ALT0 ALT1 ALT2 ALT3 —	GPIO[68] — — — AN[7]	SIUL — — — ADC_0	Input Only	—	—	—	42	50
E[5]	PCR[69]	ALT0 ALT1 ALT2 ALT3 —	GPIO[69] — — — AN[8]	SIUL — — — ADC_0	Input Only	—	—	—	44	52
E[6]	PCR[70]	ALT0 ALT1 ALT2 ALT3 —	GPIO[70] — — — AN[9]	SIUL — — — ADC_0	Input Only	—	—	—	46	54

Figure 6. Independent ADC supply[e]



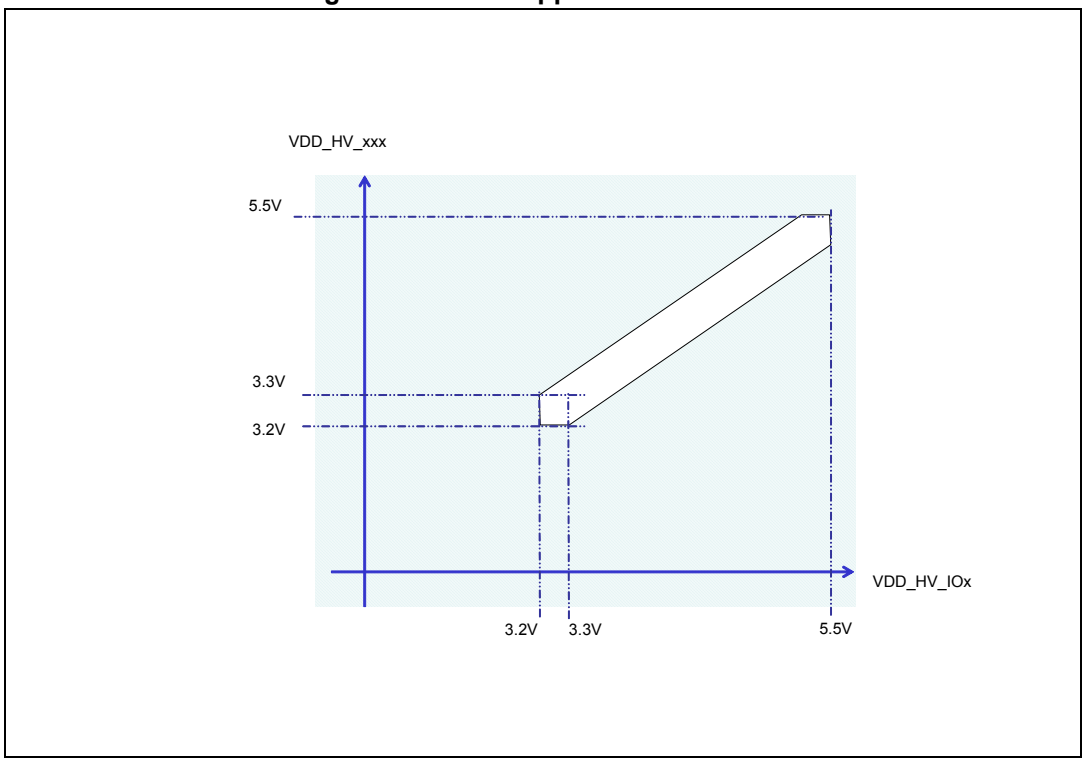
3.4 Recommended operating conditions

Table 10. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Min	Max[1]	Unit
V_{SS_HV}	SR	Digital ground	—	0	0	V
$V_{DD\_HV\_IOx}$[2]	SR	5.0 V input/output supply voltage	—	4.5	5.5	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_FL}$	SR	5.0 V code and data flash memory supply voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$ – 0.1	$V_{DD\_HV\_IOx}$ + 0.1	
$V_{SS\_HV\_FL}$	SR	Code and data flash memory ground	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	5.0 V crystal oscillator amplifier supply voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$ – 0.1	$V_{DD\_HV\_IOx}$ + 0.1	
$V_{SS\_HV\_OSC}$	SR	5.0 V crystal oscillator amplifier reference voltage	—	0	0	V

e. Device design targets the removal of this conditions. To be confirmed by design during device validation.

Figure 7. Power supplies constraints[f]



The SPC56xP54x/SPC56xP60x supply architecture provides an ADC supply that is managed independently of standard V_{DD_HV} supply. *Figure 8* shows the constraints of the ADC power supply.

f. IO AC and DC characteristics are guaranteed only in the range 3.0 V–3.6 V when PAD3V5V is low, and in the range 4.5 V–5.5 V when PAD3V5V is high.

Figure 10. Power-up typical sequence

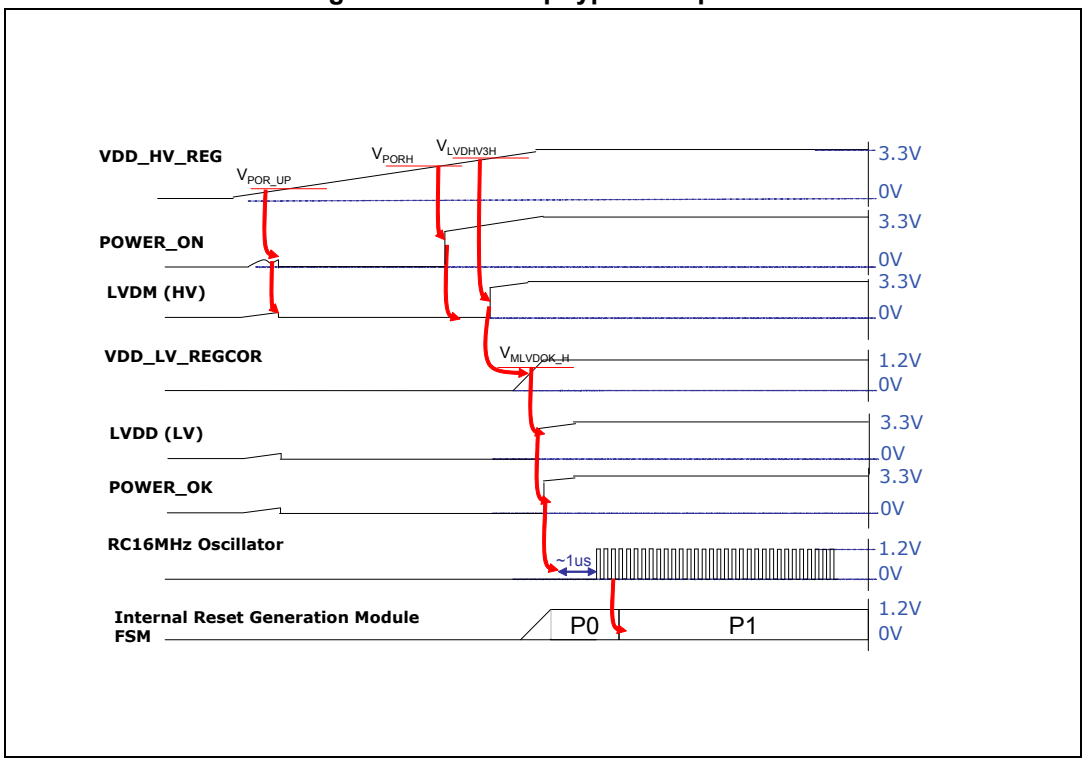
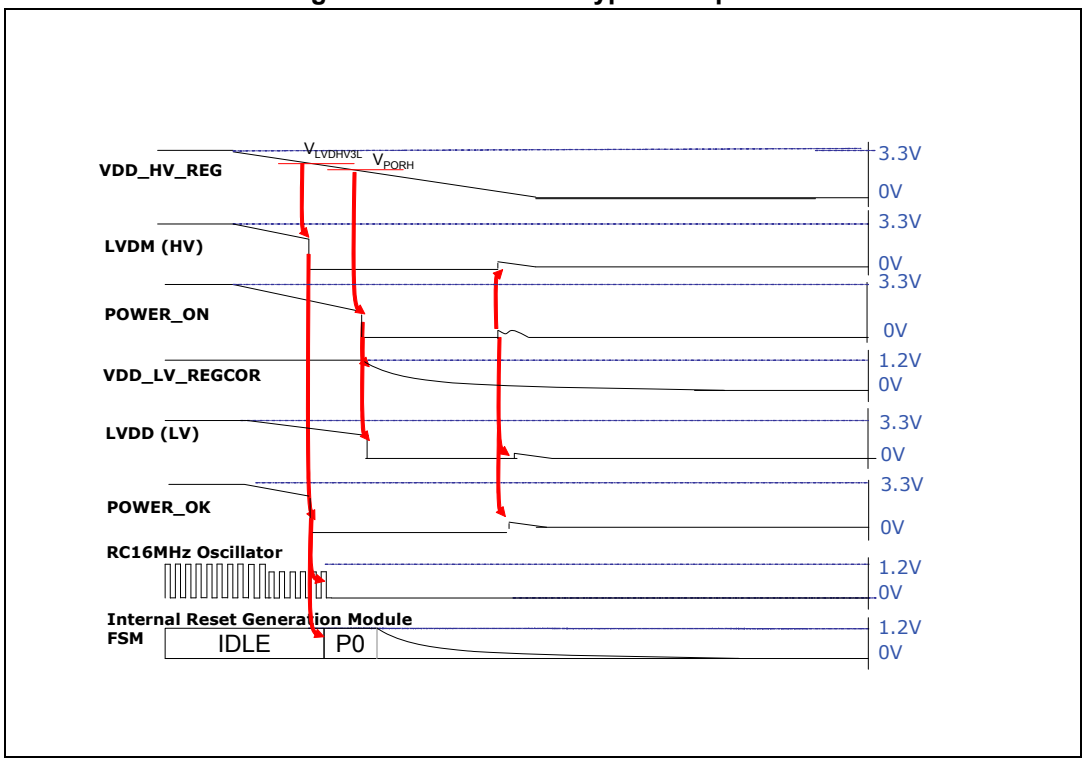


Figure 11. Power-down typical sequence



2. “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self clocked mode.
3. Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.
4. f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.
5. This value is determined by the crystal manufacturer and board design.
6. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.
7. Proper PC board layout procedures must be followed to achieve specifications.
8. Values are obtained with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).
9. Short term jitter is measured on the clock rising edge at cycle n and cycle n+4.
10. This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this PLL, load capacitors should not exceed these limits.
11. This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
12. This value is true when operating at frequencies above 60 MHz, otherwise f_{CS} is 2% (above 64 MHz).
13. Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

3.14 16 MHz RC oscillator electrical characteristics

Table 31. 16 MHz RC oscillator electrical characteristics

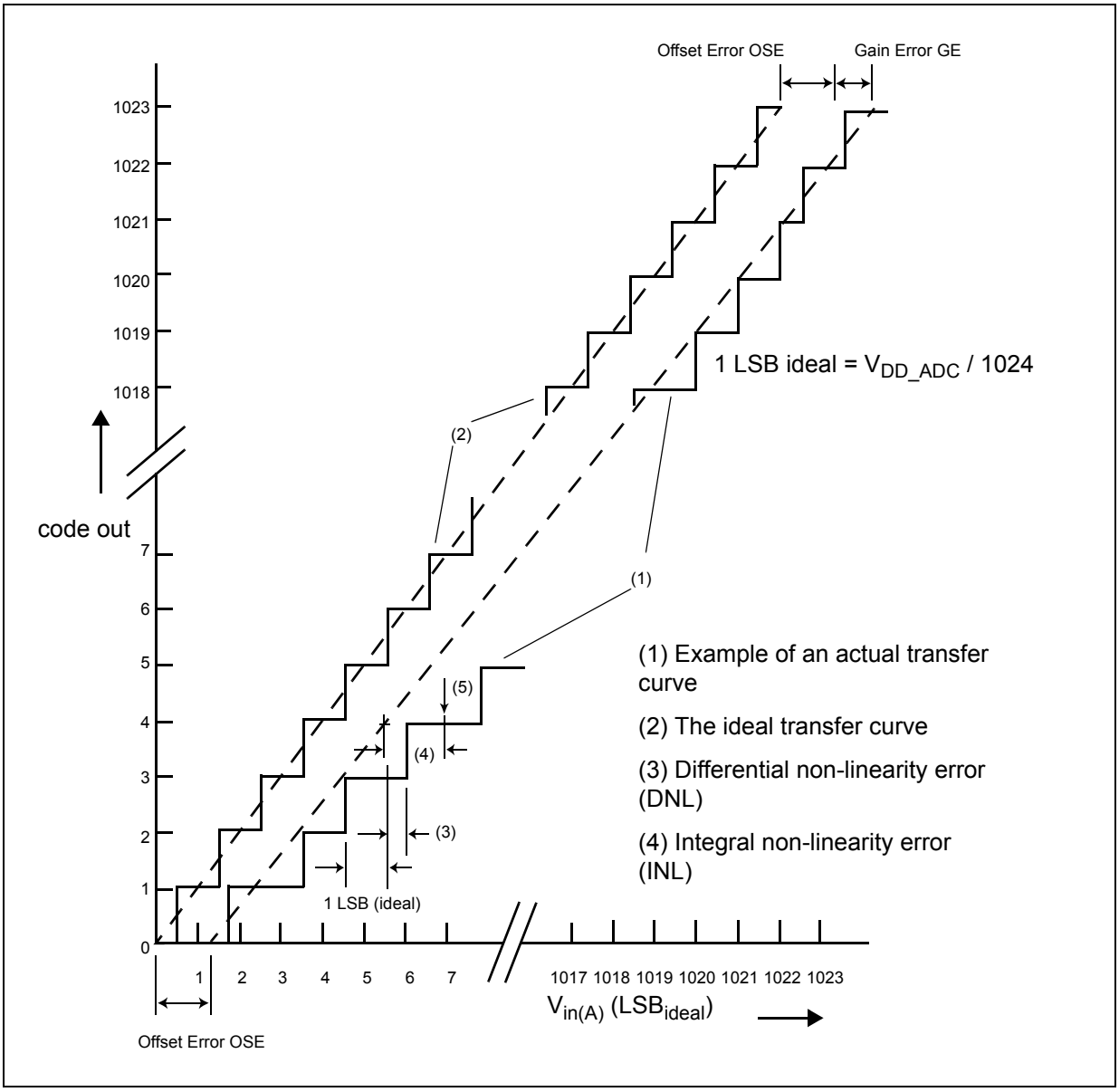
Symbol		Parameter	Conditions	Min	Typ	Max	Unit
f_{RC}	P	RC oscillator frequency	T_A = 25 °C	—	16	—	MHz
Δ_{RCMVAR}	P	Fast internal RC oscillator variation over temperature and supply with respect to f_{RC} at T_A = 25 °C in high-frequency configuration	—	–6	—	6	%
$\Delta_{RCMTRIM}$	T	Post Trim Accuracy: The variation of the PTF(1) from the 16 MHz	T_A = 25 °C	–1	—	1	%
$\Delta_{RCMSTEP}$	T	Fast internal RC oscillator trimming step	T_A = 25 °C	—	1.6	—	%

1. PTF = Post Trimming Frequency: The frequency of the output clock after trimming at typical supply voltage and temperature

3.15 Analog-to-Digital converter (ADC) electrical characteristics

The device provides a 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

Figure 15. ADC characteristics and error definitions



3.15.1 Input impedance and ADC accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high-frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuate the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the source impedance value of the transducer or circuit supplying the analog signal to be measured.

Figure 20. Start-up reset requirements(g)

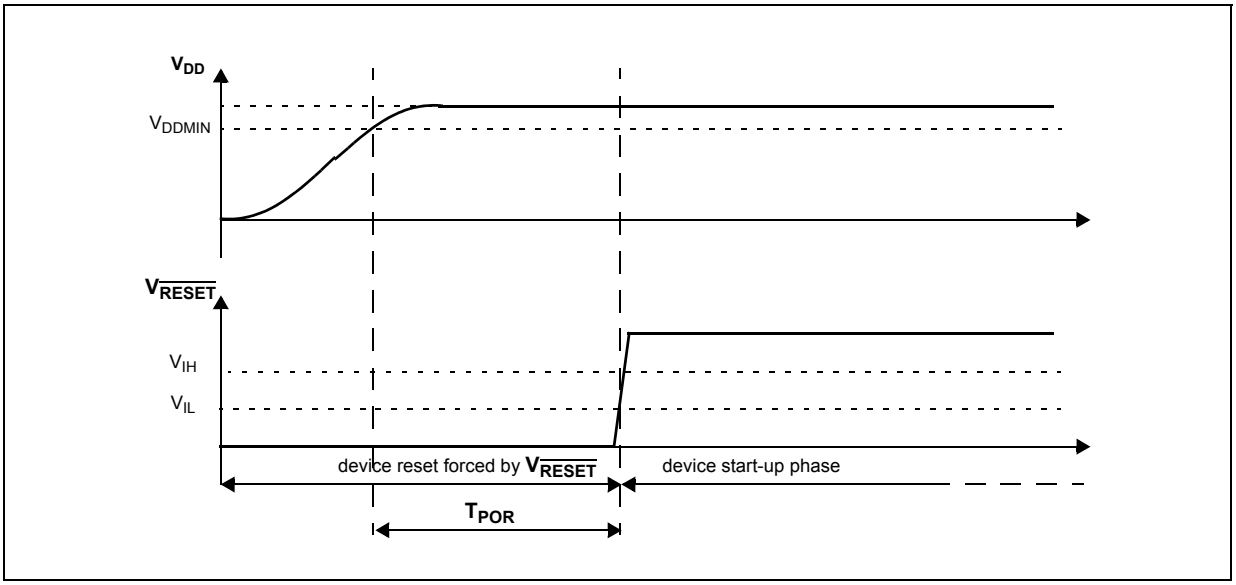
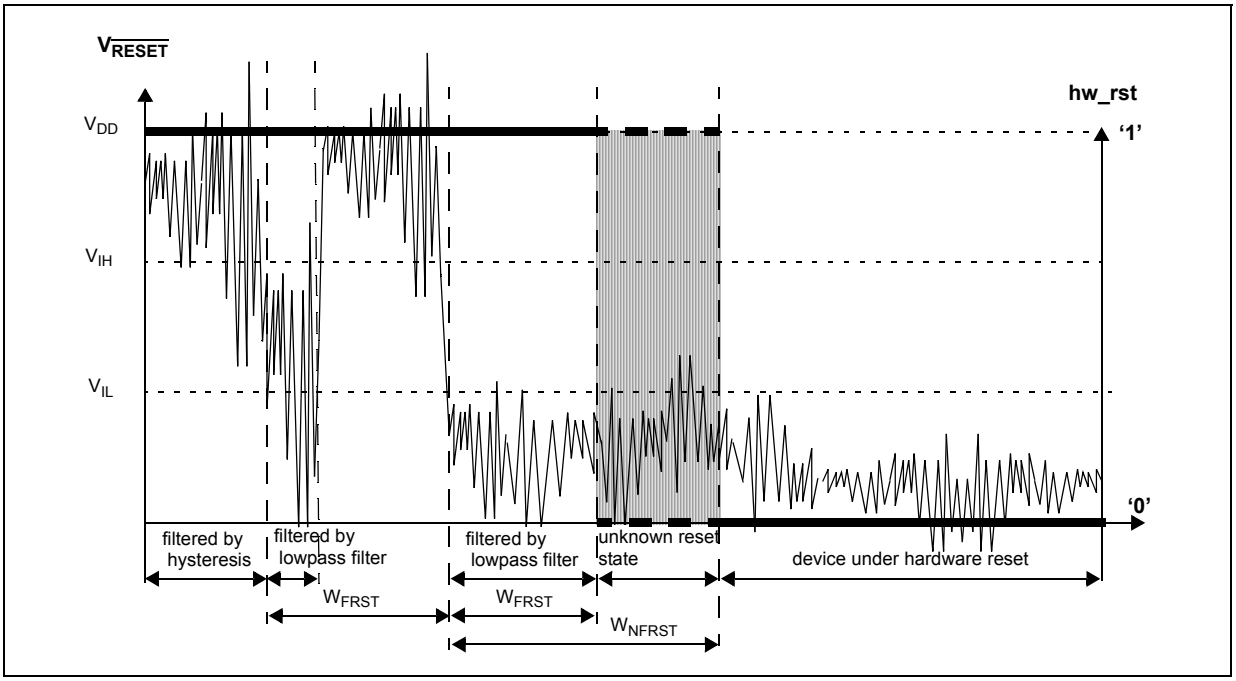


Figure 21. Noise filtering on reset signal



g. The output drive provided is open drain and hence must be terminated by an external resistor of value 1 kΩ.

Figure 32. DSPI classic SPI timing — slave, CPHA = 1

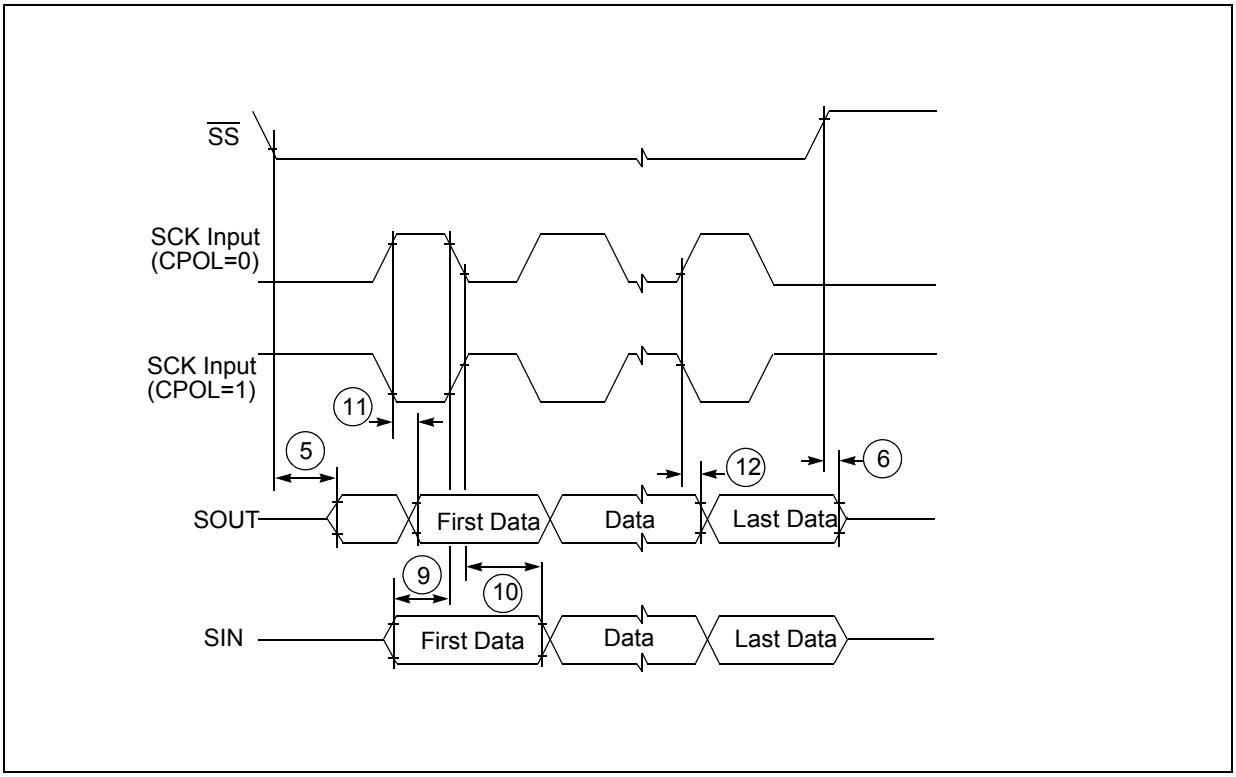


Figure 33. DSPI modified transfer format timing — master, CPHA = 0

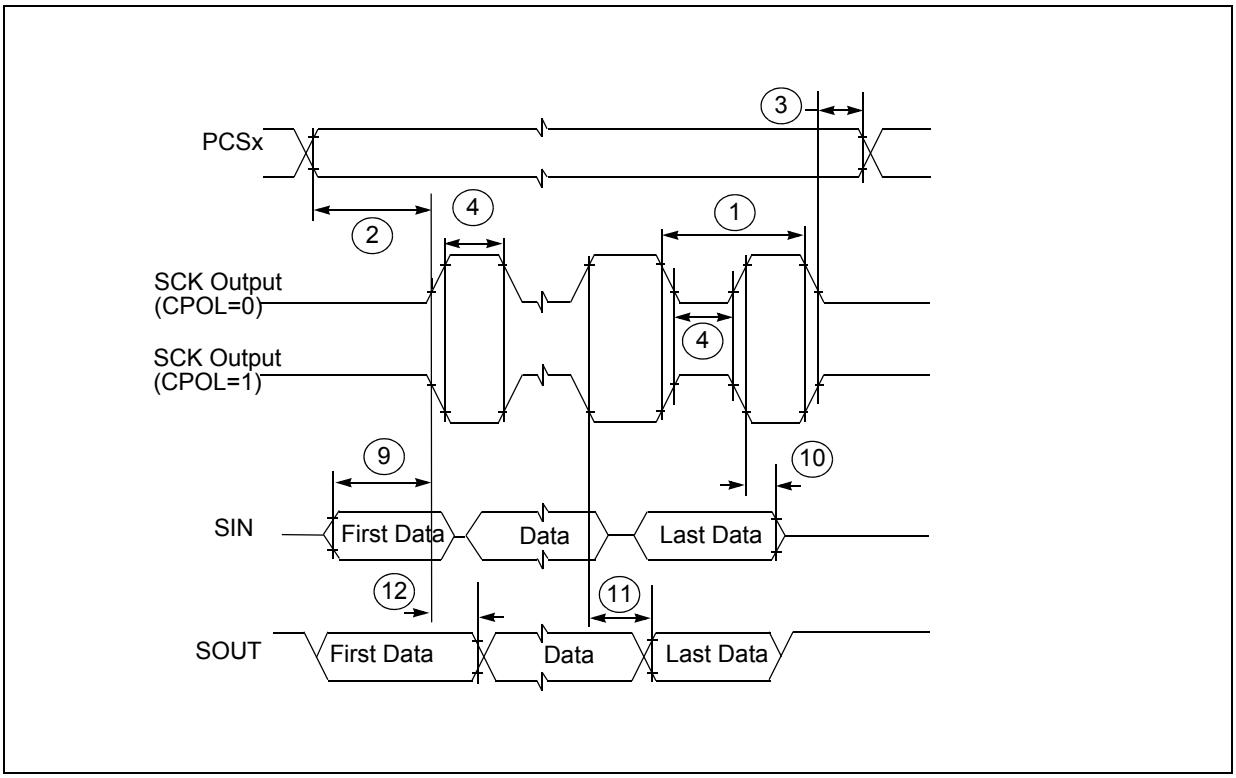


Figure 34. DSPI modified transfer format timing — master, CPHA = 1

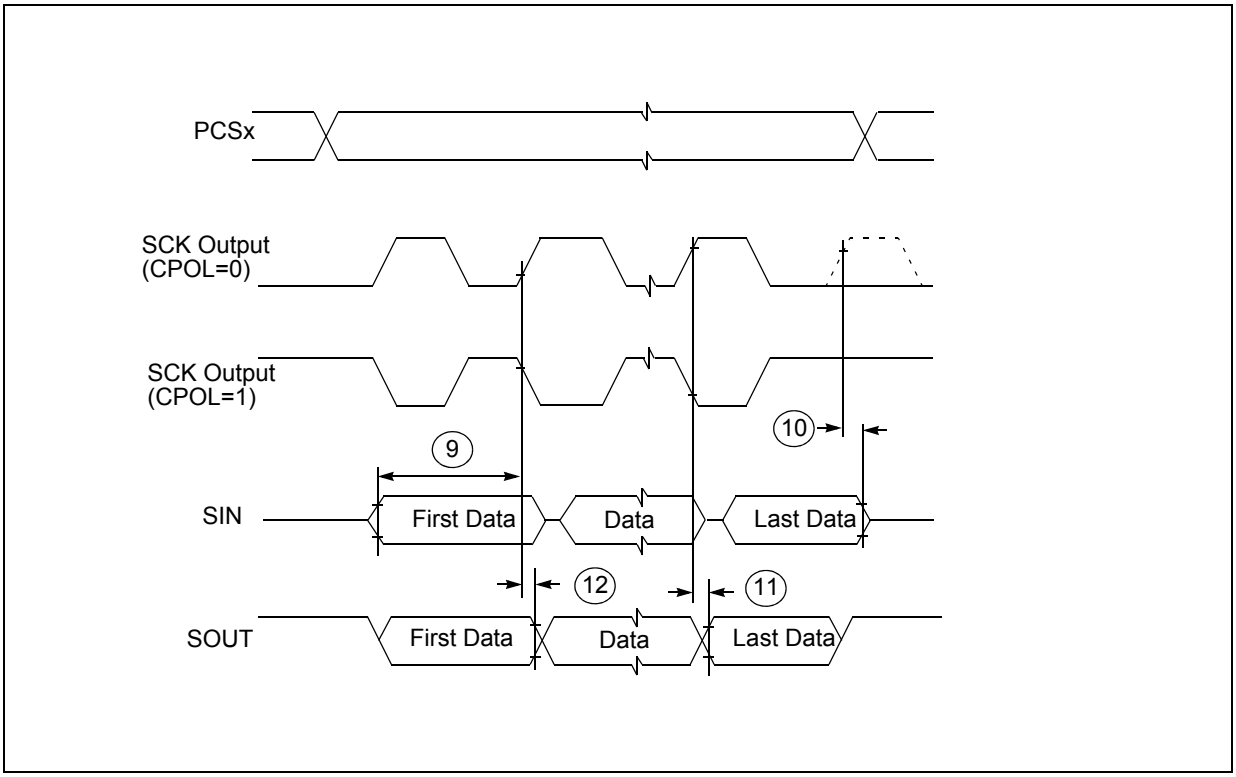


Figure 35. DSPI modified transfer format timing — slave, CPHA = 0