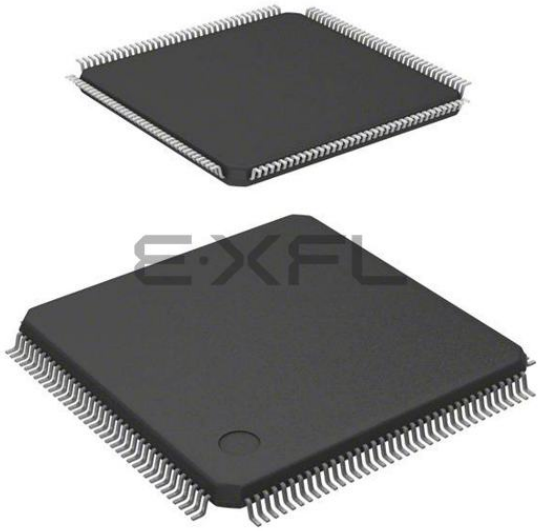

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 26x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p54l5beaby

Table 2. SPC56xP54x/SPC56xP60x device comparison (continued)

Feature		SPC560P54	SPC560P60	SPC56AP54	SPC56AP60
Enhanced DMA (direct memory access) channels		16			
FlexRay		Yes (64 message buffer)			
FlexCAN (controller area network)		3(1),(2)			
Safety port		Yes (via third FlexCAN module)			
FCCU (fault collection and control unit)		Yes(3)			
CTU (cross triggering unit)		Yes			
eTimer channels		2 × 6			
FlexPWM (pulse-width modulation) channels		No			
Analog-to-digital converters (ADC)		One (10-bit, 27-channel)(4)			
LINFlex modules		2 (1 × Master/Slave, 1 × Master only)(5)			
DSPI (deserial serial peripheral interface) modules		5(6)			
CRC (cyclic redundancy check) units		2(7)			
JTAG interface		Yes			
Nexus port controller (NPC)		Yes (Level 2+)(8)			
Supply	Digital power supply(9)	3.3 V or 5 V single supply with external transistor			
	Analog power supply	3.3 V or 5 V			
	Internal RC oscillator	16 MHz			
	External crystal oscillator	4–40 MHz			
Packages		LQFP100 LQFP144			LQFP100 LQFP144 LQFP176(10)
Temperature	Standard ambient temperature	–40 to 125 °C			

1. Each FlexCAN module has 32 message buffers.
2. One FlexCAN module can act as a Safety Port with a bit rate as high as 7.5 Mbit/s.
3. Enhanced FCCU version.
4. Same amount of ADC channels as on SPC560P44/50 not considering the internally connected ones. 26 channels on LQFP144 and 16 channels on LQFP100.
5. LinFlex_1 is Master Only.
6. Increased number of CS for DSPI_1.
7. Upgraded specification with addition of 8-bits polynomial (CRC-8 VDA CAN) support and 3rd context.
8. Improved debugging capability with data trace capability and increased Nexus throughput available on emulation package.
9. 3.3 V range and 5 V range correspond to different orderable parts.
10. Software development package only. Not available for production.

SPC56xP54x/SPC56xP60x is present on the market in two different options enabling different features: Full-featured, and Airbag configuration. *Table 3* shows the main differences between the two versions.

Table 3. SPC56xP54x/SPC56xP60x device configuration difference

Feature	Enhanced Full-featured	Full-featured	Airbag
FlexCAN (controller area network)	3	2	2
CTU (cross triggering unit)	Yes		No
FlexRay	Yes (64 message buffer)		No
DSPI (deserial serial peripheral interface) modules	5		4
CRC (cyclic redundancy check) unit	2		1

1.4 Block diagram

Figure 1 shows a top-level block diagram of the SPC56xP54x/SPC56xP60x MCU. *Table 4* summarizes the functions of the blocks.

The DSPI modules provide these features:

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- Up to 28 chip select lines available
  - 8 each on DSPI_0 and DSPI_1
  - 4 each on DSPI_2, DSPI_3, and DSPI_4
- 8 clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for deglitching
- FIFOs for buffering up to 5 transfers on the transmit and receive side
- Queueing operation possible through use of the eDMA
- General purpose I/O functionality on pins when not used for SPI

1.5.23 eTimer

Two eTimer modules are provided, each with six 16-bit general purpose up/down timer/counter per module. The following features are implemented:

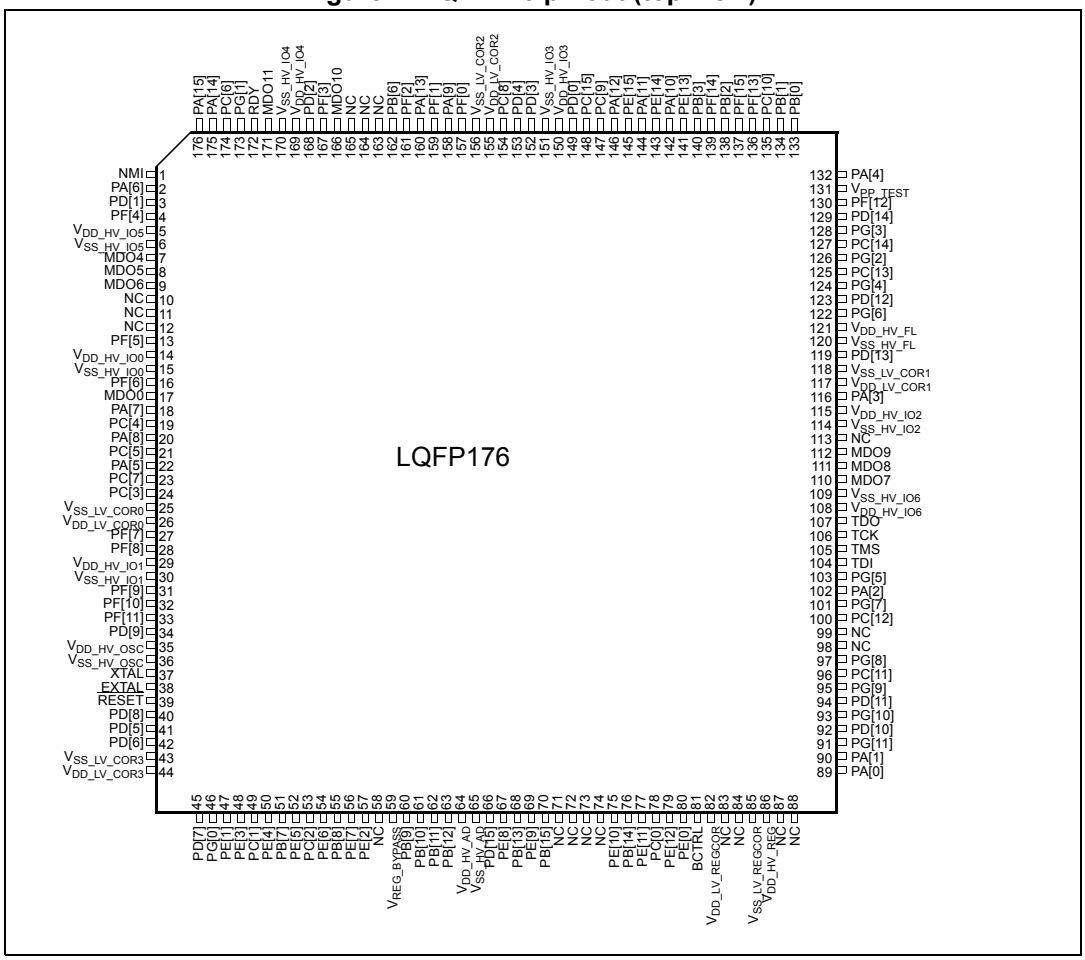
- Individual channel capability
  - Input capture trigger
  - Output compare
  - Double buffer (to capture rising edge and falling edge)
  - Separate prescaler for each counter
  - Selectable clock source
  - 0 % to 100% pulse measurement
  - Rotation direction flag (Quad decoder mode)
- Maximum count rate
  - Equals peripheral clock/2 — for external event counting
  - Equals peripheral clock — for internal clock counting
- Cascadeable counters
- Programmable count modulo
- Quadrature decode capabilities
- Counters can share available input pins
- Count once or repeatedly
- Preloadable counters
- Pins available as GPIO when timer functionality not in use

2 Package pinouts and signal descriptions

2.1 Package pinouts

The LQFP pinouts are shown in the following figures.

Figure 2. LQFP176 pinout (top view)[b]



b. Software development package only. Not available for production.

Table 5. Supply pins (continued)

Supply		Pin		
Symbol	**Description**	**LQFP 100**	**LQFP 144**	**LQFP 176(1)**
$V_{DD\_HV\_REG}$ (3.3 V or 5.0 V)	Voltage regulator supply voltage	50	72	86
$V_{DD\_LV\_REGCOR}$	1.2 V decoupling(2) pins for core logic supply and voltage regulator feedback. Decoupling capacitor must be connected between this pins and $V_{SS\_LV\_REGCOR}$.	48	70	82
$V_{SS\_LV\_REGCOR}$	1.2 V decoupling(2) pins for core logic GND and voltage regulator feedback. Decoupling capacitor must be connected between this pins and $V_{DD\_LV\_REGCOR}$.	49	71	85
ADC0 reference and supply voltage				
$V_{DD\_HV\_AD}$	ADC supply and high reference voltage	39	56	64
$V_{SS\_HV\_AD}$	ADC ground and low reference voltage	40	57	65
Power supply pins (3.3 V or 5.0 V)				
$V_{DD\_HV\_IO0}$	Input/Output supply voltage	—	6	14
$V_{SS\_HV\_IO0}$	Input/Output ground	—	7	15
$V_{DD\_HV\_IO1}$	Input/Output supply voltage	13	21	29
$V_{SS\_HV\_IO1}$	Input/Output ground	14	22	30
$V_{DD\_HV\_IO2}$	Input/Output supply voltage	63	91	115
$V_{SS\_HV\_IO2}$	Input/Output ground	62	90	114
$V_{DD\_HV\_IO3}$	Input/Output supply voltage	87	126	150
$V_{SS\_HV\_IO3}$	Input/Output ground	88	127	151
$V_{DD\_HV\_IO4}$	Input/Output supply voltage	—	—	169
$V_{SS\_HV\_IO4}$	Input/Output ground	—	—	170
$V_{DD\_HV\_IO5}$	Input/Output supply voltage	—	—	5
$V_{SS\_HV\_IO5}$	Input/Output ground	—	—	6
$V_{DD\_HV\_IO6}$	Input/Output supply voltage	—	—	108
$V_{SS\_HV\_IO6}$	Input/Output ground	—	—	109
$V_{DD\_HV\_FL}$	Code and data flash supply voltage	69	97	121
$V_{SS\_HV\_FL}$	Code and data flash supply ground	68	96	120
$V_{DD\_HV\_OSC}$	Crystal oscillator amplifier supply voltage	16	27	35
$V_{SS\_HV\_OSC}$	Crystal oscillator amplifier ground	17	28	36
Power supply pins (1.2 V)				
$V_{DD\_LV\_COR0}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR0}$ pin.	12	18	26

Table 5. Supply pins (continued)

Supply		Pin		
Symbol	Description	LQFP 100	LQFP 144	LQFP 176[1]
$V_{SS\_LV\_COR0}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR0}$ pin.	11	17	25
$V_{DD\_LV\_COR1}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR1}$ pin.	65	93	117
$V_{SS\_LV\_COR1}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR1}$ pin.	66	94	118
$V_{DD\_LV\_COR2}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR2}$ pin.	92	131	155
$V_{SS\_LV\_COR2}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR\ 2}$ pin.	93	132	156
$V_{DD\_LV\_COR3}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR3}$ pin.	25	36	44
$V_{SS\_LV\_COR3}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR\ 3}$ pin.	24	35	43

1. LQFP176 available only as development package.
2. See datasheet Voltage Regulator Electrical Characteristics section for more details.

2.2.2 System pins

Table 6 and *Table 7* contain information on pin functions for the SPC56xP54x/SPC56xP60x devices. The pins listed in *Table 6* are single-function pins. The pins shown in *Table 7* are multi-function pins, programmable via their respective Pad Configuration Register (PCR) values.

Table 6. System pins

Symbol	Description	Direction	Pad Speed[1]		Pin		
			SRC=0	SRC=1	LQFP 100	LQFP 144	LQFP 176[2]
Dedicated pins							
MDO0	Nexus Message Data Output—line 0	Output Only	Fast		—	9	17
MDO4	Nexus Message Data Output—line 4	Output Only	Fast		—	—	7

Table 6. System pins (continued)

Symbol	Description	Direction	Pad Speed[1]		Pin		
			SRC=0	SRC=1	LQFP 100	LQFP 144	LQFP 176[2]
MDO5	Nexus Message Data Output—line 5	Output Only	Fast		—	—	8
MDO6	Nexus Message Data Output—line 6	Output Only	Fast		—	—	9
MDO7	Nexus Message Data Output—line 7	Output Only	Fast		—	—	110
MDO8	Nexus Message Data Output—line 8	Output Only	Fast		—	—	111
MDO9	Nexus Message Data Output—line 9	Output Only	Fast		—	—	112
MDO10	Nexus Message Data Output—line 10	Output Only	Fast		—	—	166
MDO11	Nexus Message Data Output—line 11	Output Only	Fast		—	—	171
RDY	Nexus ready output	Output Only	—	—	—	—	172
NMI	Non-Maskable Interrupt	Input Only	—	—	1	1	1
XTAL	Analog output of the oscillator amplifier circuit. Needs to be grounded if oscillator is used in bypass mode.	—	—	—	18	29	37
EXTAL	Analog input of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode.	—	—	—	19	30	38
TMS[3]	JTAG state machine control	Input Only	—	—	59	87	105
TCK[3]	JTAG clock	Input Only	—	—	60	88	106
TDI[3]	JTAG data input	Input Only	—	—	58	86	104
TDO[3]	JTAG data output	Output Only	—	—	61	89	107
Reset pin							
$\overline{\text{RESET}}$[4]	Bidirectional reset with Schmitt trigger characteristics and noise filter	Bidirectional	Medium	—	20	31	39
Test pin							
$V_{PP\ TEST}$	Pin for testing purpose only. To be tied to ground in normal operating mode.	—	—	—	74	107	131
V_{REG_BYPASS}	Pin for testing purpose only. To be tied to ground in normal operating mode.	—	—	—	34	51	59

1. SRC values refer to the value assigned to the Slew Rate Control bits of the pad configuration register.

3.3 Absolute maximum ratings

Table 9. Absolute maximum ratings(1)

Symbol		Parameter	Conditions	Min	Max(2)	Unit
V_{SS_HV}	SR	Digital ground	—	0	0	V
$V_{DD\_HV\_IOx}$(3)	SR	3.3 V / 5.0 V input/output supply voltage with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
$V_{DD\_HV\_FL}$	SR	3.3 V / 5.0 V code and data flash memory supply voltage with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3	
$V_{SS\_HV\_FL}$	SR	Code and data flash memory ground with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
$V_{DD\_HV\_OSC}$	SR	3.3 V / 5.0 V crystal oscillator amplifier supply voltage with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3	
$V_{SS\_HV\_OSC}$	SR	3.3 V / 5.0 V crystal oscillator amplifier reference voltage with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
$V_{DD\_HV\_REG}$	SR	3.3 V / 5.0 V voltage regulator supply voltage with respect to ground (V_{SS_HV})	—	– 0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	– 0.3	$V_{DD\_HV\_IOx}$ + 0.3	
$V_{DD\_HV\_AD}$	SR	3.3 V / 5.0 V ADC supply and high reference voltage with respect to ground (V_{SS_HV})	$V_{DD\_HV\_REG}$ < 2.7 V	– 0.3	$V_{DD\_HV\_REG}$ + 0.3	V
			$V_{DD\_HV\_REG}$ > 2.7 V	– 0.3	6.0	
$V_{SS\_HV\_AD}$	SR	ADC ground and low reference voltage with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
TV_{DD}	SR	Slope characteristics on all V_{DD} during power up(4) with respect to ground (V_{SS_HV})	—	3.0(5)	500 x 10^3 (0.5 [V/µs])	V/s
V_{IN}	SR	Voltage on any pin with respect to ground ($V_{SS\_HV\_IOx}$) with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3	
V_{INAN}	SR	Analog input voltage	$V_{DD\_HV\_REG}$ < 2.7 V	$V_{SS\_HV\_AD}$ – 0.3	$V_{DD\_HV\_AD}$ + 0.3	V
			$V_{DD\_HV\_REG}$ > 2.7 V	$V_{SS\_HV\_AD}$	$V_{DD\_HV\_AD}$	V
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA

Table 11. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Min	Max(1)	Unit
$V_{DD\_HV\_REG}$	SR	3.3 V voltage regulator supply voltage	—	3.0	3.6	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$ – 0.1	$V_{DD\_HV\_IOx}$ + 0.1	
$V_{DD\_HV\_AD}$	SR	3.3 V ADC supply and high reference voltage	—	3.0	5.5	V
			Relative to $V_{DD\_HV\_REG}$	$V_{DD\_HV\_REG}$ – 0.1	5.5	
$V_{SS\_HV\_AD}$	SR	ADC ground and low reference voltage	—	0	0	V
$V_{DD\_LV\_REGCOR}$(3),(4)	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_REGCOR}$(3)	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_CORx}$(3),(4)	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_CORx}$(3)	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	—	–40	125	°C

1. Parametric figures can be out of specification when voltage drops below 4.5 V, however, guaranteeing the full functionality. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.
2. The difference between each couple of voltage supplies must be less than 100 mV, $|V_{DD\_HV\_IOy} – V_{DD\_HV\_IOx}| < 100$ mV.
3. To be connected to emitter of external NPN. Low voltage supplies are not under user control—these are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds ($V_{SS\_LV\_xxx}$) must be shorted to high voltage grounds ($V_{SS\_HV\_xxx}$) and the low voltage supply pins ($V_{DD\_LV\_xxx}$) must be connected to the external ballast emitter.
4. The low voltage supplies ($V_{DD\_LV\_xxx}$) are not all independent.
$V_{DD\_LV\_COR1}$ and $V_{DD\_LV\_COR2}$ are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash memory module. Similarly, $V_{SS\_LV\_COR1}$ and $V_{SS\_LV\_COR2}$ are internally shorted.
$V_{DD\_LV\_REGCOR}$ and $V_{DD\_LV\_REGCORx}$ are physically shorted internally, as are $V_{SS\_LV\_REGCOR}$ and $V_{SS\_LV\_CORx}$.

Figure 7 shows the constraints of the different power supplies.

Table 17. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$V_{DD\_LV\_REGCOR}$	CC	P	Output voltage under maximum load run supply current configuration	Post-trimming	1.15	—	1.32	V
C_{DEC1}	SR	—	External decoupling/stability ceramic capacitor	BJT from *Table 16*. 3 capacitances (i.e. X7R or X8R capacitors) with nominal value of 10 µF	19.5	30	—	µF
				BJT BC817, one capacitance of 22 µF	14.3	22		µF
R_{REG}	SR	—	Resulting ESR of all three capacitors of C_{DEC1}	BJT from *Table 16*. 3x10 µF. Absolute maximum value between 100 kHz and 10 MHz	—	—	50	mΩ
			Resulting ESR of the unique capacitor C_{DEC1}	BJT BC817, 1x 22 µF. Absolute maximum value between 100 kHz and 10 MHz	10	—	40	mΩ
C_{DEC2}	SR	—	External decoupling/stability ceramic capacitor	4 capacitances (i.e. X7R or X8R capacitors) with nominal value of 440 nF	1200	1760	—	nF
C_{DEC3}	SR	—	External decoupling/stability ceramic capacitor on $V_{DD\_HV\_REG}$	3 capacitances (i.e. X7R or X8R capacitors) with nominal value of 10 µF; C_{DEC3} has to be equal or greater than C_{DEC1}	19.5	30	—	µF
L_{Reg}	SR	—	Resulting ESL of $V_{DD\_HV\_REG}$, BCTRL and $V_{DD\_LV\_CORx}$ pins	—	—	—	15	nH

3.8.2 Voltage monitor electrical characteristics

The device implements a Power On Reset module to ensure correct power-up initialization, as well as three low voltage detectors to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the 5.0V ± 10% range
- LVDLVCOR monitors low voltage digital power domain

3.11.2 DC electrical characteristics (3.3 V)

Table 22 gives the DC electrical characteristics at 3.3 V (3.0 V < $V_{DD\_HV\_IOx}$ < 3.6 V, NVUSRO[PAD3V5V]=1) as described in *Figure 14*.

Figure 14. I/O input DC electrical characteristics definition

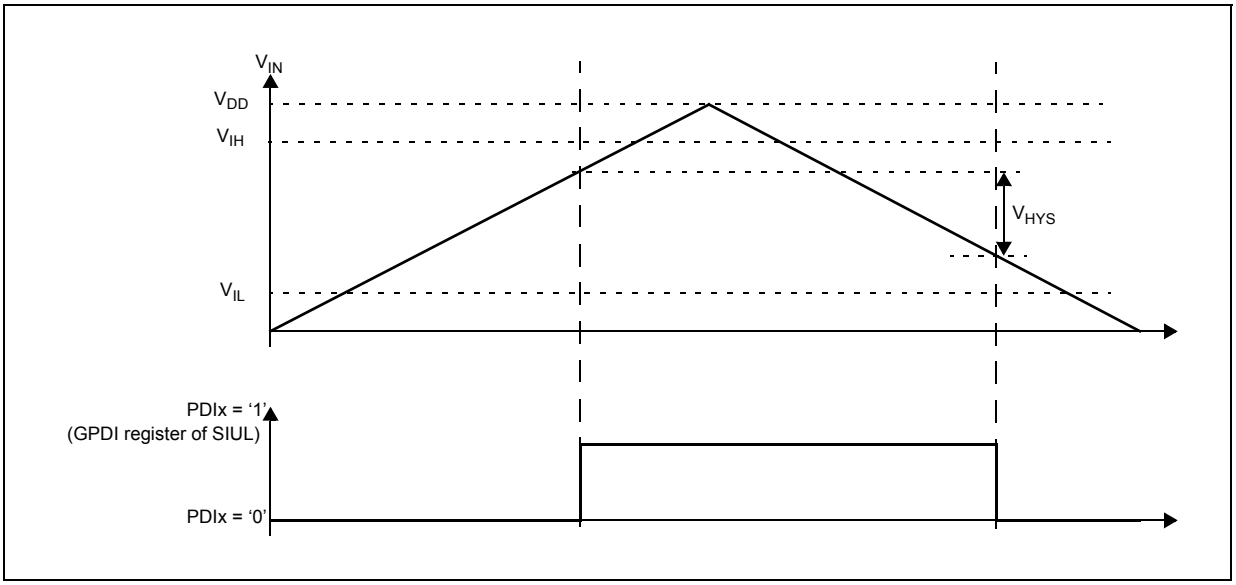
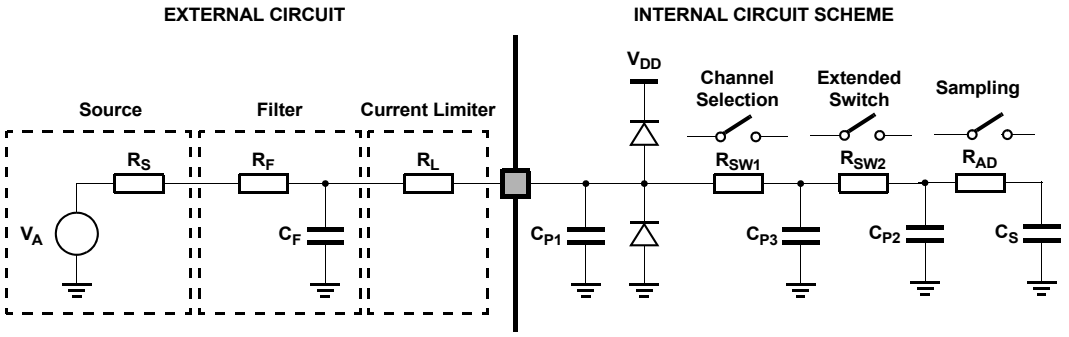


Table 22. DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V]=1)(1)

Symbol		Parameter	Conditions	Min	Max	Unit
V_{IL}	D	Minimum low level input voltage	—	–0.1(2)	—	V
V_{IL}	P	Maximum low level input voltage	—	—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IH}	P	Minimum high level input voltage	—	0.65 $V_{DD\_HV\_IOx}$	—	V
V_{IH}	D	Maximum high level input voltage	—	—	$V_{DD\_HV\_IOx}$ + 0.1(2)	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IOx}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 2 mA	—	0.5	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –2 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_F}	P	Fast, high level output voltage	I_{OL} = 11 mA	—	0.5	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –11 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_SYM}	P	Symmetric, high level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_SYM}	P	Symmetric, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
I_{PU}	P	Equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	

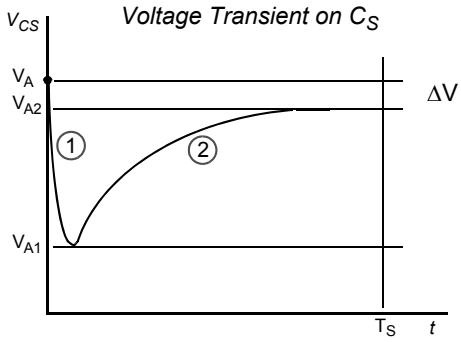
Figure 17. Input equivalent circuit (extended channels)



R_S: Source impedance
R_F: Filter resistance
C_F: Filter capacitance
R_L: Current limiter resistance
R_{SW1}: Channel selection switch impedance (two contributions, R_{SW1} and R_{SW2})
R_{AD}: Sampling switch impedance
C_P: Pin capacitance (two contributions, C_{P1}, C_{P2} and C_{P3})
C_S: Sampling capacitance

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in *Figure 16*): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

Figure 18. Transient behavior during sampling phase



$\Delta V < 0.5$ LSB

$\tau_1 < (R_{SW} + R_{AD})\, C_S << T_S$

$\tau_2 = R_L\,(C_S + C_{P1} + C_{P2})$

Table 32. ADC conversion characteristics (continued)

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
TUE	T	Total unadjusted error with current injection	16 precision channels	–3	—	3	LSB
TUE	T	Total unadjusted error with current injection	10 standard channels	–4	—	4	LSB

1. V_{DD} = 3.3 V to 3.6 V / 4.5 V to 5.5 V, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified and analog input voltage from $V_{SS\_HV\_AD}$ to $V_{DD\_HV\_AD}$.
2. V_{INAN} may exceed V_{SS_ADC} and V_{DD_ADC} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.
3. AD_clk clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
4. When configured to allow 60 MHz ADC, the minimum ADC clock speed is 9 MHz, below which precision is lost.
5. During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC_S}. After the end of the sample time t_{ADC_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC_S} depend on programming.
6. This parameter includes the sample time t_{ADC_S}.
7. 20 MHz ADC clock. Specific prescaler is programmed on MC_PLL_CLK to provide 20 MHz clock to the ADC.
8. See *Figure 16*.

3.16 Flash memory electrical characteristics

Table 33. Program and erase specifications

Symbol		Parameter	Conditions	Value				Unit
				Min	Typ[1]	Initial max[2]	Max[3]	
$T_{wprogram}$	P	Word Program (32 bits) Time[4]	Data Flash	—	30	70	500	µs
$T_{dwprogram}$	P	Double Word (64 bits) Program Time[4]	Code Flash	—	18	50	500	µs
T_{BKPRG}	P	Bank Program (64 KB)[4, 5]	Data Flash	—	0.49	1.2	4.1	s
	P	Bank Program (1056 KB)[4, 5]	Code Flash	—	2.6	6.6	66	s
T_{MDPRG}	P	Module Program (512 KB)[4]	Code Flash	—	1.3	1.65	33	s
$T_{16kpperase}$	P	16 KB Block Pre-program and Erase Time	Code Flash	—	200	500	5000	ms
			Data Flash		700	800		
$T_{32kpperase}$	P	32 KB Block Pre-program and Erase Time	Code Flash	—	300	600	5000	ms
$T_{64kpperase}$	P	64 KB Block Pre-program and Erase Time	Code Flash	—	400	900	5000	ms
$T_{128kpperase}$	P	128 KB Block Pre-program and Erase Time	Code Flash	—	600	1300	5000	ms
t_{ESRT}	P	Erase Suspend Request Rate[6]	Code Flash	20	—	—	—	ms
			Data Flash	10				

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3. The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
4. Actual hardware programming times. This does not include software overhead.
5. Typical bank programming time assumes that all cells are programmed in a single pulse. In reality some cells will require more than one pulse, adding a small overhead to total bank programming time (see Initial Max column).
6. Time between erase suspend resume and next erase suspend.

Table 34. Flash memory module life

Symbol		Parameter	Conditions	Value		Unit
				Min	Typ	
P/E	C	Number of program/erase cycles per block for 16 KB blocks over the operating temperature range (T_J)	—	100000	100000	cycles
P/E	C	Number of program/erase cycles per block for 32 KB blocks over the operating temperature range (T_J)	—	10000	100000	cycles
P/E	C	Number of program/erase cycles per block for 64 KB blocks over the operating temperature range (T_J)	—	10000	100000	cycles
P/E	C	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	—	1000	100000	cycles
Retention	C	Minimum data retention at 85 °C average ambient temperature(1)	Blocks with 0 – 1000 P/E cycles	20	—	years
			Blocks with 10000 P/E cycles	10	—	years
			Blocks with 100000 P/E cycles	5	—	years

1. Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

Table 35. Flash read access timing

Symbol	C	Parameter	Conditions(1)	Max	Unit
Fmax	C	Maximum working frequency for Code Flash at given number of WS in worst conditions	2 wait states	66	MHz
			0 wait states	22	
Fmax	C	Maximum working frequency for Data Flash at given number of WS in worst conditions	8 wait states	66	MHz

1. VDD = 3.3 V ± 10% / 5.0 V ± 10%, TA = –40 to 125 °C, unless otherwise specified.

3.17 AC specifications

3.17.1 Pad AC specifications

Table 36. Output pin transition times

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
T_{tr}	CC	D	Output transition time output pin[2] SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
		T		C_L = 50 pF		—	—	50	
		D		C_L = 100 pF		—	—	75	
T_{tr}	CC	D	Output transition time output pin[2] MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	
T_{tr}	CC	D	Output transition time output pin[2] FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	4	ns
				C_L = 50 pF		—	—	6	
				C_L = 100 pF		—	—	12	
				C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	4	
				C_L = 50 pF		—	—	7	
				C_L = 100 pF		—	—	12	
T_{sim}[3]	CC	T	Symmetric, same drive strength between N and P transistor	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	4	ns
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified.
2. C_L includes device and package capacitances (C_{PKG} < 5 pF).
3. Transition timing of both positive and negative slopes will differ maximum 50 %.

3.18 AC timing characteristics

3.18.1 $\overline{\text{RESET}}$ pin characteristics

The SPC56xP54x/SPC56xP60x implements a dedicated bidirectional RESET pin.

Figure 23. JTAG test access port timing

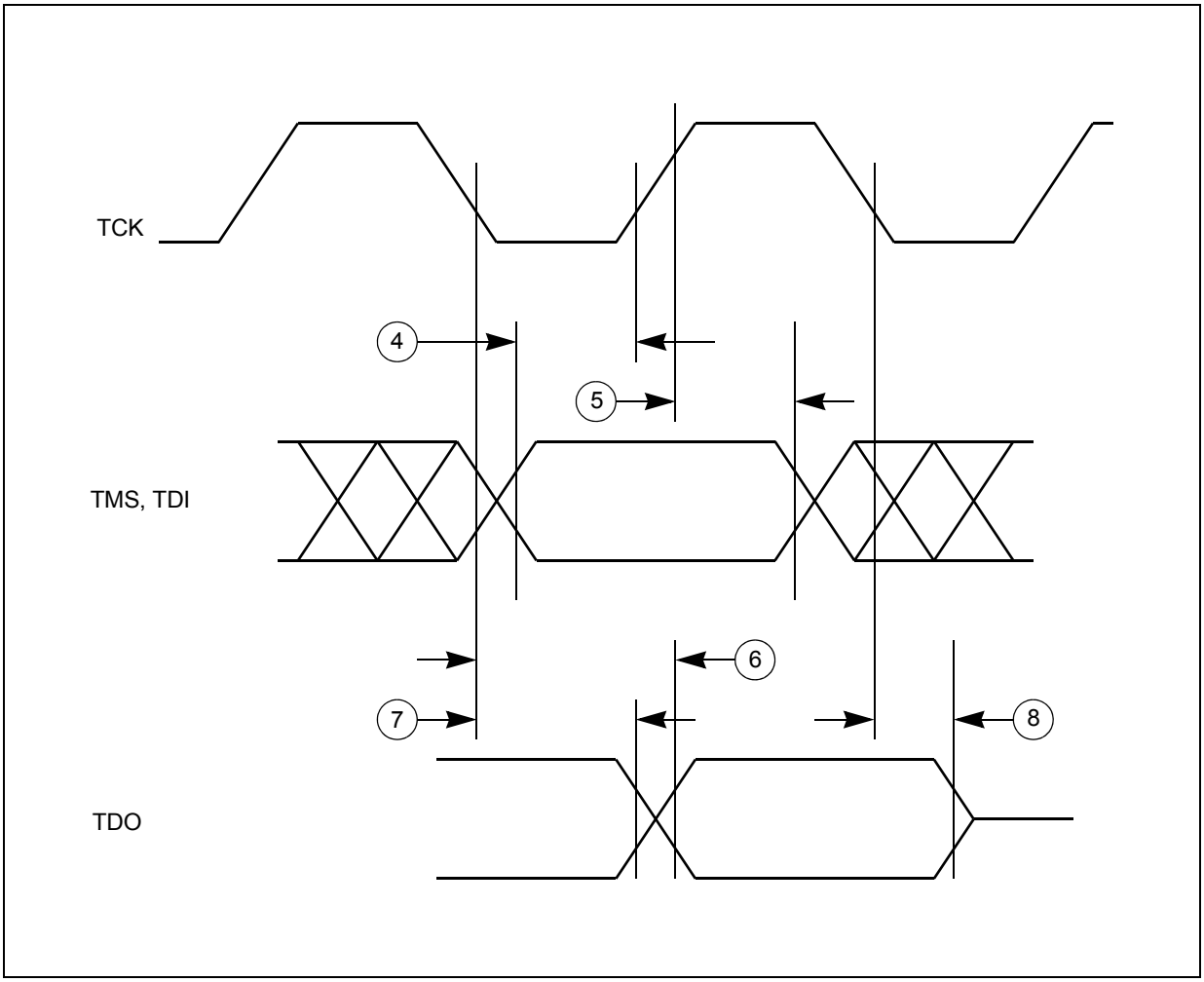


Table 41. DSPI timing[1] (continued)

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
12	t_{HO}	CC	D	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
					Slave	6	—	
					Master (MTFE = 1, CPHA = 0)	6	—	
					Master (MTFE = 1, CPHA = 1)	–2	—	

1. All timing are provided with 50pF capacitance on output, 1ns transition time on input signal

Figure 29. DSPI classic SPI timing — master, CPHA = 0

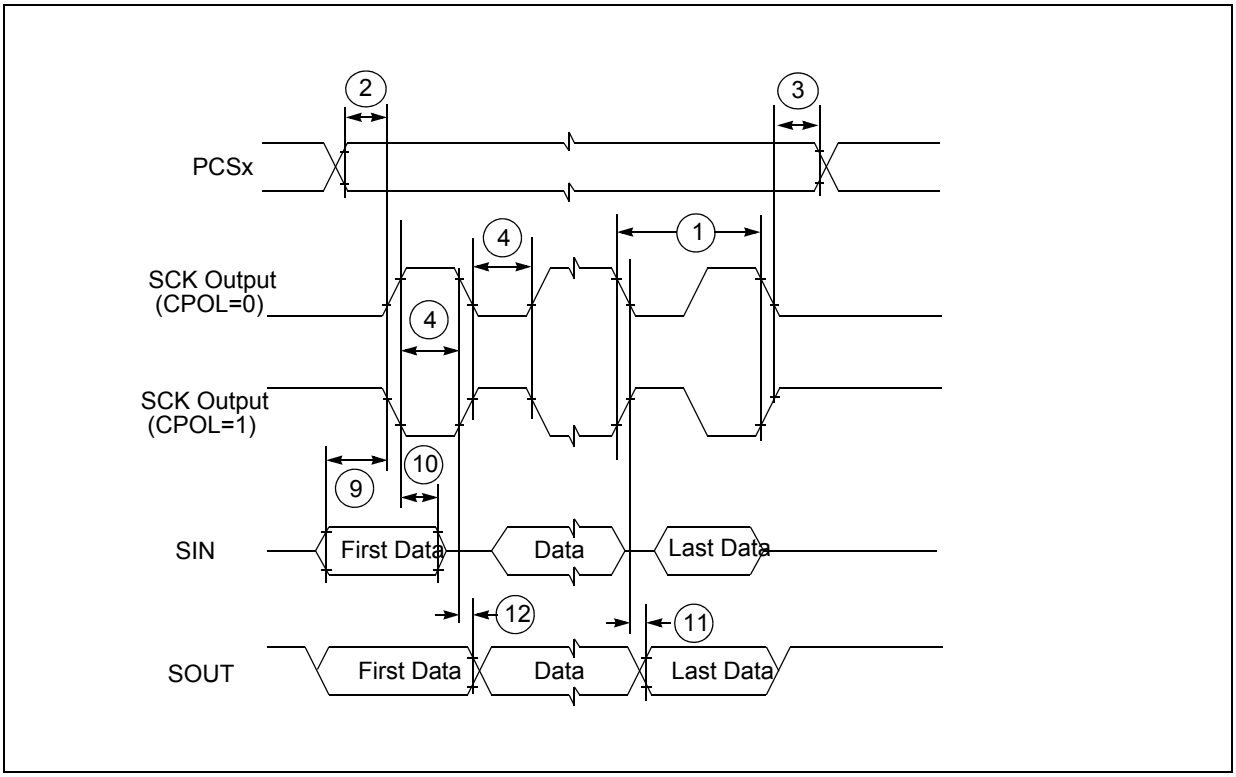


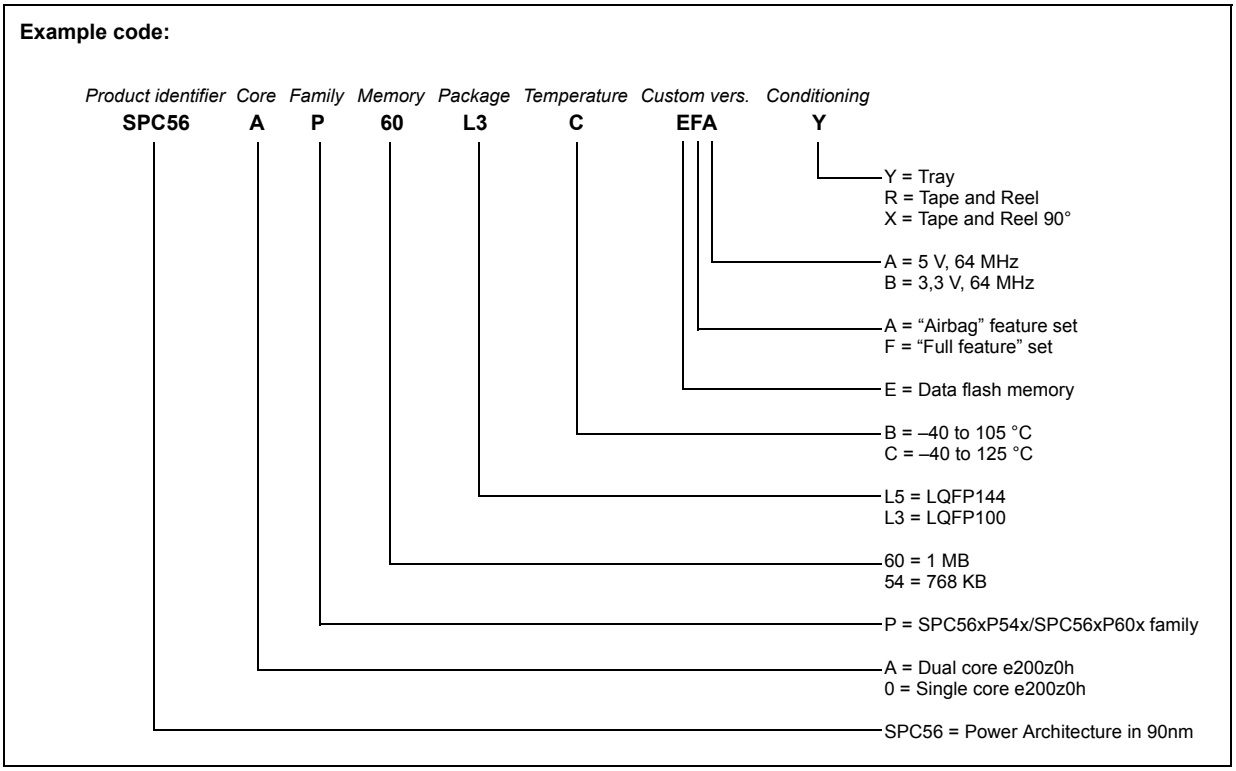
Table 42. LQFP144 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	—	17.500	—	—	0.6890	—
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	—	17.500	—	—	0.6890	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0°	3.5 °	0.0 °	7.0 °
ccc[2]	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Tolerance.

5 Ordering information

Figure 40. Ordering information scheme(h)



h. Not all configurations are available on the market. Please contact your ST sales representative to get the list of orderable commercial part number.

6 Revision history

Table 44 summarizes revisions to this document.

Table 44. Document revision history

Date	Revision	Substantive changes
21-Dec-2010	1	Initial release
18-Oct-2011	2	In the Feature list: Revised the first bullet. Changed “Up to 82 GPIO” to “Up to 80 GPIO” Changed “and 82 GPIO” to “and 49 GPIO” Changed “FlexRay module“ to “1 FlexRay™ module”. Added *Section 1.5: Feature details* *Table 4: SPC56xP54x/SPC56xP60x series block summary*, added FlexRay entry. In the “LQFP176 pinout (top view)” figure: – Pin 104 now is TDI, was PB[5] – Pin 107 now is TDO, was PB[4] – Pin 71 now is NC, was OKOUT – Pin 72 now is NC, was OKOUT_B – Pin 87 now is NC, was NBYPASS_HV – Pin 88 now is NC, was IPP_LIVI_B_VDDIO *Table 7: Pin muxing*: PB[6] was clk_out_div5, is now clk_out_div256 Removed PB[4] and PB[5] rows In the A[3] row, changed ABS[2] to ABS[1] *Section 3.11: DC electrical characteristics*, added “Peripherals supply current (5 V and 3.3 V)” table *Table 14: EMI testing specifications*, removed all references to SAE Replaced both *Table 12: Thermal characteristics for 144-pin LQFP* and *Table 13: Thermal characteristics for 100-pin LQFP* *Table 30: PLLMRFM electrical specifications (V_{DDPLL} = 1.08 V to 1.32 V, V_{SS} = V_{SSPLL} = 0 V, TA = TL to TH)*, changed the max value of f_{SYS} from 120 to 64 *Table 33: Program and erase specifications*: Removed all TBC changed the initial max value of T_{BKPRG} (Code Flash) from 3.3 to 6.6 s changed the max value of T_{BKPRG} (Data Flash) from 1.9 to 4.1 s changed the max value of $T_{wprogram}$ (Data Flash) from 300 to 500 µs Added t_{ESRT} row *Table 17: Voltage regulator electrical characteristics*, updated $V_{DD\_LV\_REGCOR}$ values Updated *Table 18: Low voltage monitor electrical characteristics* Updated *Table 21: Supply current (5.0 V, NVUSRO[PAD3V5V]=0)* and *Table 23: Supply current (3.3 V, NVUSRO[PAD3V5V]=1)* Removed “NVUSRO[OSCILLATOR_MARGIN] field description” section. Removed orderable parts tables.