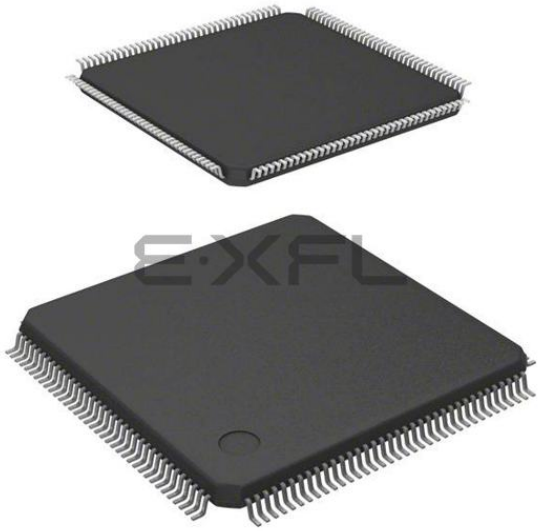

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 26x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p54l5ceaay

Table 2. SPC56xP54x/SPC56xP60x device comparison (continued)

Feature		SPC560P54	SPC560P60	SPC56AP54	SPC56AP60
Enhanced DMA (direct memory access) channels		16			
FlexRay		Yes (64 message buffer)			
FlexCAN (controller area network)		3(1),(2)			
Safety port		Yes (via third FlexCAN module)			
FCCU (fault collection and control unit)		Yes(3)			
CTU (cross triggering unit)		Yes			
eTimer channels		2 × 6			
FlexPWM (pulse-width modulation) channels		No			
Analog-to-digital converters (ADC)		One (10-bit, 27-channel)(4)			
LINFlex modules		2 (1 × Master/Slave, 1 × Master only)(5)			
DSPI (deserial serial peripheral interface) modules		5(6)			
CRC (cyclic redundancy check) units		2(7)			
JTAG interface		Yes			
Nexus port controller (NPC)		Yes (Level 2+)(8)			
Supply	Digital power supply(9)	3.3 V or 5 V single supply with external transistor			
	Analog power supply	3.3 V or 5 V			
	Internal RC oscillator	16 MHz			
	External crystal oscillator	4–40 MHz			
Packages		LQFP100 LQFP144			LQFP100 LQFP144 LQFP176(10)
Temperature	Standard ambient temperature	–40 to 125 °C			

1. Each FlexCAN module has 32 message buffers.
2. One FlexCAN module can act as a Safety Port with a bit rate as high as 7.5 Mbit/s.
3. Enhanced FCCU version.
4. Same amount of ADC channels as on SPC560P44/50 not considering the internally connected ones. 26 channels on LQFP144 and 16 channels on LQFP100.
5. LinFlex_1 is Master Only.
6. Increased number of CS for DSPI_1.
7. Upgraded specification with addition of 8-bits polynomial (CRC-8 VDA CAN) support and 3rd context.
8. Improved debugging capability with data trace capability and increased Nexus throughput available on emulation package.
9. 3.3 V range and 5 V range correspond to different orderable parts.
10. Software development package only. Not available for production.

1.5 Feature details

1.5.1 High performance e200z0h core processor

The e200z0h Power Architecture core provides the following features:

- High performance e200z0 core processor for managing peripherals and interrupts
- Single issue 4-stage pipeline in-order execution 32-bit Power Architecture CPU
- Harvard architecture
- Variable length encoding (VLE), allowing mixed 16-bit and 32-bit instructions
  - Results in smaller code size footprint
  - Minimizes impact on performance
- Branch processing acceleration using lookahead instruction buffer
- Load/store unit
  - 1-cycle load latency
  - Misaligned access support
  - No load-to-use pipeline bubbles
- Thirty-two 32-bit general purpose registers (GPRs)
- Separate instruction bus and load/store bus Harvard architecture
- Hardware vectored interrupt support
- Reservation instructions for implementing read-modify-write constructs
- Long cycle time instructions, except for guarded loads, do not increase interrupt latency
- Extensive system development support through Nexus debug port
- Non maskable Interrupt support

1.5.2 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between six master ports and six slave ports. The crossbar supports a 32-bit address bus width and a 32-bit data bus width.

The crossbar allows for two concurrent transactions to occur from any master port to any slave port; but one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grant it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters are treated with equal priority and will be granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

1.5.24 Analog-to-digital converter (ADC)

The ADC module provides the following features:

Analog part:

- 1 on-chip analog-to-digital converter
- 10-bit AD resolution
- 1 sample and hold unit per ADC
- Conversion time, including sampling time, less than 1 μs (at full precision)
- Typical sampling time is 150 ns min. (at full precision)
- Differential non-linearity error (DNL) ±1 LSB
- Integral non-linearity error (INL) ±1.5 LSB
- Total unadjusted error (TUE) <3 LSB
- Single-ended input signal range from 0 to 3.3 V / 5.0 V
- ADC and its reference can be supplied with a voltage independent from V_{DDIO}
- ADC supply can be equal or higher than V_{DDIO}
- ADC supply and the ADC reference are not independent from each other (they are internally bonded to the same pad)
- Sample times of 2 (default), 8, 64, or 128 ADC clock cycles

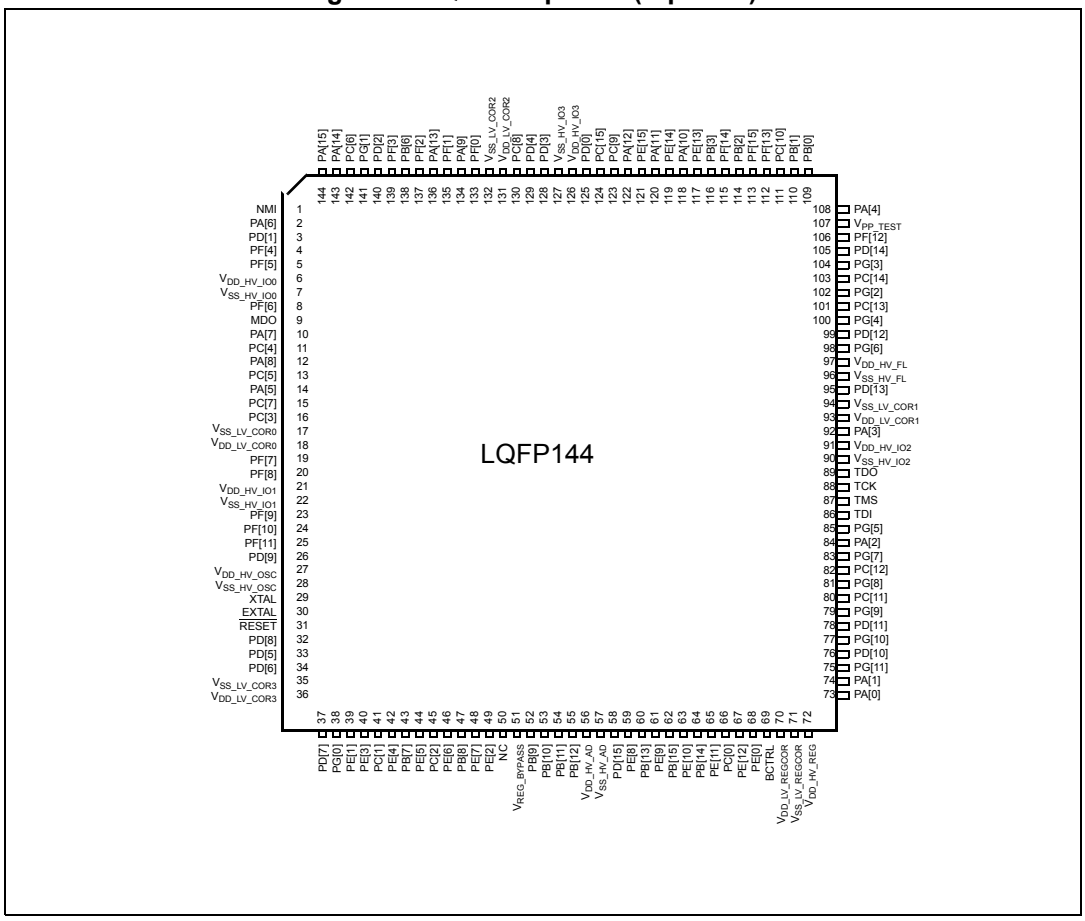
Digital part:

- 27 input channels (26 + 1 internally connected)
- 4 analog watchdogs to compare ADC results against predefined levels (low, high, range) before results are stored
- 2 operating modes: Normal mode and CTU control mode
- Normal mode features
  - Register-based interface with the CPU: control register, status register, 1 result register per channel
  - ADC state machine managing 3 request flows: regular command, hardware injected command, and software injected command
  - Selectable priority between software and hardware injected commands
  - DMA compatible interface
- CTU control mode features
  - Triggered mode only
  - 4 independent result queues (2 × 16 entries, 2 × 4 entries)
  - Result alignment circuitry (left justified; right justified)
  - 32-bit read mode allows to have channel ID on one of the 16-bit part
  - DMA compatible interfaces

1.5.25 Cross triggering unit (CTU)

The Cross Triggering Unit (CTU) allows automatic generation of ADC conversion requests on user selected conditions with minimized CPU load for dynamic configuration.

Figure 3. LQFP144 pinout (top view)(c)



c. Availability of port pin alternate functions depends on product selection.

2. LQFP176 available only as development package.
3. In this pin there is an internal pull; refer to JTAGC chapter in the device reference manual for pull direction.
4. Its configuration can be set up by the PCR[108] register inside the SIU module. See SIUL chapter in the device reference manual.

2.2.3 Pin muxing

Table 7 defines the pin list and muxing for the SPC56xP54x/SPC56xP60x devices relative to Full-featured version.

Each row of *Table 7* shows all the possible ways of configuring each pin, via “alternate functions”. The default function assigned to each pin after reset is the ALT0 function.

Pins marked as external interrupt capable can also be used to resume from STOP and HALT mode.

SPC56xP54x/SPC56xP60x devices provide four main I/O pad types depending on the associated functions:

- *Slow pads* are the most common, providing a compromise between transition time and low electromagnetic emission.
- *Medium pads* provide fast enough transition for serial communication channels with controlled current to reduce electromagnetic emission.
- *Fast pads* provide maximum speed. They are used for improved NEXUS debugging capability.
- *Symmetric pads* are designed to meet FlexRay requirements.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance.

Table 7. Pin muxing(1)

Port pin	PCR No.	Alternate function(2), (3)	Functions	Peripheral (4)	I/O direction (5)	Pad speed(6)		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176(7)
Port A										
A[0]	PCR[0]	ALT0 ALT1 ALT2 ALT3 —	GPIO[0] ETC[0] SCK_2 F[0] EIRQ[0]	SIUL eTimer_0 DSPI_2 FCCU SIUL	I/O I/O I/O O I	Slow	Medium	51	73	89
A[1]	PCR[1]	ALT0 ALT1 ALT2 ALT3 —	GPIO[1] ETC[1] SOUT_2 F[1] EIRQ[1]	SIUL eTimer_0 DSPI_2 FCCU SIUL	I/O I/O O O I	Slow	Medium	52	74	90

Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
A[2] [8]	PCR[2]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[2] ETC[2] CS3_4 — SIN_2 ABS[0] EIRQ[2]	SIUL eTimer_0 DSPI_4 — DSPI_2 MC_RGM SIUL	I/O I/O O — I I I	Slow	Medium	57	84	102
A[3] [8]	PCR[3]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[3] ETC[3] CS0_2 — ABS[1] EIRQ[3]	SIUL eTimer_0 DSPI_2 — MC_RGM SIUL	I/O I/O I/O — I I	Slow	Medium	64	92	116
A[4] [8]	PCR[4]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[4] ETC[0] CS1_2 ETC[4] FAB EIRQ[4]	SIUL eTimer_1 DSPI_2 eTimer_0 MC_RGM SIUL	I/O I/O O I/O I I	Slow	Medium	75	108	132
A[5]	PCR[5]	ALT0 ALT1 ALT2 ALT3 —	GPIO[5] CS0_1 ETC[5] CS7_0 EIRQ[5]	SIUL DSPI_1 eTimer_1 DSPI_0 SIUL	I/O I/O I/O O I	Slow	Medium	8	14	22
A[6]	PCR[6]	ALT0 ALT1 ALT2 ALT3 —	GPIO[6] SCK_1 CS2_4 — EIRQ[6]	SIUL DSPI_1 DSPI_4 — SIUL	I/O I/O I/O — I	Slow	Medium	2	2	2
A[7]	PCR[7]	ALT0 ALT1 ALT2 ALT3 —	GPIO[7] SOUT_1 CS1_4 — EIRQ[7]	SIUL DSPI_1 DSPI_4 — SIUL	I/O O I/O — I	Slow	Medium	4	10	18
A[8]	PCR[8]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[8] — CS0_4 — SIN_1 EIRQ[8]	SIUL — DSPI_4 — DSPI_1 SIUL	I/O — I/O — I I	Slow	Medium	6	12	20

3.3 Absolute maximum ratings

Table 9. Absolute maximum ratings(1)

Symbol		Parameter	Conditions	Min	Max(2)	Unit
V_{SS_HV}	SR	Digital ground	—	0	0	V
$V_{DD\_HV\_IOx}$(3)	SR	3.3 V / 5.0 V input/output supply voltage with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
$V_{DD\_HV\_FL}$	SR	3.3 V / 5.0 V code and data flash memory supply voltage with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3	
$V_{SS\_HV\_FL}$	SR	Code and data flash memory ground with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
$V_{DD\_HV\_OSC}$	SR	3.3 V / 5.0 V crystal oscillator amplifier supply voltage with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3	
$V_{SS\_HV\_OSC}$	SR	3.3 V / 5.0 V crystal oscillator amplifier reference voltage with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
$V_{DD\_HV\_REG}$	SR	3.3 V / 5.0 V voltage regulator supply voltage with respect to ground (V_{SS_HV})	—	– 0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	– 0.3	$V_{DD\_HV\_IOx}$ + 0.3	
$V_{DD\_HV\_AD}$	SR	3.3 V / 5.0 V ADC supply and high reference voltage with respect to ground (V_{SS_HV})	$V_{DD\_HV\_REG}$ < 2.7 V	– 0.3	$V_{DD\_HV\_REG}$ + 0.3	V
			$V_{DD\_HV\_REG}$ > 2.7 V	– 0.3	6.0	
$V_{SS\_HV\_AD}$	SR	ADC ground and low reference voltage with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
TV_{DD}	SR	Slope characteristics on all V_{DD} during power up(4) with respect to ground (V_{SS_HV})	—	3.0(5)	500 x 10^3 (0.5 [V/µs])	V/s
V_{IN}	SR	Voltage on any pin with respect to ground ($V_{SS\_HV\_IOx}$) with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3	
V_{INAN}	SR	Analog input voltage	$V_{DD\_HV\_REG}$ < 2.7 V	$V_{SS\_HV\_AD}$ – 0.3	$V_{DD\_HV\_AD}$ + 0.3	V
			$V_{DD\_HV\_REG}$ > 2.7 V	$V_{SS\_HV\_AD}$	$V_{DD\_HV\_AD}$	V
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA

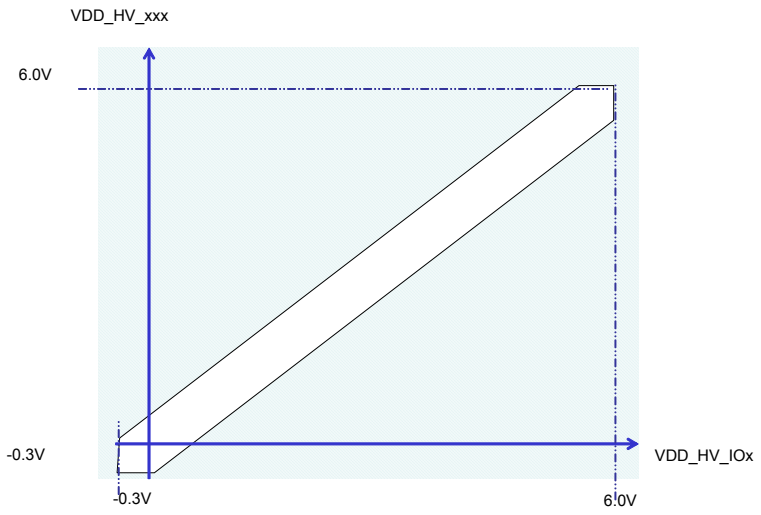
Table 9. Absolute maximum ratings(1) (continued)

Symbol		Parameter	Conditions	Min	Max(2)	Unit
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
I_{VDD_LV}	SR	Low voltage static current sink through V_{DD_LV}	—	—	155	mA
T_{STG}	SR	Storage temperature	—	–55	150	°C
T_J	SR	Junction temperature under bias	—	–40	150	°C

1. Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.
3. The difference between each couple of voltage supplies must be less than 300 mV, $|V_{DD\_HV\_IOy} - V_{DD\_HV\_IOx}| < 300$ mV.
4. Guaranteed by device validation.
5. Minimum value of TV_{DD} must be guaranteed until $V_{DD\_HV\_REG}$ reaches 2.6 V (maximum value of V_{PORH}).

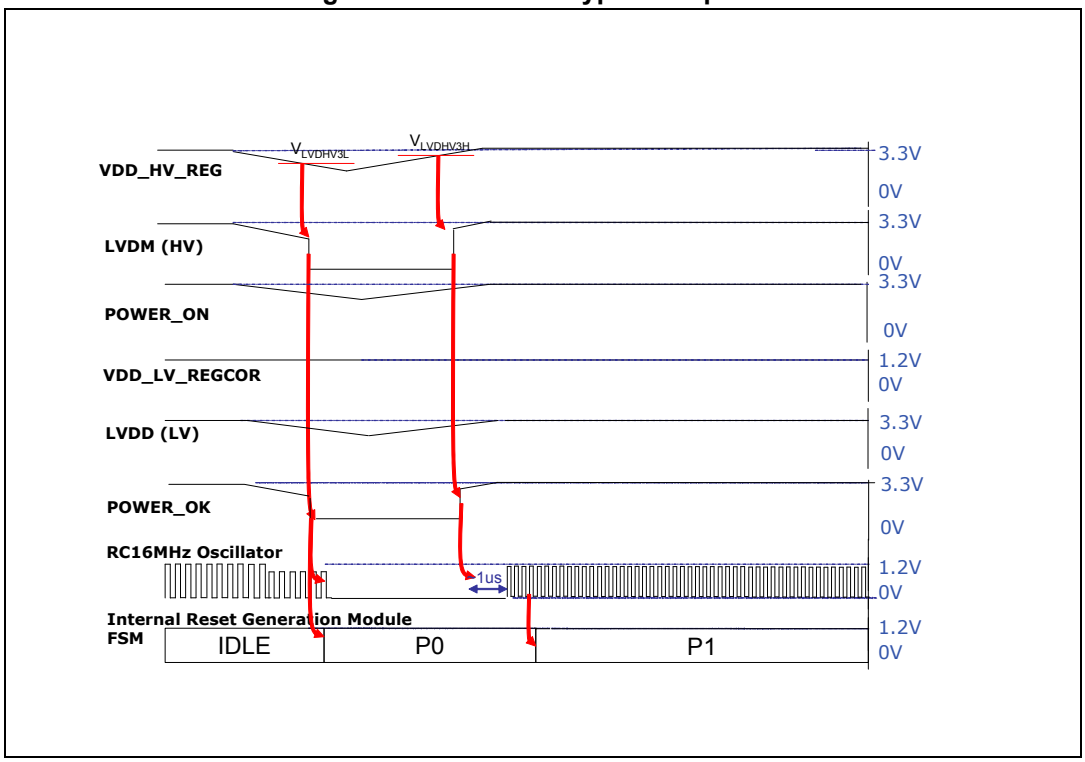
Figure 5 shows the constraints of the different power supplies.

Figure 5. Power supplies constraints



The SPC56xP54x/SPC56xP60x supply architecture provides an ADC supply that is managed independently of standard V_{DD_HV} supply. *Figure 6* shows the constraints of the ADC power supply.

Figure 12. Brown-out typical sequence



3.10 NVUSRO register

Portions of the device configuration, such as high voltage supply, and watchdog enable/disable after reset are controlled via bit values in the non-volatile user options register (NVUSRO) register.

For a detailed description of the NVUSRO register, please refer to the device reference manual.

3.10.1 NVUSRO[PAD3V5V] field description

Table 19 shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 19. PAD3V5V field description(1)

Value(2)	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1. See the device reference manual for more information on the NVUSRO register.
2. '1' is delivery value. It is part of shadow Flash, thus programmable by customer.

The DC electrical characteristics are dependent on the PAD3V5V bit value.

3.11.2 DC electrical characteristics (3.3 V)

Table 22 gives the DC electrical characteristics at 3.3 V (3.0 V < $V_{DD\_HV\_IOx}$ < 3.6 V, NVUSRO[PAD3V5V]=1) as described in *Figure 14*.

Figure 14. I/O input DC electrical characteristics definition

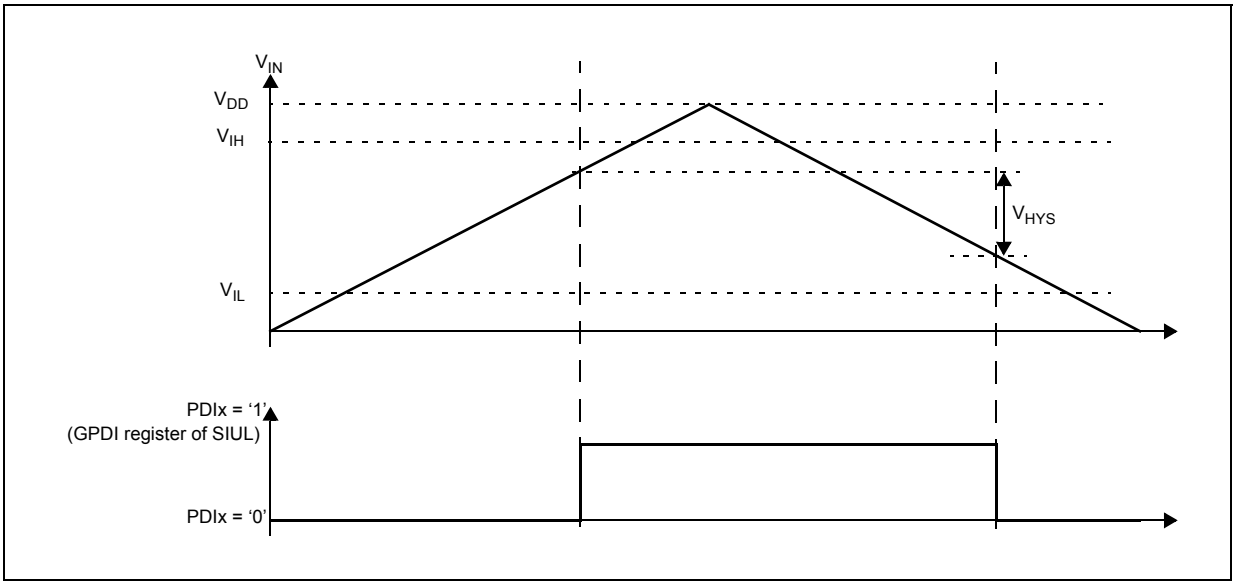


Table 22. DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V]=1)(1)

Symbol		Parameter	Conditions	Min	Max	Unit
V_{IL}	D	Minimum low level input voltage	—	–0.1(2)	—	V
V_{IL}	P	Maximum low level input voltage	—	—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IH}	P	Minimum high level input voltage	—	0.65 $V_{DD\_HV\_IOx}$	—	V
V_{IH}	D	Maximum high level input voltage	—	—	$V_{DD\_HV\_IOx}$ + 0.1(2)	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IOx}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 2 mA	—	0.5	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –2 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_F}	P	Fast, high level output voltage	I_{OL} = 11 mA	—	0.5	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –11 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_SYM}	P	Symmetric, high level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_SYM}	P	Symmetric, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
I_{PU}	P	Equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	

2. “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self clocked mode.
3. Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.
4. f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.
5. This value is determined by the crystal manufacturer and board design.
6. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.
7. Proper PC board layout procedures must be followed to achieve specifications.
8. Values are obtained with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).
9. Short term jitter is measured on the clock rising edge at cycle n and cycle n+4.
10. This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this PLL, load capacitors should not exceed these limits.
11. This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
12. This value is true when operating at frequencies above 60 MHz, otherwise f_{CS} is 2% (above 64 MHz).
13. Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

3.14 16 MHz RC oscillator electrical characteristics

Table 31. 16 MHz RC oscillator electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
f_{RC}	P	RC oscillator frequency	T_A = 25 °C	—	16	—	MHz
Δ_{RCMVAR}	P	Fast internal RC oscillator variation over temperature and supply with respect to f_{RC} at T_A = 25 °C in high-frequency configuration	—	–6	—	6	%
$\Delta_{RCMTRIM}$	T	Post Trim Accuracy: The variation of the PTF(1) from the 16 MHz	T_A = 25 °C	–1	—	1	%
$\Delta_{RCMSTEP}$	T	Fast internal RC oscillator trimming step	T_A = 25 °C	—	1.6	—	%

1. PTF = Post Trimming Frequency: The frequency of the output clock after trimming at typical supply voltage and temperature

3.15 Analog-to-Digital converter (ADC) electrical characteristics

The device provides a 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

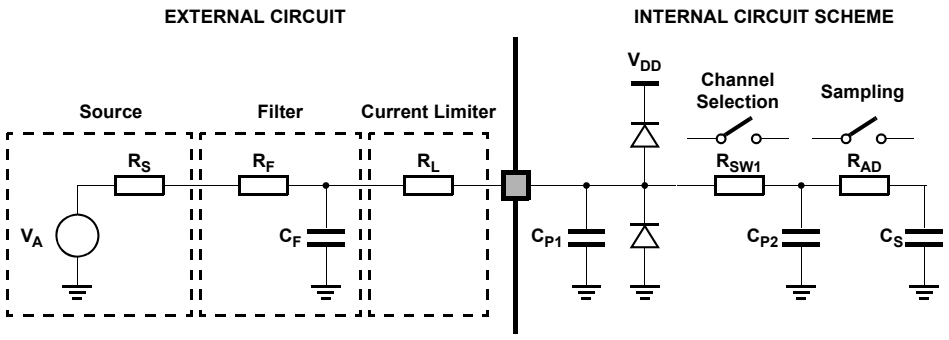
In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: being C_S and C_{P2} substantially two switched capacitances, with a frequency equal to the ADC conversion rate, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with $C_S + C_{P2}$ equal to 3 pF, a resistance of 330 kΩ is obtained ($R_{EQ} = 1 / (fc \times (C_S + C_{P2}))$, where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on $C_S + C_{P2}$) and the sum of $R_S + R_F$, the external circuit must be designed to respect the *Equation 4*:

Equation 4

$$V_A \times \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 4 generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

Figure 16. Input equivalent circuit (precise channels)



R_S Source Impedance

R_F Filter Resistance

C_F Filter Capacitance

R_L Current Limiter Resistance

R_{SW1} Channel Selection Switch Impedance

R_{AD}Sampling Switch Impedance

C_P Pin Capacitance (two contributions, C_{P1} and C_{P2})

3.17 AC specifications

3.17.1 Pad AC specifications

Table 36. Output pin transition times

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
T_{tr}	CC	D	Output transition time output pin[2] SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
		T		C_L = 50 pF		—	—	50	
		D		C_L = 100 pF		—	—	75	
T_{tr}	CC	D	Output transition time output pin[2] MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	
T_{tr}	CC	D	Output transition time output pin[2] FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	4	ns
				C_L = 50 pF		—	—	6	
				C_L = 100 pF		—	—	12	
				C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	4	
				C_L = 50 pF		—	—	7	
				C_L = 100 pF		—	—	12	
T_{sim}[3]	CC	T	Symmetric, same drive strength between N and P transistor	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	4	ns
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified.
2. C_L includes device and package capacitances (C_{PKG} < 5 pF).
3. Transition timing of both positive and negative slopes will differ maximum 50 %.

3.18 AC timing characteristics

3.18.1 $\overline{\text{RESET}}$ pin characteristics

The SPC56xP54x/SPC56xP60x implements a dedicated bidirectional RESET pin.

Figure 20. Start-up reset requirements(g)

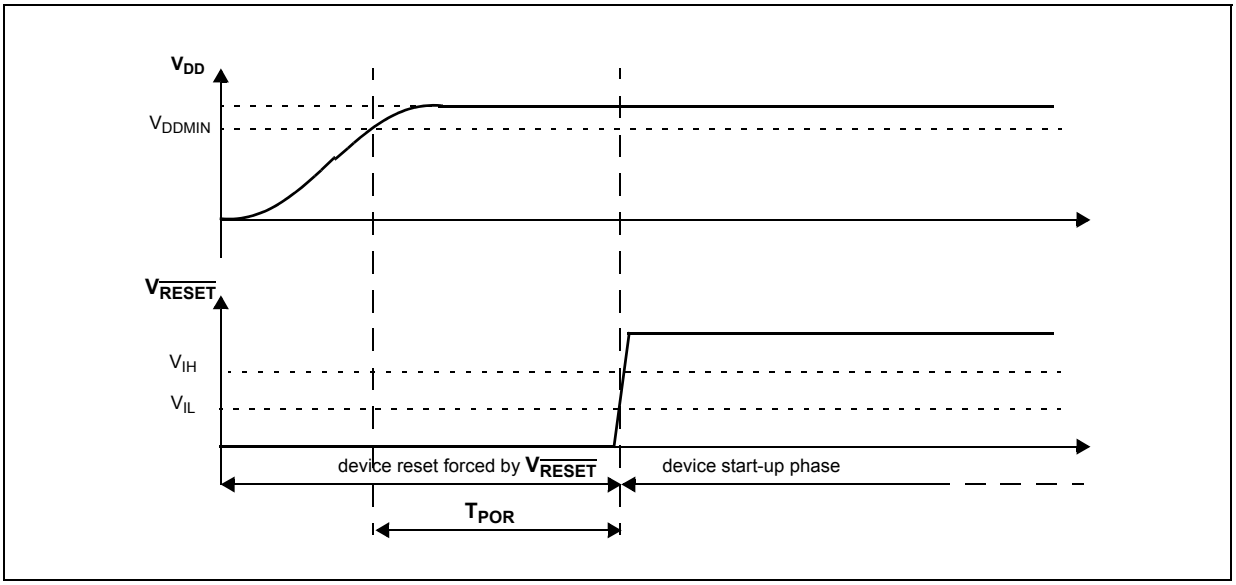
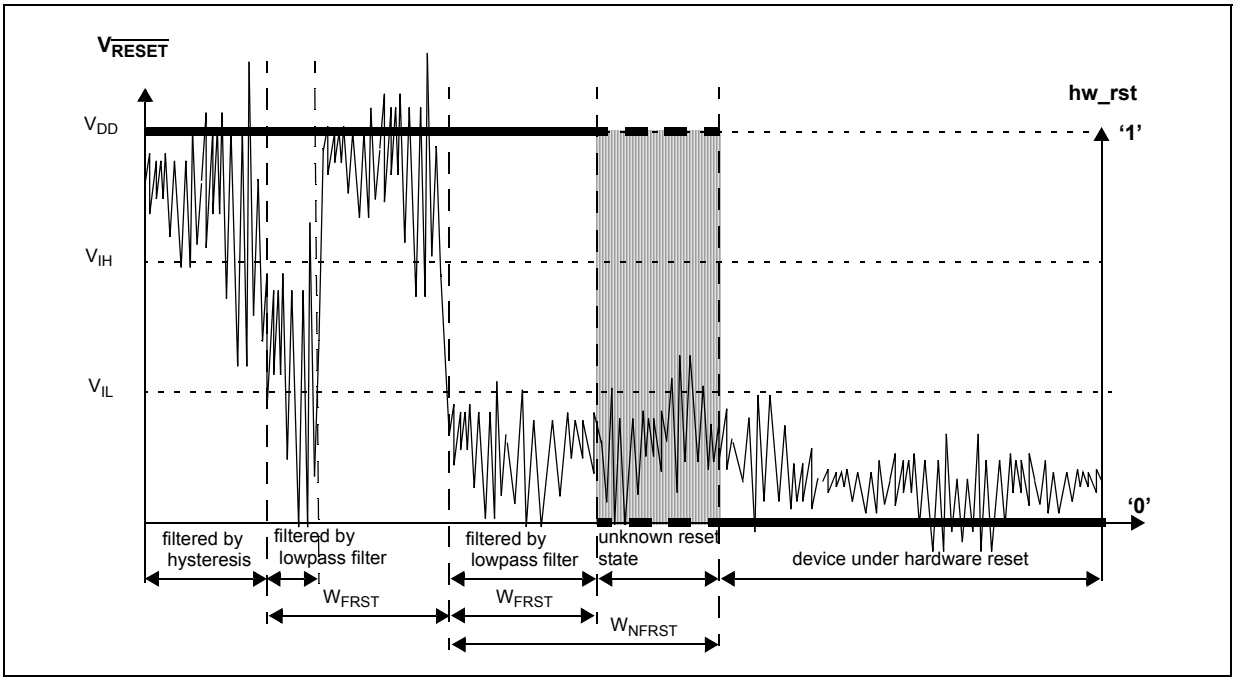


Figure 21. Noise filtering on reset signal



g. The output drive provided is open drain and hence must be terminated by an external resistor of value 1 kΩ.

Table 37. $\overline{\text{RESET}}$ electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input High Level CMOS (Schmitt Trigger)	—	$0.65V_{DD}$	—	$V_{DD}+0.4$	V
V_{IL}	SR	P	Input low Level CMOS (Schmitt Trigger)	—	–0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	$0.1V_{DD}$	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 2mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
				Push Pull, I_{OL} = 1mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
				Push Pull, I_{OL} = 1mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
T_{tr}	CC	D	Output transition time output pin[3] MEDIUM configuration	C_L = 25pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
				C_L = 50pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
				C_L = 100pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
				C_L = 25pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
				C_L = 50pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
				C_L = 100pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W_{FRST}	SR	P	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ input not filtered pulse	—	500	—	—	ns
T_{POR}	CC	D	maximum delay before internal reset is released after all VDD_HV reach nominal supply	Monotonic VDD_HV supply ramp	—	—	1	ms
$\lvert I_{WPU}\rvert$	CC	P	Weak pull-up current absolute value	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	10	—	150	µA
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	10	—	150	
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[4]	10	—	250	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified.
2. This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of device reference manual).
3. C_L includes device and package capacitance (C_{PKG} < 5 pF).
4. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Figure 30. DSPI classic SPI timing — master, CPHA = 1

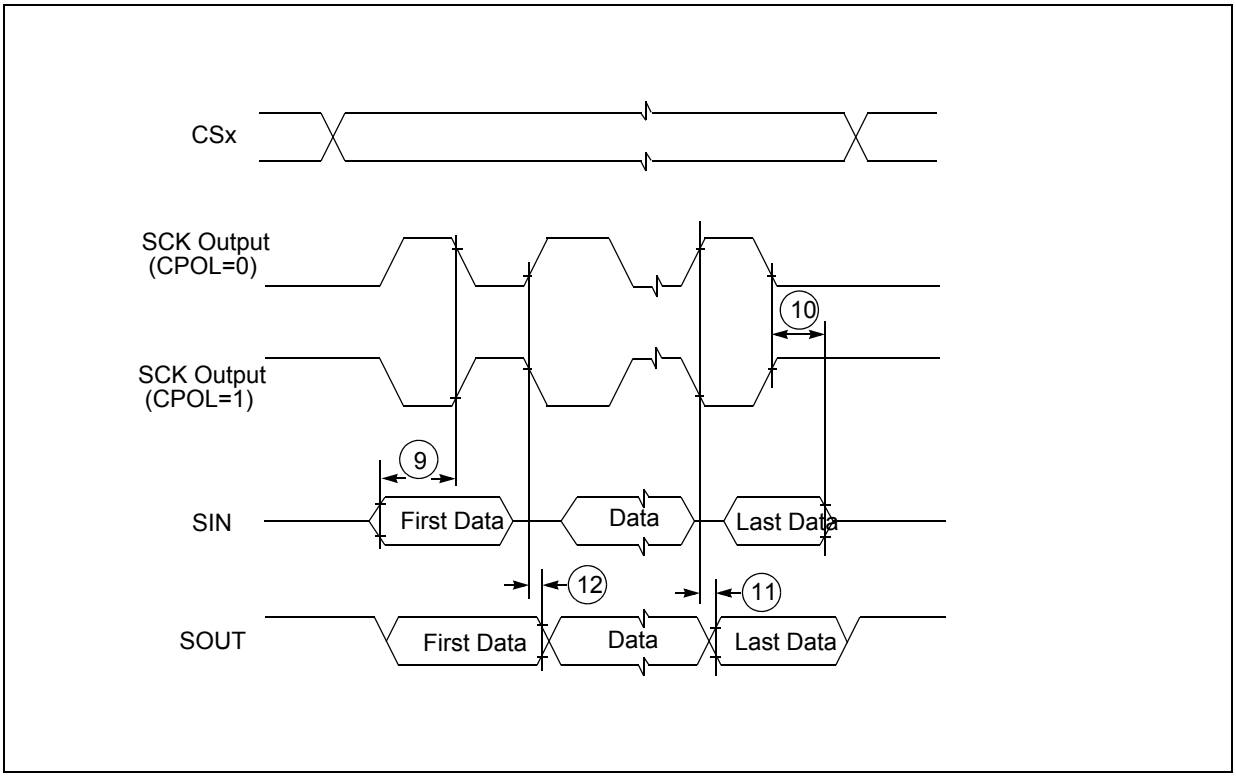


Figure 31. DSPI classic SPI timing — slave, CPHA = 0

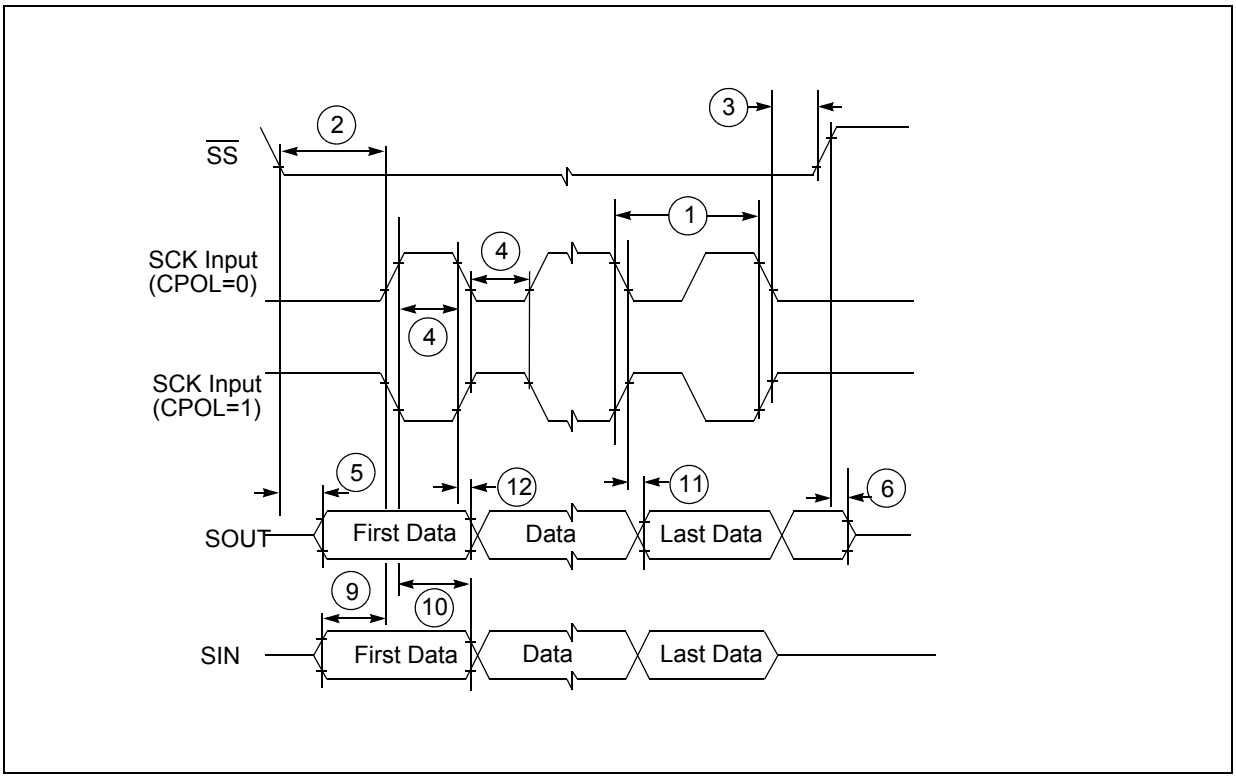


Figure 36. DSPI modified transfer format timing — slave, CPHA = 1

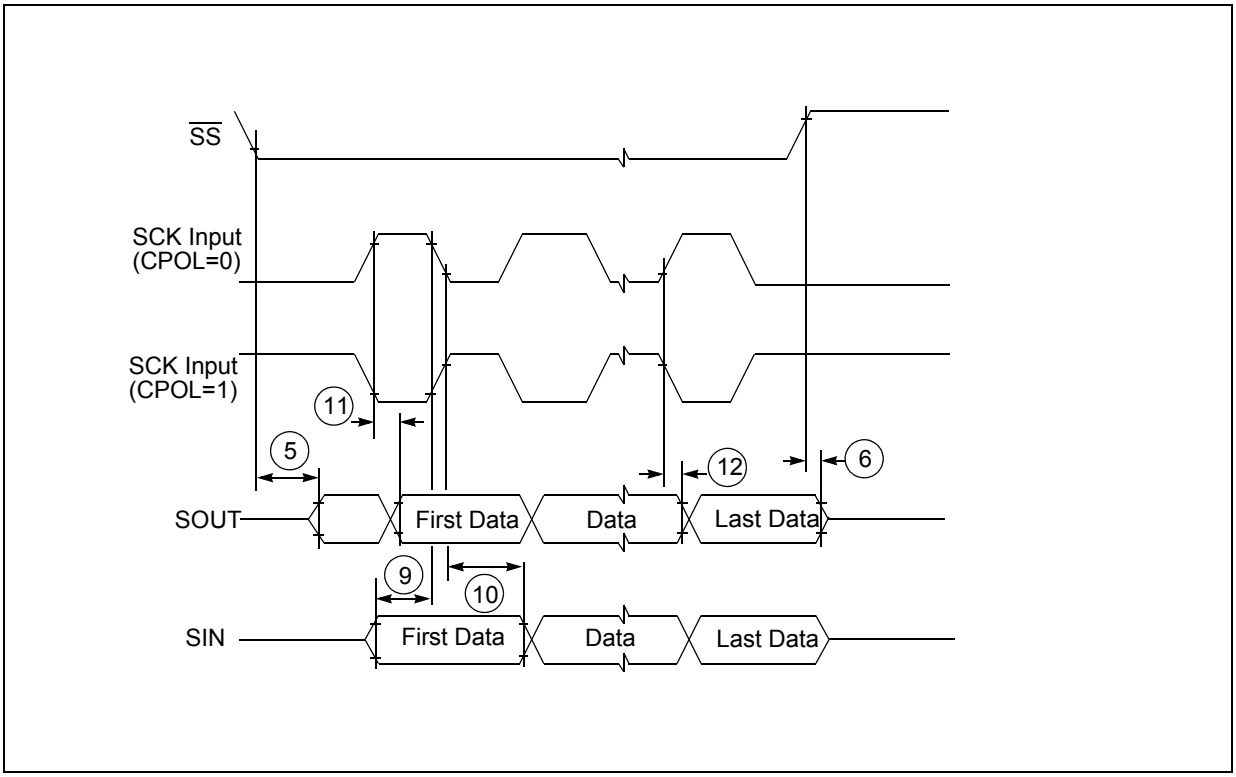
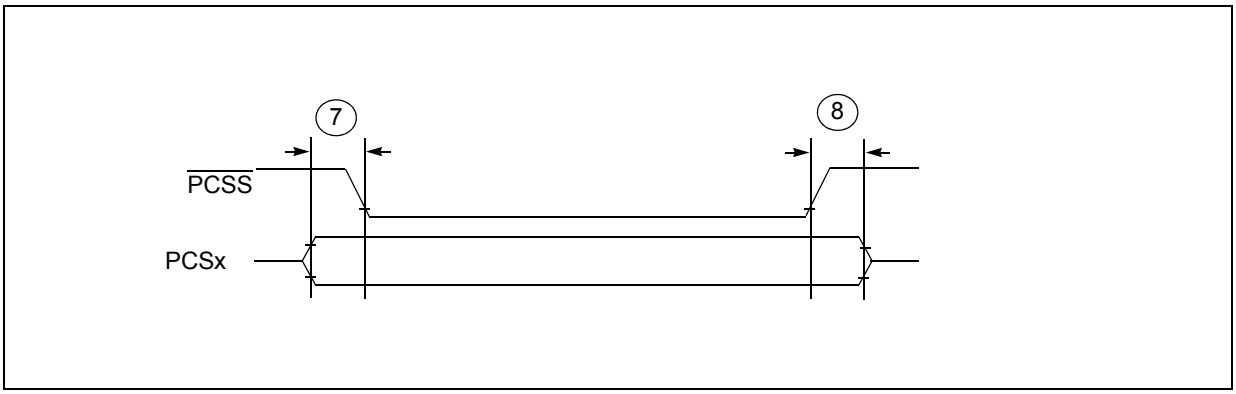


Figure 37. DSPI PCS strobe (PCSS) timing



4.2.2 LQFP100 mechanical outline drawing

Figure 39. LQFP100 package mechanical drawing

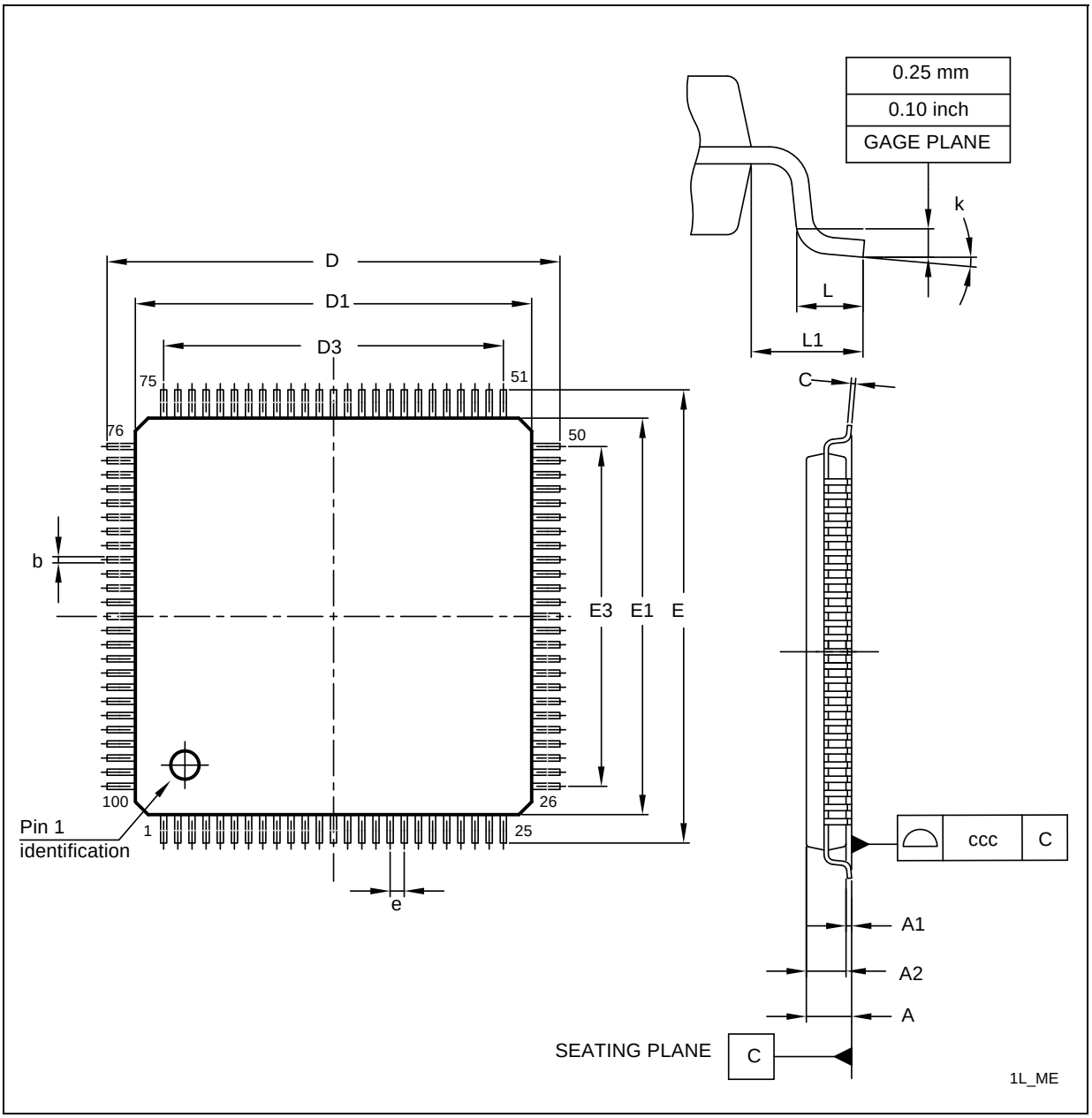


Table 43. LQFP100 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571

Table 43. LQFP100 mechanical data (continued)

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	—	12.000	—	—	0.4724	—
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	—	12.000	—	—	0.4724	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0 °	0.0 °	3.5 °	7.0 °
ccc[2]	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Tolerance.