STMicroelectronics - SPC560P54L5CEFAY Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 26x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p54l5cefay

allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

The INTC provides the following features:

- Unique 9-bit vector for each separate interrupt source
- 8 software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority.
  - Modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources.
- 2 external high priority interrupts directly accessing the main core and IOP critical interrupt mechanism

The INTC module is replicated for each processor.

1.5.7 System clocks and clock generation

The following list summarizes the system clock and clock generation on the SPC56xP54x/SPC56xP60x:

- Lock detect circuitry continuously monitors lock status
- Loss of clock (LOC) detection for PLL outputs
- Programmable output clock divider (÷1, ÷2, ÷4, ÷8)
- Programmable output clock divider (÷1, ÷2, ÷3 to ÷256)
- eTimer module running at the same frequency as the e200z0h core
- On-chip oscillator with automatic level control
- Internal 16 MHz RC oscillator for rapid start-up and safe mode
  - Supports frequency trimming by user application

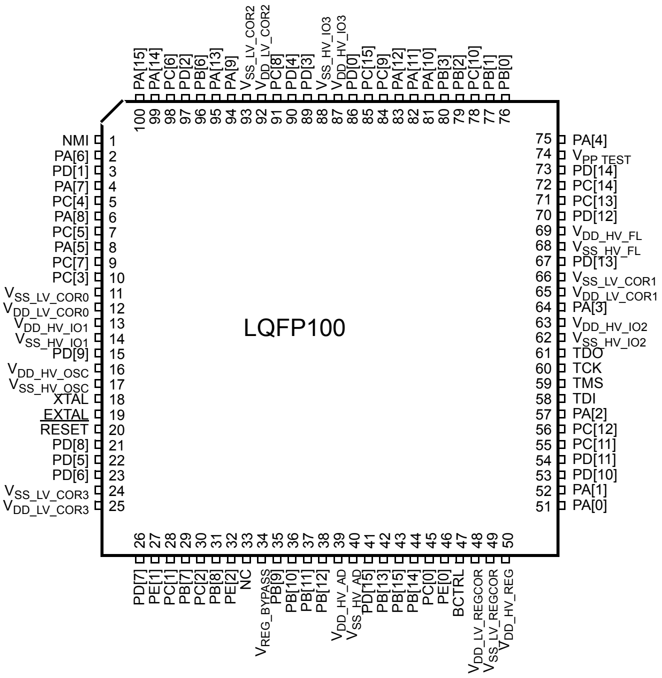
1.5.8 Frequency modulated phase-locked loop (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 40 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The FMPLL multiplication factor, output clock divider ratio are all software configurable.

The FMPLL has the following major features:

- Input clock frequency from 4 MHz to 40 MHz
- Voltage controlled oscillator (VCO) range from 256 MHz to 512 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- Modulation enabled/disabled through software

Figure 4. LQFP100 pinout (top view)[d]



2.2 Pin descriptions

The following sections provide signal descriptions and related information about the functionality and configuration of the SPC56xP54x/SPC56xP60x devices.

2.2.1 Power supply and reference voltage pins

Table 5 lists the power supply and reference voltage for the SPC56xP54x/SPC56xP60x devices.

Table 5. Supply pins

Supply		Pin		
Symbol	Description	LQFP 100	LQFP 144	LQFP 176(1)
VREG control and power supply pins				
BCTRL	Voltage regulator external NPN Ballast base control pin	47	69	81

d. Availability of port pin alternate functions depends on product selection.

Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
B[9]	PCR[25]	ALT0 ALT1 ALT2 ALT3 —	GPIO[25] — — — AN[11]	SIUL — — — ADC_0	Input Only	—	—	35	52	60
B[10]	PCR[26]	ALT0 ALT1 ALT2 ALT3 —	GPIO[26] — — — AN[12]	SIUL — — — ADC_0	Input Only	—	—	36	53	61
B[11]	PCR[27]	ALT0 ALT1 ALT2 ALT3 —	GPIO[27] — — — AN[13]	SIUL — — — ADC_0	Input Only	—	—	37	54	62
B[12]	PCR[28]	ALT0 ALT1 ALT2 ALT3 —	GPIO[28] — — — AN[14]	SIUL — — — ADC_0	Input Only	—	—	38	55	63
B[13]	PCR[29]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[29] — — — AN[16] RXD	SIUL — — — ADC_0 LINFlex_1	Input Only	—	—	42	60	68
B[14]	PCR[30]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[30] — — — AN[17] ETC[4] EIRQ[19]	SIUL — — — ADC_0 eTimer_0 SIUL	Input Only	—	—	44	64	76
B[15]	PCR[31]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[31] — — — AN[18] EIRQ[20]	SIUL — — — ADC_0 SIUL	Input Only	—	—	43	62	70

Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
Port C										
C[0]	PCR[32]	ALT0 ALT1 ALT2 ALT3 —	GPIO[32] — — — AN[19]	SIUL — — — ADC_0	Input Only	—	—	45	66	78
C[1]	PCR[33]	ALT0 ALT1 ALT2 ALT3 —	GPIO[33] — — — AN[2]	SIUL — — — ADC_0	Input Only	—	—	28	41	49
C[2]	PCR[34]	ALT0 ALT1 ALT2 ALT3 —	GPIO[34] — — — AN[3]	SIUL — — — ADC_0	Input Only	—	—	30	45	53
C[3]	PCR[35]	ALT0 ALT1 ALT2 ALT3 —	GPIO[35] CS1_0 ETC[4] TXD EIRQ[21]	SIUL DSPI_0 eTimer_1 LINFlex_1 SIUL	I/O O I/O O I	Slow	Medium	10	16	24
C[4]	PCR[36]	ALT0 ALT1 ALT2 ALT3 —	GPIO[36] CS0_0 — DEBUG[4] EIRQ[22]	SIUL DSPI_0 — SSCM SIUL	I/O I/O — — I	Slow	Medium	5	11	19
C[5]	PCR[37]	ALT0 ALT1 ALT2 ALT3 —	GPIO[37] SCK_0 SCK_4 DEBUG[5] EIRQ[23]	SIUL DSPI_0 DSPI_4 SSCM SIUL	I/O I/O I/O — I	Slow	Medium	7	13	21
C[6]	PCR[38]	ALT0 ALT1 ALT2 ALT3 —	GPIO[38] SOUT_0 — DEBUG[6] EIRQ[24]	SIUL DSPI_0 — SSCM SIUL	I/O O — — I	Slow	Medium	98	142	174

Table 7. Pin muxing[(1)] (continued)

Port pin	PCR No.	Alternate function[(2),(3)]	Functions	Peripheral[(4)]	I/O direction[(5)]	Pad speed[(6)]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[(7)]
C[15]	PCR[47]	ALT0 ALT1 ALT2 ALT3 —	GPIO[47] CA_TR_EN ETC[0] — EXT_IN	SIUL FlexRay_0 eTimer_1 — CTU_0	I/O O I/O — I	Slow	Symmetric	85	124	148
Port D										
D[0]	PCR[48]	ALT0 ALT1 ALT2 ALT3	GPIO[48] CA_TX ETC[1] —	SIUL FlexRay_0 eTimer_1 —	I/O O I/O —	Slow	Symmetric	86	125	149
D[1]	PCR[49]	ALT0 ALT1 ALT2 ALT3 —	GPIO[49] CS4_1 ETC[2] EXT_TRG CA_RX	SIUL DSPI_1 eTimer_1 CTU_0 FlexRay_0	I/O O I/O O I	Slow	Medium	3	3	3
D[2]	PCR[50]	ALT0 ALT1 ALT2 ALT3 —	GPIO[50] CS5_1 ETC[3] — CB_RX	SIUL DSPI_1 eTimer_1 — FlexRay_0	I/O O I/O — I	Slow	Medium	97	140	168
D[3]	PCR[51]	ALT0 ALT1 ALT2 ALT3	GPIO[51] CB_TX ETC[4] —	SIUL FlexRay_0 eTimer_1 —	I/O O I/O —	Slow	Symmetric	89	128	152
D[4]	PCR[52]	ALT0 ALT1 ALT2 ALT3	GPIO[52] CB_TR_EN ETC[5] —	SIUL FlexRay_0 eTimer_1 —	I/O O I/O —	Slow	Symmetric	90	129	153
D[5]	PCR[53]	ALT0 ALT1 ALT2 ALT3	GPIO[53] CS3_0 — SOUT_3	SIUL DSPI_0 — DSPI_3	I/O O — O	Slow	Medium	22	33	41
D[6]	PCR[54]	ALT0 ALT1 ALT2 ALT3	GPIO[54] CS2_0 SCK_3 SOUT_4	SIUL DSPI_0 DSPI_3 DSPI_4	I/O O I/O O	Slow	Medium	23	34	42

Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
D[7]	PCR[55]	ALT0 ALT1 ALT2 ALT3 —	GPIO[55] CS3_1 — CS4_0 SIN_3	SIUL DSPI_1 — DSPI_0 DSPI_3	I/O O — O I	Slow	Medium	26	37	45
D[8]	PCR[56]	ALT0 ALT1 ALT2 ALT3	GPIO[56] CS2_1 RDY CS5_0	SIUL DSPI_1 nexus_0 DSPI_0	I/O O O O	Slow	Medium	21	32	40
D[9]	PCR[57]	ALT0 ALT1 ALT2 ALT3	GPIO[57] — TXD CS6_1	SIUL — LINFlex_1 DSPI_1	I/O — O O	Slow	Medium	15	26	34
D[10]	PCR[58]	ALT0 ALT1 ALT2 ALT3	GPIO[58] — CS0_3 —	SIUL — DSPI_3 —	I/O — I/O —	Slow	Medium	53	76	92
D[11]	PCR[59]	ALT0 ALT1 ALT2 ALT3	GPIO[59] — CS1_3 SCK_3	SIUL — DSPI_3 DSPI_3	I/O — O I/O	Slow	Medium	54	78	94
D[12]	PCR[60]	ALT0 ALT1 ALT2 ALT3 —	GPIO[60] — — CS7_1 RXD	SIUL — — DSPI_1 LINFlex_1	I/O — — O I	Slow	Medium	70	99	123
D[13]	PCR[61]	ALT0 ALT1 ALT2 ALT3	GPIO[61] — CS2_3 SOUT_3	SIUL — DSPI_3 DSPI_3	I/O — O O	Slow	Medium	67	95	119
D[14]	PCR[62]	ALT0 ALT1 ALT2 ALT3 —	GPIO[62] — CS3_3 — SIN_3	SIUL — DSPI_3 — DSPI_3	I/O — O — I	Slow	Medium	73	105	129
D[15]	PCR[63]	ALT0 ALT1 ALT2 ALT3 —	GPIO[63] — — — AN[20]	SIUL — — — ADC_0	Input Only	—	—	41	58	66

Table 7. Pin muxing(1) (continued)

Port pin	PCR No.	Alternate function(2), (3)	Functions	Peripheral (4)	I/O direction (5)	Pad speed(6)		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176(7)
Port E										
E[0]	PCR[64]	ALT0 ALT1 ALT2 ALT3 —	GPIO[64] — — — AN[21]	SIUL — — — ADC_0	Input Only	—	—	46	68	80
E[1]	PCR[65]	ALT0 ALT1 ALT2 ALT3 —	GPIO[65] — — — AN[4]	SIUL — — — ADC_0	Input Only	—	—	27	39	47
E[2]	PCR[66]	ALT0 ALT1 ALT2 ALT3 —	GPIO[66] — — — AN[5]	SIUL — — — ADC_0	Input Only	—	—	32	49	57
E[3]	PCR[67]	ALT0 ALT1 ALT2 ALT3 —	GPIO[67] — — — AN[6]	SIUL — — — ADC_0	Input Only	—	—	—	40	48
E[4]	PCR[68]	ALT0 ALT1 ALT2 ALT3 —	GPIO[68] — — — AN[7]	SIUL — — — ADC_0	Input Only	—	—	—	42	50
E[5]	PCR[69]	ALT0 ALT1 ALT2 ALT3 —	GPIO[69] — — — AN[8]	SIUL — — — ADC_0	Input Only	—	—	—	44	52
E[6]	PCR[70]	ALT0 ALT1 ALT2 ALT3 —	GPIO[70] — — — AN[9]	SIUL — — — ADC_0	Input Only	—	—	—	46	54

Table 7. Pin muxing(1) (continued)

Port pin	PCR No.	Alternate function(2),(3)	Functions	Peripheral(4)	I/O direction(5)	Pad speed(6)		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176(7)
E[7]	PCR[71]	ALT0 ALT1 ALT2 ALT3 —	GPIO[71] — — — AN[10]	SIUL — — — ADC_0	Input Only	—	—	—	48	56
E[8]	PCR[72]	ALT0 ALT1 ALT2 ALT3 —	GPIO[72] — — — AN[22]	SIUL — — — ADC_0	Input Only	—	—	—	59	67
E[9]	PCR[73]	ALT0 ALT1 ALT2 ALT3 —	GPIO[73] — — — AN[23]	SIUL — — — ADC_0	Input Only	—	—	—	61	69
E[10]	PCR[74]	ALT0 ALT1 ALT2 ALT3 —	GPIO[74] — — — AN[24]	SIUL — — — ADC_0	Input Only	—	—	—	63	75
E[11]	PCR[75]	ALT0 ALT1 ALT2 ALT3 —	GPIO[75] — — — AN[25]	SIUL — — — ADC_0	Input Only	—	—	—	65	77
E[12]	PCR[76]	ALT0 ALT1 ALT2 ALT3 —	GPIO[76] — — — AN[26]	SIUL — — — ADC_0	Input Only	—	—	—	67	79
E[13]	PCR[77]	ALT0 ALT1 ALT2 ALT3 —	GPIO[77] SCK_3 — — EIRQ[25]	SIUL DSPI_3 — — SIUL	I/O I/O — — I	Slow	Medium	—	117	141
E[14]	PCR[78]	ALT0 ALT1 ALT2 ALT3 —	GPIO[78] SOUT_3 — — EIRQ[26]	SIUL DSPI_3 — — SIUL	I/O O — — I	Slow	Medium	—	119	143

Table 7. Pin muxing[(1)] (continued)

Port pin	PCR No.	Alternate function[(2),(3)]	Functions	Peripheral [(4)]	I/O direction [(5)]	Pad speed[(6)] SRC = 0	Pad speed[(6)] SRC = 1	Pin LQFP 100	Pin LQFP 144	Pin LQFP 176[(7)]
E[15]	PCR[79]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[79] — — — SIN_3 EIRQ[27]	SIUL — — — DSPI_3 SIUL	I/O — — — I I	Slow	Medium	—	121	145
Port F										
F[0]	PCR[80]	ALT0 ALT1 ALT2 ALT3 —	GPIO[80] DBG_0 CS3_3 — EIRQ[28]	SIUL FlexRay_0 DSPI_3 — SIUL	I/O O O — I	Slow	Medium	—	133	157
F[1]	PCR[81]	ALT0 ALT1 ALT2 ALT3 —	GPIO[81] DBG_1 CS2_3 — EIRQ[29]	SIUL FlexRay_0 DSPI_3 — SIUL	I/O O O — I	Slow	Medium	—	135	159
F[2]	PCR[82]	ALT0 ALT1 ALT2 ALT3	GPIO[82] DBG_2 CS1_3 —	SIUL FlexRay_0 DSPI_3 —	I/O O O —	Slow	Medium	—	137	161
F[3]	PCR[83]	ALT0 ALT1 ALT2 ALT3	GPIO[83] DBG_3 CS0_3 —	SIUL FlexRay_0 DSPI_3 —	I/O O I/O —	Slow	Medium	—	139	167
F[4]	PCR[84]	ALT0 ALT1 ALT2 ALT3	— — MDO[3] —	— — nexus_0 —	— — O —	Slow	Fast	—	4	4
F[5]	PCR[85]	ALT0 ALT1 ALT2 ALT3	— — MDO[2] —	— — nexus_0 —	— — O —	Slow	Fast	—	5	13
F[6]	PCR[86]	ALT0 ALT1 ALT2 ALT3	GPIO[86] — MDO[1] —	SIUL — nexus_0 —	I/O — O —	Slow	Fast	—	8	16

3 Electrical characteristics

3.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This can be done by the internal pull-up or pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

Caution: All of the following parameter values can vary depending on the application and must be confirmed during silicon validation, silicon characterization or silicon reliability trial.

3.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 8* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 8. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

Table 13. Thermal characteristics for 100-pin LQFP

Symbol		Parameter	Conditions	Typical value	Unit
$R_{\theta JA}$	D	Thermal resistance junction-to-ambient, natural convection(1)	Single layer board—1s	47.3	°C/W
	D		Four layer board—2s2p	35.6	°C/W
$R_{\theta JB}$	D	Thermal resistance junction-to-board(2)	Four layer board—2s2p	19.1	°C/W
$R_{\theta JCtop}$	D	Thermal resistance junction-to-case (top)(3)	Single layer board—1s	9.1	°C/W
Ψ_{JB}	D	Junction-to-board, natural convection(4)	Operating conditions	19.1	°C/W
Ψ_{JC}	D	Junction-to-case, natural convection(5)	Operating conditions	1.1	°C/W

1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-7. Thermal test board meets JEDEC specification for this package.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.
5. Thermal characterization parameter indicating the temperature difference between the case and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

3.5.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from *Equation 1*:

Equation 1 $T_J = T_A + (R_{\theta JA} \times P_D)$

where:

T_A= ambient temperature for the package (^oC)

$R_{\theta JA}$= junction to ambient thermal resistance ($^oC/W$)

P_D= power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in *Equation 2* as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

Equation 2 $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

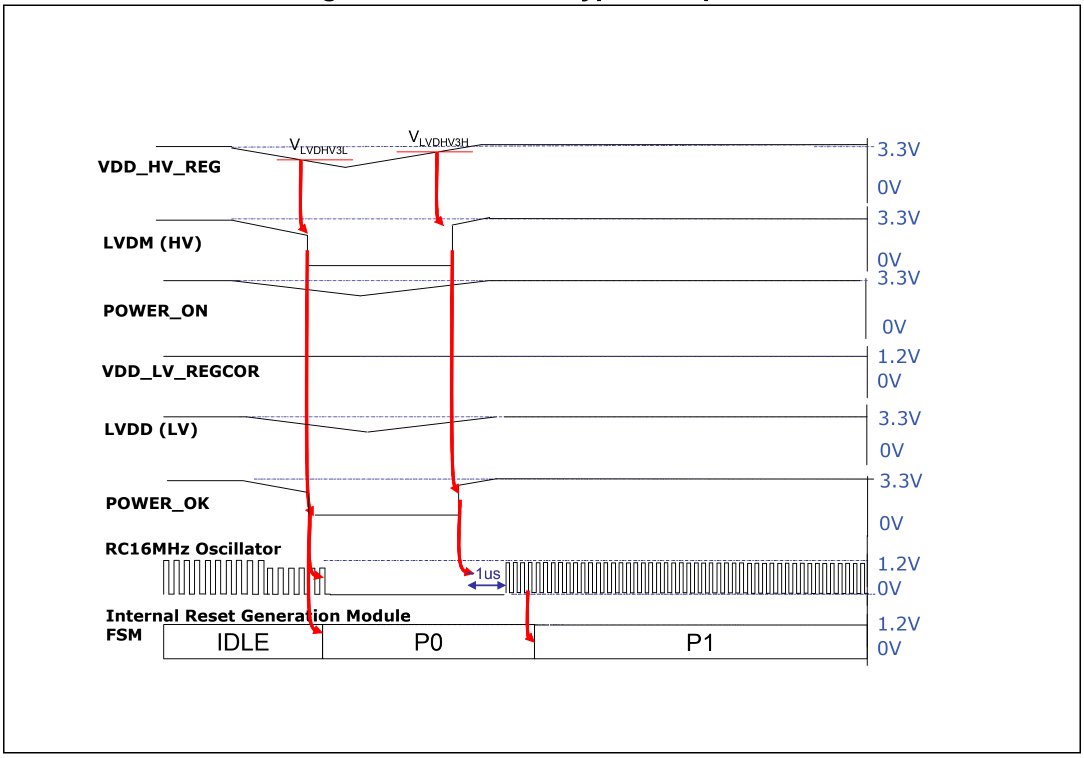
where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$= junction to case thermal resistance (°C/W)

$R_{\theta CA}$= case to ambient thermal resistance (°C/W)

Figure 12. Brown-out typical sequence



3.10 NVUSRO register

Portions of the device configuration, such as high voltage supply, and watchdog enable/disable after reset are controlled via bit values in the non-volatile user options register (NVUSRO) register.

For a detailed description of the NVUSRO register, please refer to the device reference manual.

3.10.1 NVUSRO[PAD3V5V] field description

Table 19 shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 19. PAD3V5V field description(1)

Value(2)	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1. See the device reference manual for more information on the NVUSRO register.
2. '1' is delivery value. It is part of shadow Flash, thus programmable by customer.

The DC electrical characteristics are dependent on the PAD3V5V bit value.

Table 21. Supply current (5.0 V, NVUSRO[PAD3V5V]=0)

Symbol		Parameter		Conditions		Value Typ	Value Max	Unit
$I_{DD\_LV\_CORE}$	T	Supply current	RUN — Maximum Mode(1)	$V_{DD\_LV\_CORE}$ externally forced at 1.3 V ADC Freq = 32 MHz PLL Freq = 64 MHz	64 MHz	90	120	mA
			RUN - Platform consumption, single core(2)	VDD_LV_CORE externally forced to 1.3V	16 MHz	21	37	
					40 MHz	35	55	
					64 MHz	48	72	
			RUN - Platform consumption, dual core(3)		16 MHz	24	41	
					40 MHz	42	64	
					64 MHz	58	85	
	P		RUN — Maximum Mode(4)	$V_{DD\_LV\_CORE}$ externally forced at 1.3 V	64 MHz	85	113	
			HALT Mode(5)	$V_{DD\_LV\_CORE}$ externally forced at 1.3 V	—	5.5	15	
			STOP Mode(6)	$V_{DD\_LV\_CORE}$ externally forced at 1.3 V	—	4.5	13	
I_{DD_FLASH}	T		Flash memory supply current during read	$V_{DD\_HV\_FL}$ at 5.0 V	—	—	14	
			Flash memory supply current during erase operation on 1 flash memory module	$V_{DD\_HV\_FL}$ at 5.0 V	—	—	42	
I_{DD_ADC}	T		ADC supply current — Maximum Mode	$V_{DD\_HV\_AD}$ at 5.0 V ADC Freq = 16 MHz	—	3	4	
I_{DD_OSC}	T		OSC supply current	V_{DD_OSC} at 5.0 V	8 MHz	2.6	3.2	

1. Maximum mode configuration: Code fetched from Flash executed by dual core, SIUL, PIT, ADC_0, eTimer_0/1, LINFlex_0/1, STM, INTC_0/1, DSPI_0/1/2/3/4, FlexCAN_0/1, FlexRay (static consumption), CRC_0/1, FCCU, SRAM enabled. I/O supply current excluded.
2. RAM, Code and Data Flash powered, code fetched from Flash executed by single core, all peripherals gated; IRC16MHz on, PLL64MHz OFF (except for code running at 64 MHz).
   Code is performing continuous data transfer from Flash to RAM.
3. RAM, Code and Data Flash powered, code fetched from Flash executed by dual core, all peripherals gated; IRC16MHz on, PLL64MHz OFF (except for code running at 64 MHz).
   Code is performing continuous data transfer from Flash to RAM.
4. Maximum mode configuration: Code fetched from RAM executed by dual core, SIUL, PIT, ADC_0, eTimer_0/1, LINFlex_0/1, STM, INTC_0/1, DSPI_0/1/2/3/4, FlexCAN_0/1, FlexRay (static consumption), CRC_0/1, FCCU, SRAM enabled. I/O supply current excluded.
5. HALT mode configuration, only for the “P” classification: Code Flash memory in low power mode, data Flash memory in power down mode, OSC/PLL are OFF, FIRC is ON, Core clock gated, all peripherals are disabled.
6. STOP mode configuration, only for the “P” classification: Code and data Flash memories in power down mode, OSC/PLL are OFF, FIRC is ON, Core clock gated, all peripherals are disabled.

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Equation 5

$$\tau_1 = (R_{SW} + R_{AD}) \times \frac{C_P \times C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Equation 6

$$\tau_1 < (R_{SW} + R_{AD}) \times C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to *Equation 7*:

Equation 7

$$V_{A1} \times (C_S + C_{P1} + C_{P2}) = V_A \times (C_{P1} + C_{P2})$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Equation 8

$$\tau_2 < R_L \times (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraint on R_L sizing is obtained:

Equation 9

$$8.5 \times \tau_2 = 8.5 \times R_L \times (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. *Equation 10* must be respected (charge balance assuming now C_S already charged at V_{A1}):

Equation 10

$$V_{A2} \times (C_S + C_{P1} + C_{P2} + C_F) = V_A \times C_F + V_{A1} \times (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the R_FC_F filter, is not able to provide the extra charge to compensate the voltage drop on

3.18.2 IEEE 1149.1 interface timing

Table 38. JTAG pin AC electrical characteristics

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	CC	D	TCK cycle time	—	100	—	ns
2	t_{JDC}	CC	D	TCK clock pulse width (measured at $V_{DD\_HV\_IOx}/2$)	—	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40% – 70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	—	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO data valid	—	—	40	ns
7	t_{TDOI}	CC	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	CC	D	TCK low to TDO high impedance	—	40	—	ns
9	t_{BSDV}	CC	D	TCK falling edge to output valid	—	—	50	ns
10	t_{BSDVZ}	CC	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
11	t_{BSDHZ}	CC	D	TCK falling edge to output high impedance	—	—	50	ns
12	t_{BSDST}	CC	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
13	t_{BSDHT}	CC	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

Figure 22. JTAG test clock input timing

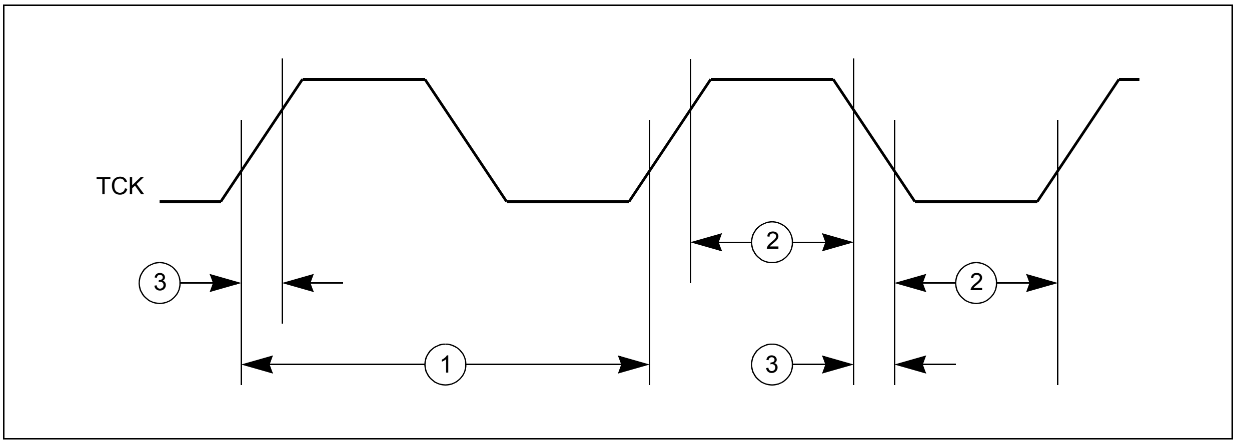
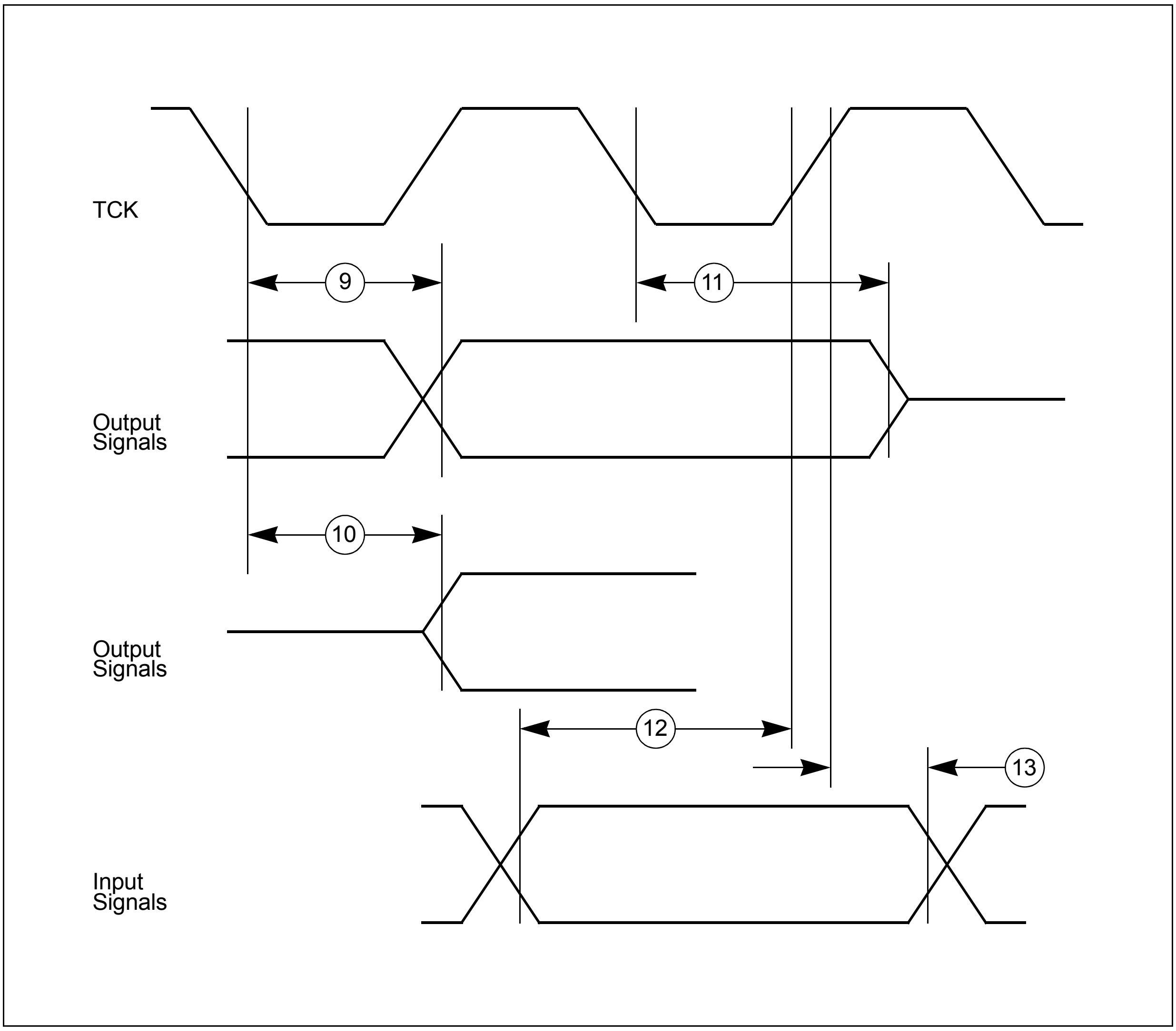


Figure 24. JTAG boundary scan timing



3.18.3 Nexus timing

Table 39. Nexus debug port timing(1)

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{MCYC}	CC	D	MCKO cycle time	32	—	—	ns
2	t_{MDOV}	CC	D	MCKO edge to MDO data valid	–0.1 × t_{MCYC}	—	0.25 × t_{MCYC}	ns
3	t_{MSEOV}	CC	D	MCKO edge to $\overline{\text{MSEO}}$ data valid	–0.1 × t_{MCYC}	—	0.25 × t_{MCYC}	ns
4	t_{EVTOV}	CC	D	MCKO edge to $\overline{\text{EVTO}}$ data valid	–0.1 × t_{MCYC}	—	0.25 × t_{MCYC}	ns
5	t_{TCYC}	CC	D	TCK cycle time	64(2)	—	—	ns

Figure 34. DSPI modified transfer format timing — master, CPHA = 1

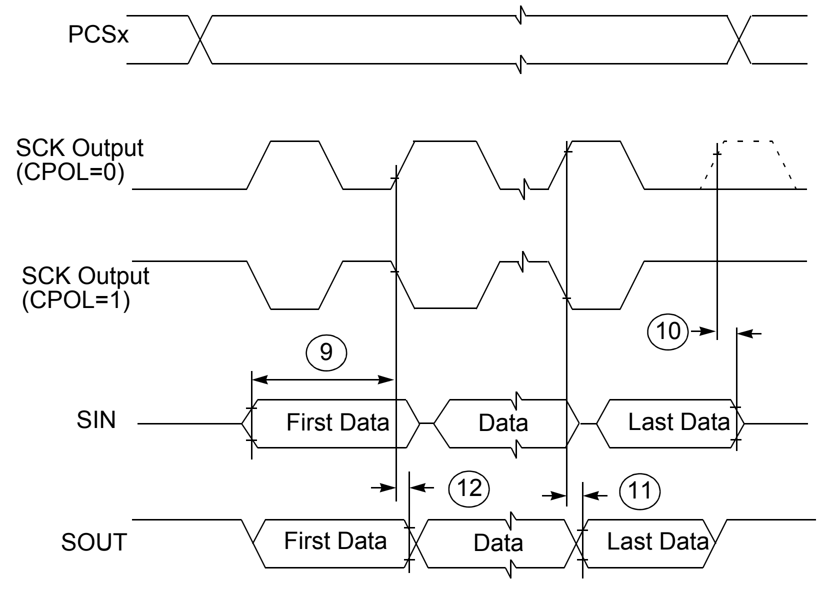


Figure 35. DSPI modified transfer format timing — slave, CPHA = 0

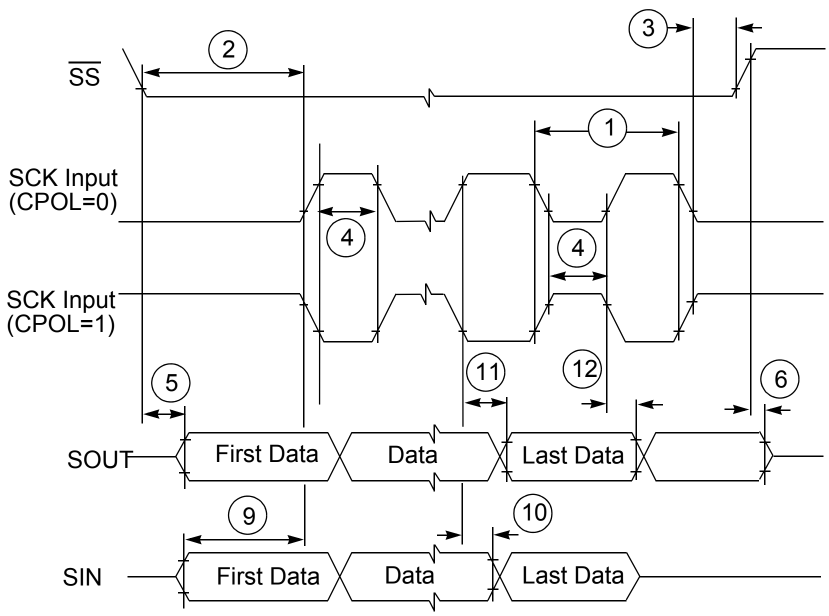


Figure 36. DSPI modified transfer format timing — slave, CPHA = 1

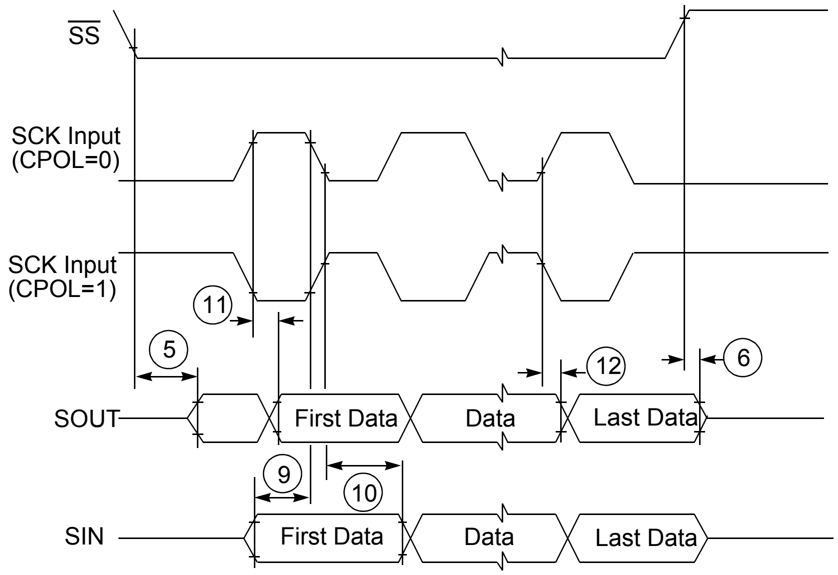
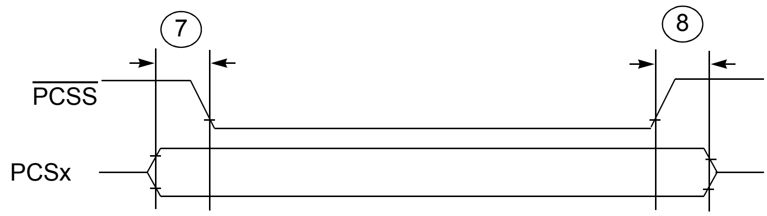


Figure 37. DSPI PCS strobe (PCSS) timing



4.2.2 LQFP100 mechanical outline drawing

Figure 39. LQFP100 package mechanical drawing

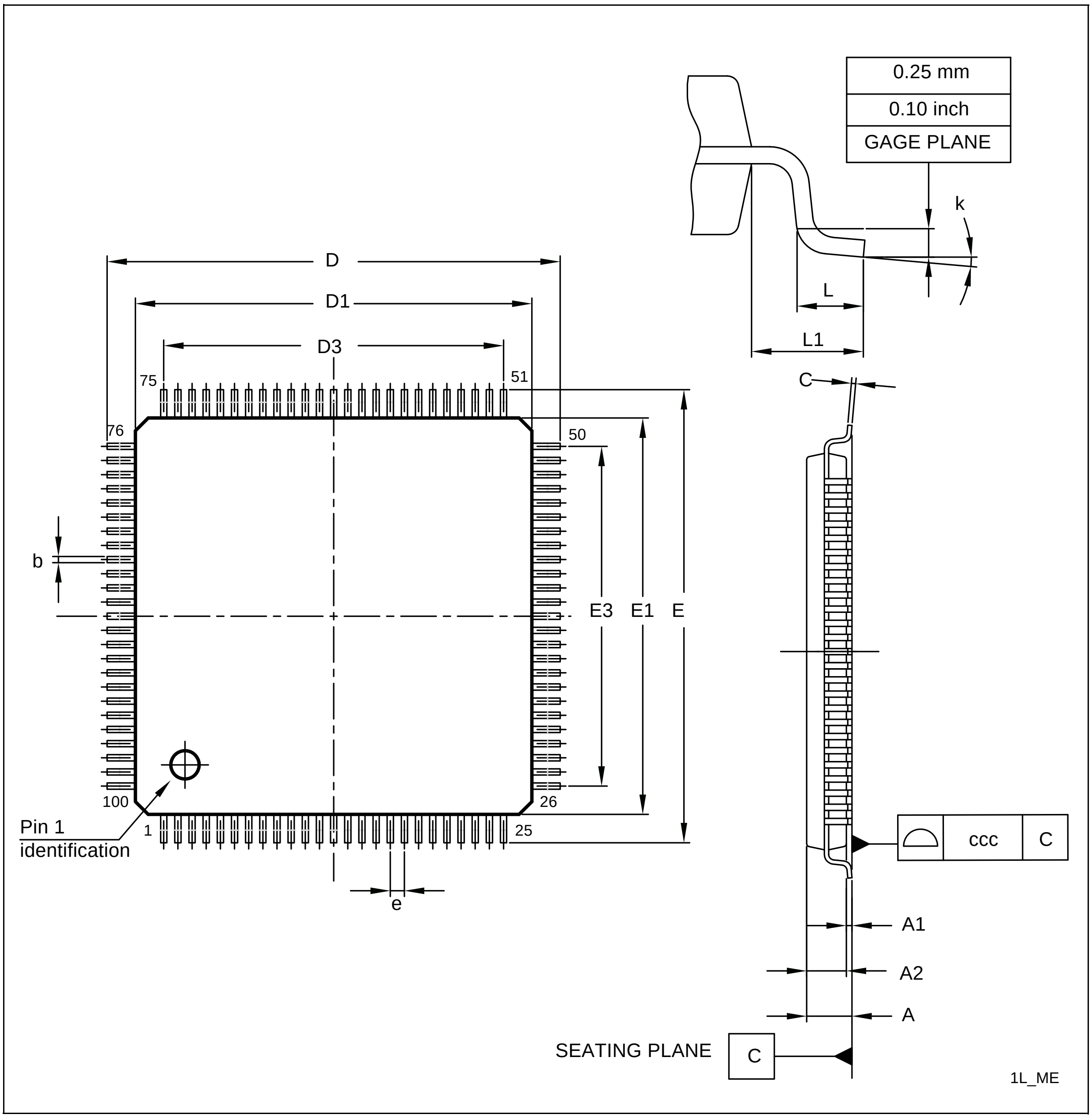


Table 43. LQFP100 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571