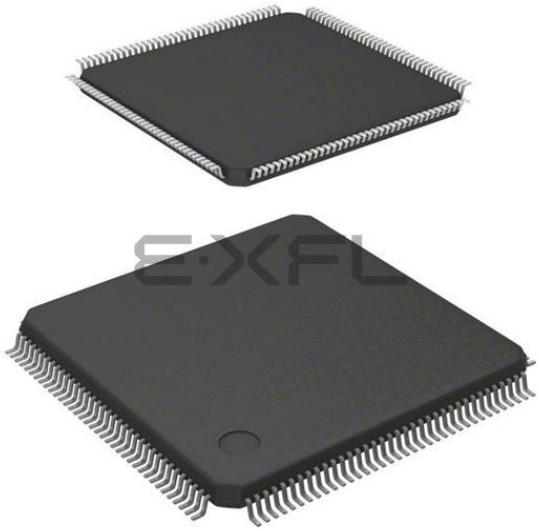

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 26x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p60l5ceaar

Table 1. Device summary

Package	Part number	
	768 KB Flash	1 MB Flash
LQFP144	SPC560P54L5 SPC56AP54L5	SPC560P60L5 SPC56AP60L5
LQFP100	SPC560P54L3 SPC56AP54L3	SPC560P60L3 SPC56AP60L3

SPC56xP54x/SPC56xP60x is present on the market in two different options enabling different features: Full-featured, and Airbag configuration. *Table 3* shows the main differences between the two versions.

Table 3. SPC56xP54x/SPC56xP60x device configuration difference

Feature	Enhanced Full-featured	Full-featured	Airbag
FlexCAN (controller area network)	3	2	2
CTU (cross triggering unit)	Yes		No
FlexRay	Yes (64 message buffer)		No
DSPI (deserial serial peripheral interface) modules	5		4
CRC (cyclic redundancy check) unit	2		1

1.4 Block diagram

Figure 1 shows a top-level block diagram of the SPC56xP54x/SPC56xP60x MCU. *Table 4* summarizes the functions of the blocks.

The flash memory module provides the following features:

- Up to 1024 KB flash memory
  - 14 blocks (2×16 KB + 2×32 KB + 2×16 KB + 2×64 KB + 6×128 KB) code flash
  - 4 blocks (16 KB + 16 KB + 16 KB + 16 KB) data flash
  - Full Read While Write (RWW) capability between code and data flash
- Four 128-bit wide prefetch buffers to provide single cycle in-line accesses (prefetch buffers can be configured to prefetch code or data or both)
- Typical flash memory access time: 0 wait states for buffer hits, 2 wait states for page buffer miss at 64 MHz
- Hardware managed flash memory writes handled by 32-bit RISC Krypton engine
- Hardware and software configurable read and write access protections on a per-master basis.
- Configurable access timing allowing use in a wide range of system frequencies.
- Multiple-mapping support and mapping-based block access timing (0–31 additional cycles) allowing use for emulation of other memory types.
- Software programmable block program/erase restriction control.
- Erase of selected block(s)
- Read page size of 128 bits (4 words)
- 64-bit ECC with single-bit correction, double-bit detection for data integrity
- Embedded hardware program and erase algorithm
- Erase suspend, program suspend and erase-suspended program
- Censorship protection scheme to prevent flash memory content visibility
- Hardware support for EEPROM emulation

1.5.5 On-chip SRAM with ECC

The SPC56xP54x/SPC56xP60x SRAM module provides a general-purpose memory of up to 80 KB.

The SRAM module provides the following features:

- Supports read/write accesses mapped to the SRAM memory from any master
- Up to 80 KB general purpose RAM
  - 2 blocks (48 KB + 32 KB)
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory
- Typical SRAM access time: 0 wait state for reads and 32-bit writes; 1 wait state for 8- and 16-bit writes if back to back with a read to same memory block

1.5.6 Interrupt controller (INTC)

The INTC (interrupt controller) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To

- Triangle wave modulation
- Programmable modulation depth (±0.25% to ±4% deviation from center frequency)
  - Programmable modulation frequency dependent on reference frequency
- Self-clocked mode (SCM) operation

1.5.9 Main oscillator

The main oscillator provides these features:

- Input frequency range 4 MHz to 40 MHz
- Crystal input mode or Oscillator input mode
- PLL reference

1.5.10 Internal RC oscillator

This device has an RC ladder phase-shift oscillator. The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared by the stable bandgap reference voltage.

The RC Oscillator provides these features:

- Nominal frequency 16 MHz
- ±6% variation over voltage and temperature after process trim
- Clock output of the RC oscillator serves as system clock source in case loss of lock or loss of clock is detected by the PLL
- RC oscillator is used as the default system clock during startup

1.5.11 Periodic interrupt timer (PIT)

The PIT module implements these features:

- Up to four general purpose interrupt timers
- 32-bit counter resolution
- Clocked by system clock frequency
- Each channel can be used as trigger for a DMA request

1.5.12 System timer module (STM)

The STM module implements these features:

- 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

The STM module is replicated for each processor.

The default booting scheme is the one which uses the internal flash memory (an internal pull-down is used to select this mode). The alternate option allows the user to boot via FlexCAN or LINFlex (using the boot assist module software).

A censorship scheme is provided to protect the contents of the flash memory and offer increased security for the entire device.

A password mechanism is designed to grant the legitimate user access to the non-volatile memory.

1.5.16.1 Boot assist module (BAM)

The BAM is a block of read-only one-time programmed memory and is identical for all SPC56xP54x/SPC56xP60x devices that are based on the e200z0h core. The BAM program is executed every time the device is powered on if the alternate boot mode has been selected by the user.

The BAM provides the following features:

- Serial bootloading via FlexCAN or LINFlex.
- BAM can accept a password via the used serial communication channel to grant the legitimate user access to the non-volatile memory.

1.5.17 Error correction status module (ECSM)

The ECSM on this device features the following:

- Platform configuration and revision
- ECC error reporting for flash memory and SRAM
- ECC error injection for SRAM

The ECSM module is replicated for each processor.

1.5.18 FlexCAN

The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. FlexCAN module contains 32 message buffers.

The FlexCAN module provides the following features:

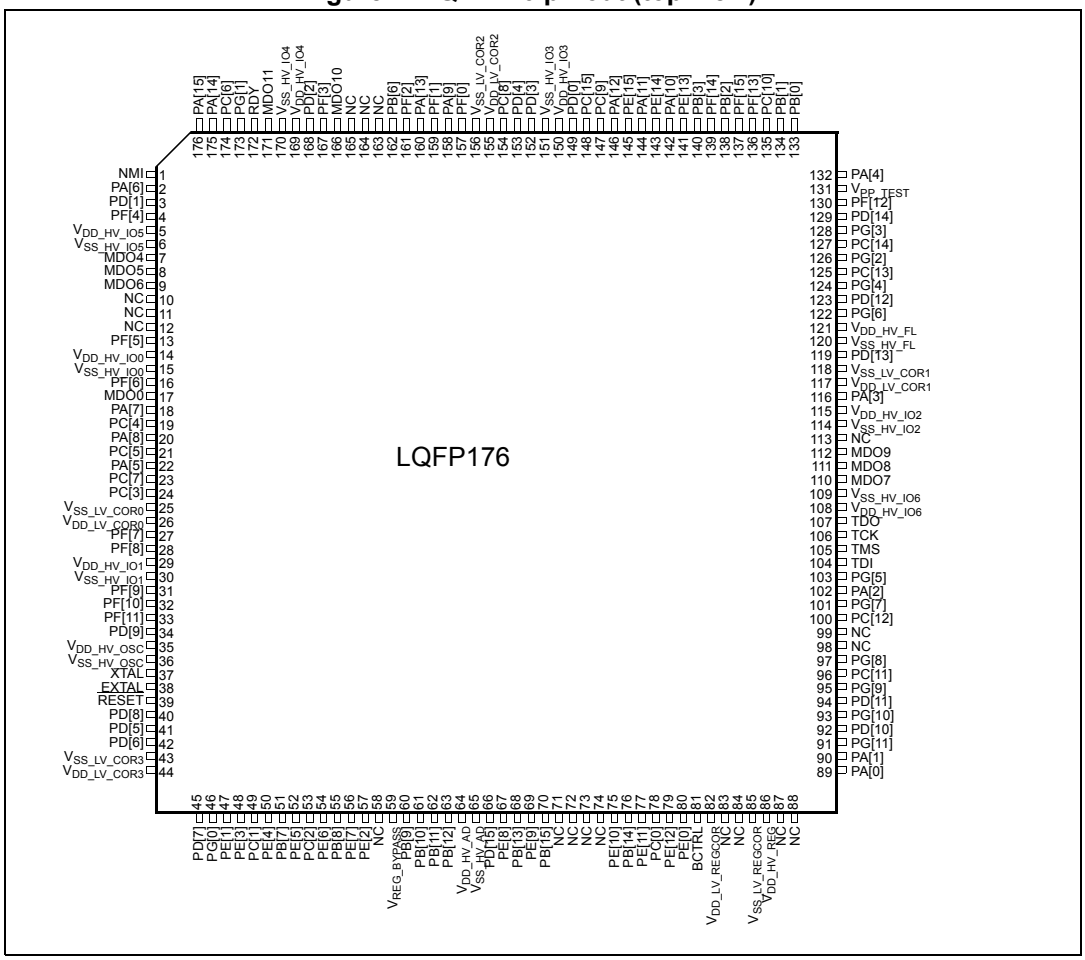
- Full implementation of the CAN protocol specification, Version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - 0 to 8 bytes data length
  - Programmable bit rate as fast as 1 Mbit/s
- 32 message buffers of 0 to 8 bytes data length
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- 3 programmable mask registers

2 Package pinouts and signal descriptions

2.1 Package pinouts

The LQFP pinouts are shown in the following figures.

Figure 2. LQFP176 pinout (top view)[b]



b. Software development package only. Not available for production.

Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
A[2] [8]	PCR[2]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[2] ETC[2] CS3_4 — SIN_2 ABS[0] EIRQ[2]	SIUL eTimer_0 DSPI_4 — DSPI_2 MC_RGM SIUL	I/O I/O O — I I I	Slow	Medium	57	84	102
A[3] [8]	PCR[3]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[3] ETC[3] CS0_2 — ABS[1] EIRQ[3]	SIUL eTimer_0 DSPI_2 — MC_RGM SIUL	I/O I/O I/O — I I	Slow	Medium	64	92	116
A[4] [8]	PCR[4]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[4] ETC[0] CS1_2 ETC[4] FAB EIRQ[4]	SIUL eTimer_1 DSPI_2 eTimer_0 MC_RGM SIUL	I/O I/O O I/O I I	Slow	Medium	75	108	132
A[5]	PCR[5]	ALT0 ALT1 ALT2 ALT3 —	GPIO[5] CS0_1 ETC[5] CS7_0 EIRQ[5]	SIUL DSPI_1 eTimer_1 DSPI_0 SIUL	I/O I/O I/O O I	Slow	Medium	8	14	22
A[6]	PCR[6]	ALT0 ALT1 ALT2 ALT3 —	GPIO[6] SCK_1 CS2_4 — EIRQ[6]	SIUL DSPI_1 DSPI_4 — SIUL	I/O I/O I/O — I	Slow	Medium	2	2	2
A[7]	PCR[7]	ALT0 ALT1 ALT2 ALT3 —	GPIO[7] SOUT_1 CS1_4 — EIRQ[7]	SIUL DSPI_1 DSPI_4 — SIUL	I/O O I/O — I	Slow	Medium	4	10	18
A[8]	PCR[8]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[8] — CS0_4 — SIN_1 EIRQ[8]	SIUL — DSPI_4 — DSPI_1 SIUL	I/O — I/O — I I	Slow	Medium	6	12	20

Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
G[8]	PCR[104]	ALT0 ALT1 ALT2 ALT3 —	GPIO[104] — CS3_4 — —	SIUL — DSPI_4 — —	I/O — O — —	Slow	Medium	—	81	97
G[9]	PCR[105]	ALT0 ALT1 ALT2 ALT3 —	GPIO[105] — — — RXD	SIUL — — — FlexCAN_1	I/O — — — I	Slow	Medium	—	79	95
G[10]	PCR[106]	ALT0 ALT1 ALT2 ALT3	GPIO[106] — TXD —	SIUL — FlexCAN_1 —	I/O — O —	Slow	Medium	—	77	93
G[11]	PCR[107]	ALT0 ALT1 ALT2 ALT3	GPIO[107] — — —	SIUL — — —	I/O — — —	Slow	Medium	—	75	91

1. This table concerns Enhanced Full-featured version. Please refer to “SPC56xP54x/SPC56xP60x device configuration difference” table for difference between Enhanced Full-featured, Full-featured, and Airbag configuration.
2. ALT0 is the primary (default) function for each port after reset.
3. Alternate functions are chosen by setting the values of the PCR[PA] bitfields inside the SIU module. PCR[PA] = 00 → ALT0; PCR[PA] = 01 → ALT1; PCR[PA] = 10 → ALT2; PCR[PA] = 11 → ALT3. This is intended to select the output functions; to use one of the input-only functions, the PCR[IBE] bit must be written to ‘1’, regardless of the values selected in the PCR[PA] bitfields. For this reason, the value corresponding to an input only function is reported as “—”.
4. Module included on the MCU.
5. Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMI[PADSEL*x*] bitfields inside the SIUL module.
6. Programmable via the SRC (Slew Rate Control) bits in the respective Pad Configuration Register.
7. LQFP176 available only as development package.
8. Weak pull down during reset.

3 Electrical characteristics

3.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This can be done by the internal pull-up or pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

Caution: All of the following parameter values can vary depending on the application and must be confirmed during silicon validation, silicon characterization or silicon reliability trial.

3.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 8* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 8. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute maximum ratings

Table 9. Absolute maximum ratings(1)

Symbol		Parameter	Conditions	Min	Max(2)	Unit
V_{SS_HV}	SR	Digital ground	—	0	0	V
$V_{DD\_HV\_IOx}$(3)	SR	3.3 V / 5.0 V input/output supply voltage with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
$V_{DD\_HV\_FL}$	SR	3.3 V / 5.0 V code and data flash memory supply voltage with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3	
$V_{SS\_HV\_FL}$	SR	Code and data flash memory ground with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
$V_{DD\_HV\_OSC}$	SR	3.3 V / 5.0 V crystal oscillator amplifier supply voltage with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3	
$V_{SS\_HV\_OSC}$	SR	3.3 V / 5.0 V crystal oscillator amplifier reference voltage with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
$V_{DD\_HV\_REG}$	SR	3.3 V / 5.0 V voltage regulator supply voltage with respect to ground (V_{SS_HV})	—	– 0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	– 0.3	$V_{DD\_HV\_IOx}$ + 0.3	
$V_{DD\_HV\_AD}$	SR	3.3 V / 5.0 V ADC supply and high reference voltage with respect to ground (V_{SS_HV})	$V_{DD\_HV\_REG}$ < 2.7 V	– 0.3	$V_{DD\_HV\_REG}$ + 0.3	V
			$V_{DD\_HV\_REG}$ > 2.7 V	– 0.3	6.0	
$V_{SS\_HV\_AD}$	SR	ADC ground and low reference voltage with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
TV_{DD}	SR	Slope characteristics on all V_{DD} during power up(4) with respect to ground (V_{SS_HV})	—	3.0(5)	500 x 10^3 (0.5 [V/µs])	V/s
V_{IN}	SR	Voltage on any pin with respect to ground ($V_{SS\_HV\_IOx}$) with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3	
V_{INAN}	SR	Analog input voltage	$V_{DD\_HV\_REG}$ < 2.7 V	$V_{SS\_HV\_AD}$ – 0.3	$V_{DD\_HV\_AD}$ + 0.3	V
			$V_{DD\_HV\_REG}$ > 2.7 V	$V_{SS\_HV\_AD}$	$V_{DD\_HV\_AD}$	V
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA

Table 10. Recommended operating conditions (5.0 V) (continued)

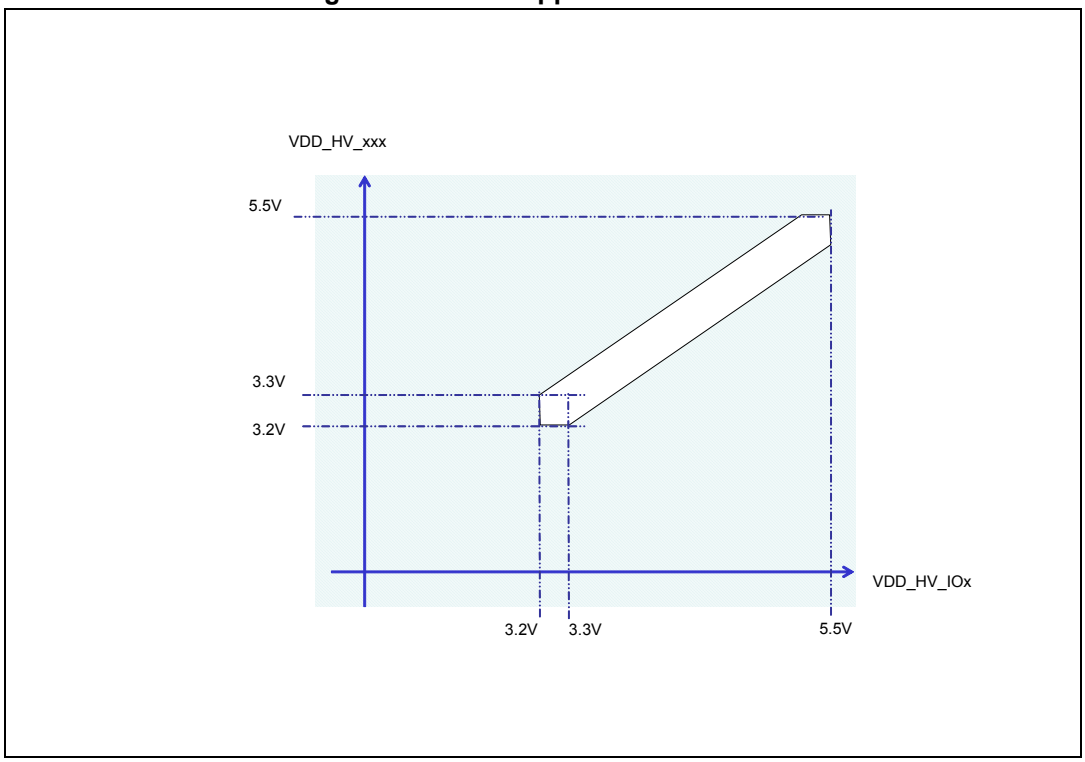
Symbol		Parameter	Conditions	Min	Max(1)	Unit
$V_{DD\_HV\_REG}$	SR	5.0 V voltage regulator supply voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$ – 0.1	$V_{DD\_HV\_IOx}$ + 0.1	
$V_{DD\_HV\_AD}$	SR	5.0 V ADC supply and high reference voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_REG}$	$V_{DD\_HV\_REG}$ – 0.1	—	
$V_{SS\_HV\_AD}$	SR	ADC ground and low reference voltage	—	0	0	V
$V_{DD\_LV\_REGCOR}$(3),(4)	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_REGCOR}$(3)	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_CORx}$(3),(4)	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_CORx}$(3)	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	—	–40	125	°C

1. Parametric figures can be out of specification when voltage drops below 4.5 V, however, guaranteeing the full functionality. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.
2. The difference between each couple of voltage supplies must be less than 100 mV, $|V_{DD\_HV\_IOy} – V_{DD\_HV\_IOx}| < 100$ mV.
3. To be connected to emitter of external NPN. Low voltage supplies are not under user control—these are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds ($V_{SS\_LV\_xxx}$) must be shorted to high voltage grounds ($V_{SS\_HV\_xxx}$) and the low voltage supply pins ($V_{DD\_LV\_xxx}$) must be connected to the external ballast emitter.
4. The low voltage supplies ($V_{DD\_LV\_xxx}$) are not all independent. $V_{DD\_LV\_COR1}$ and $V_{DD\_LV\_COR2}$ are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash memory module. Similarly, $V_{SS\_LV\_COR1}$ and $V_{SS\_LV\_COR2}$ are internally shorted. $V_{DD\_LV\_REGCOR}$ and $V_{DD\_LV\_REGCORx}$ are physically shorted internally, as are $V_{SS\_LV\_REGCOR}$ and $V_{SS\_LV\_CORx}$.

Table 11. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Min	Max(1)	Unit
V_{SS_HV}	SR	Digital ground	—	0	0	V
$V_{DD\_HV\_IOx}$(2)	SR	3.3 V input/output supply voltage	—	3.0	3.6	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_FL}$	SR	3.3 V code and data flash memory supply voltage	—	3.0	3.6	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$ – 0.1	$V_{DD\_HV\_IOx}$ + 0.1	
$V_{SS\_HV\_FL}$	SR	Code and data flash memory ground	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	3.0	3.6	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$ – 0.1	$V_{DD\_HV\_IOx}$ + 0.1	
$V_{SS\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	0	0	V

Figure 7. Power supplies constraints[f]



The SPC56xP54x/SPC56xP60x supply architecture provides an ADC supply that is managed independently of standard V_{DD_HV} supply. *Figure 8* shows the constraints of the ADC power supply.

f. IO AC and DC characteristics are guaranteed only in the range 3.0 V–3.6 V when PAD3V5V is low, and in the range 4.5 V–5.5 V when PAD3V5V is high.

Table 13. Thermal characteristics for 100-pin LQFP

Symbol		Parameter	Conditions	Typical value	Unit
$R_{\theta JA}$	D	Thermal resistance junction-to-ambient, natural convection(1)	Single layer board—1s	47.3	°C/W
	D		Four layer board—2s2p	35.6	°C/W
$R_{\theta JB}$	D	Thermal resistance junction-to-board(2)	Four layer board—2s2p	19.1	°C/W
$R_{\theta JCtop}$	D	Thermal resistance junction-to-case (top)(3)	Single layer board—1s	9.1	°C/W
Ψ_{JB}	D	Junction-to-board, natural convection(4)	Operating conditions	19.1	°C/W
Ψ_{JC}	D	Junction-to-case, natural convection(5)	Operating conditions	1.1	°C/W

1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-7. Thermal test board meets JEDEC specification for this package.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.
5. Thermal characterization parameter indicating the temperature difference between the case and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

3.5.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from *Equation 1*:

Equation 1 $T_J = T_A + (R_{\theta JA} \times P_D)$

where:

T_A= ambient temperature for the package (^oC)

$R_{\theta JA}$= junction to ambient thermal resistance ($^oC/W$)

P_D= power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in *Equation 2* as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

Equation 2 $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$= junction to case thermal resistance (°C/W)

$R_{\theta CA}$= case to ambient thermal resistance (°C/W)

Table 23. Supply current (3.3 V, NVUSRO[PAD3V5V]=1)

Symbol		Parameter		Conditions		Value		Unit
						Typ	Max	
$I_{DD\_LV\_CORE}$	T	Supply current	RUN — Maximum Mode(1)	$V_{DD\_LV\_CORE}$ externally forced at 1.3 V ADC Freq = 32 MHz PLL Freq = 64 MHz	64 MHz	90	120	mA
			RUN - Platform consumption, single core(2)	VDD_LV_CORE externally forced to 1.3V	16 MHz	21	37	
					40 MHz	35	55	
					64 MHz	48	72	
			RUN - Platform consumption, dual core(3)		16 MHz	24	41	
					40 MHz	42	64	
					64 MHz	58	85	
	P		RUN — Maximum Mode(4)	$V_{DD\_LV\_CORE}$ externally forced at 1.3 V	64 MHz	85	113	
			HALT Mode(5)	$V_{DD\_LV\_CORE}$ externally forced at 1.3 V	—	5.5	15	
			STOP Mode(6)	$V_{DD\_LV\_CORE}$ externally forced at 1.3 V	—	4.5	13	
I_{DD_FLASH}	D		Flash memory supply current during read	$V_{DD\_HV\_FL}$ at 3.3 V	—	—	14	
			Flash memory supply current during erase operation on 1 flash memory module	$V_{DD\_HV\_FL}$ at 3.3 V	—	—	42	
I_{DD_ADC}	T		ADC supply current — Maximum Mode	$V_{DD\_HV\_AD}$ at 3.3 V ADC Freq = 16 MHz	—	3	4	
I_{DD_OSC}	T		OSC supply current	V_{DD_OSC} at 3.3 V	8 MHz	2.4	3	

1. Maximum mode configuration: Code fetched from Flash executed by dual core, SIUL, PIT, ADC_0, eTimer_0/1, LINFlex_0/1, STM, INTC_0/1, DSPI_0/1/2/3/4, FlexCAN_0/1, FlexRay (static consumption), CRC_0/1, FCCU, SRAM enabled. I/O supply current excluded.
2. RAM, Code and Data Flash powered, code fetched from Flash executed by single core, all peripherals gated; IRC16MHz on, PLL64MHz OFF (except for code running at 64 MHz).
Code is performing continuous data transfer from Flash to RAM.
3. RAM, Code and Data Flash powered, code fetched from Flash executed by dual core, all peripherals gated; IRC16MHz on, PLL64MHz OFF (except for code running at 64 MHz).
Code is performing continuous data transfer from Flash to RAM.
4. Maximum mode configuration: Code fetched from RAM executed by dual core, SIUL, PIT, ADC_0, eTimer_0/1, LINFlex_0/1, STM, INTC_0/1, DSPI_0/1/2/3/4, FlexCAN_0/1, FlexRay (static consumption), CRC_0/1, FCCU, SRAM enabled. I/O supply current excluded.
5. HALT mode configuration, only for the “P” classification: Code Flash memory in low power mode, data Flash memory in power down mode, OSC/PLL are OFF, FIRC is ON, Core clock gated, all peripherals are disabled.
6. STOP mode configuration, only for the “P” classification: Code and data Flash memories in power down mode, OSC/PLL are OFF, FIRC is ON, Core clock gated, all peripherals are disabled.

Table 24. Peripherals supply current (5 V and 3.3 V)(1)

Symbol		Parameter	Conditions		Value		Unit
					Typ	Max	
$I_{DD\_HV(CAN)}$	T	CAN (FlexCAN) supply current on VDD_HV_REG	500 Kbyte/s	Total (static + dynamic) consumption: – FlexCAN in loop-back mode – XTAL@ 8 MHz used as CAN engine clock source – Message sending period is 580 µs	21.6 * f_{periph}	28.1* f_{periph}	µA
$I_{DD\_HV(SCI)}$	T	SCI (LINFlex) supply current on VDD_HV_REG	Total (static + dynamic) consumption: – LIN mode – Baudrate: 115.2 Kbyte/s		10.8 * f_{periph}	14.1 * f_{periph}	
$I_{DD\_HV(SPI)}$	T	SPI (DSPI) supply current on VDD_HV_REG	Ballast dynamic consumption (continuous communication): – Baudrate: 2 Mbit/s – Transmission every 8 µs – Frame: 16 bits		4.8 * f_{periph}	6.3 * f_{periph}	
$I_{DD\_HV(ADC)}$	T	ADC supply current on VDD_HV_REG	VDD = 5.5 V	Ballast dynamic consumption (continuous conversion)	120 * f_{periph}	156 * f_{periph}	
$I_{DD\_HV\_ADC(ADC)}$	T	ADC supply current on VDD_HV_ADC	VDD = 5.5 V	Analog dynamic consumption (continuous conversion)	0.005 * f_{periph} + 2.8	0.007 * f_{periph} + 3.4	mA
$I_{DD\_HV(eTimer)}$	T	eTimer supply current on VDD_HV_REG	PWM signals generation on all 1 channel @10kHz	Dynamic consumption does not change varying the frequency	1.8	2.4	mA
$I_{DD\_HV(FlexRay)}$	T	FlexRay supply current on VDD_HV_REG	Static consumption		4.2 * f_{periph}	5.5 * f_{periph}	µA

1. Operating conditions: f_{periph} = 8 MHz to 64 MHz

2. “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self clocked mode.
3. Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.
4. f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.
5. This value is determined by the crystal manufacturer and board design.
6. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.
7. Proper PC board layout procedures must be followed to achieve specifications.
8. Values are obtained with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).
9. Short term jitter is measured on the clock rising edge at cycle n and cycle n+4.
10. This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this PLL, load capacitors should not exceed these limits.
11. This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
12. This value is true when operating at frequencies above 60 MHz, otherwise f_{CS} is 2% (above 64 MHz).
13. Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

3.14 16 MHz RC oscillator electrical characteristics

Table 31. 16 MHz RC oscillator electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
f_{RC}	P	RC oscillator frequency	T_A = 25 °C	—	16	—	MHz
Δ_{RCMVAR}	P	Fast internal RC oscillator variation over temperature and supply with respect to f_{RC} at T_A = 25 °C in high-frequency configuration	—	–6	—	6	%
$\Delta_{RCMTRIM}$	T	Post Trim Accuracy: The variation of the PTF(1) from the 16 MHz	T_A = 25 °C	–1	—	1	%
$\Delta_{RCMSTEP}$	T	Fast internal RC oscillator trimming step	T_A = 25 °C	—	1.6	—	%

1. PTF = Post Trimming Frequency: The frequency of the output clock after trimming at typical supply voltage and temperature

3.15 Analog-to-Digital converter (ADC) electrical characteristics

The device provides a 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

3.18.2 IEEE 1149.1 interface timing

Table 38. JTAG pin AC electrical characteristics

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	CC	D	TCK cycle time	—	100	—	ns
2	t_{JDC}	CC	D	TCK clock pulse width (measured at $V_{DD\_HV\_IOx}/2$)	—	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40% – 70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	—	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO data valid	—	—	40	ns
7	t_{TDOI}	CC	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	CC	D	TCK low to TDO high impedance	—	40	—	ns
9	t_{BSDV}	CC	D	TCK falling edge to output valid	—	—	50	ns
10	t_{BSDVZ}	CC	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
11	t_{BSDHZ}	CC	D	TCK falling edge to output high impedance	—	—	50	ns
12	t_{BSDST}	CC	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
13	t_{BSDHT}	CC	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

Figure 22. JTAG test clock input timing

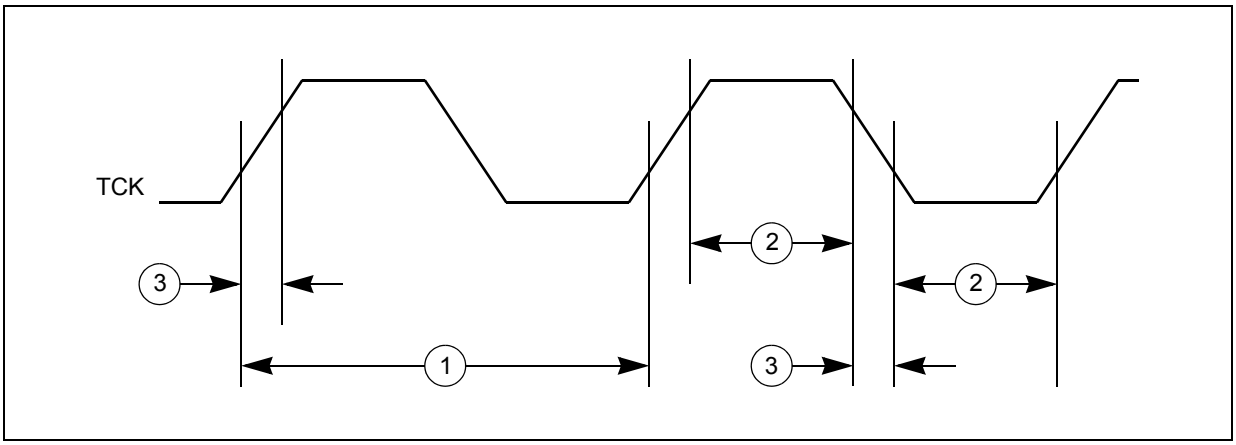


Figure 23. JTAG test access port timing

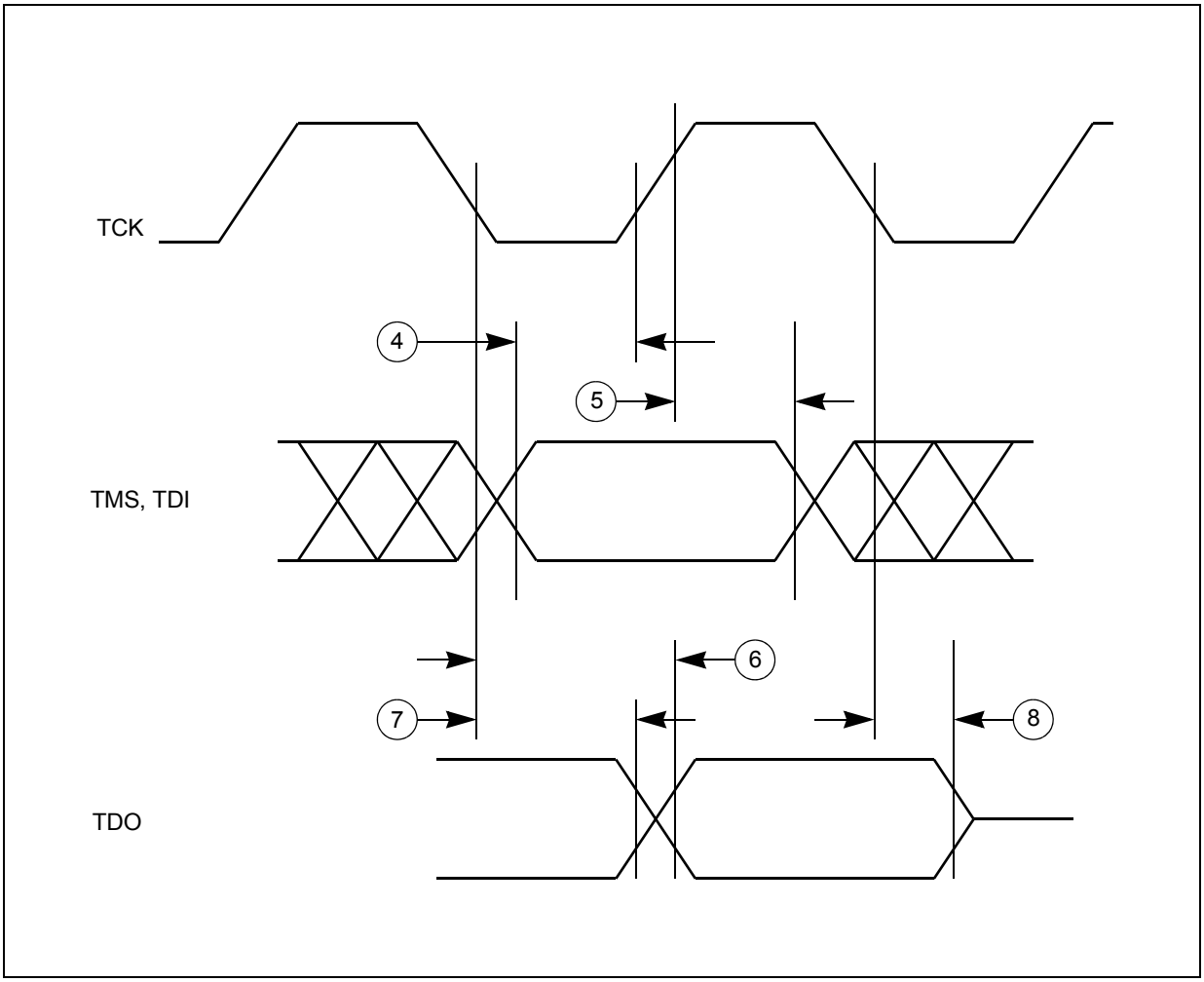
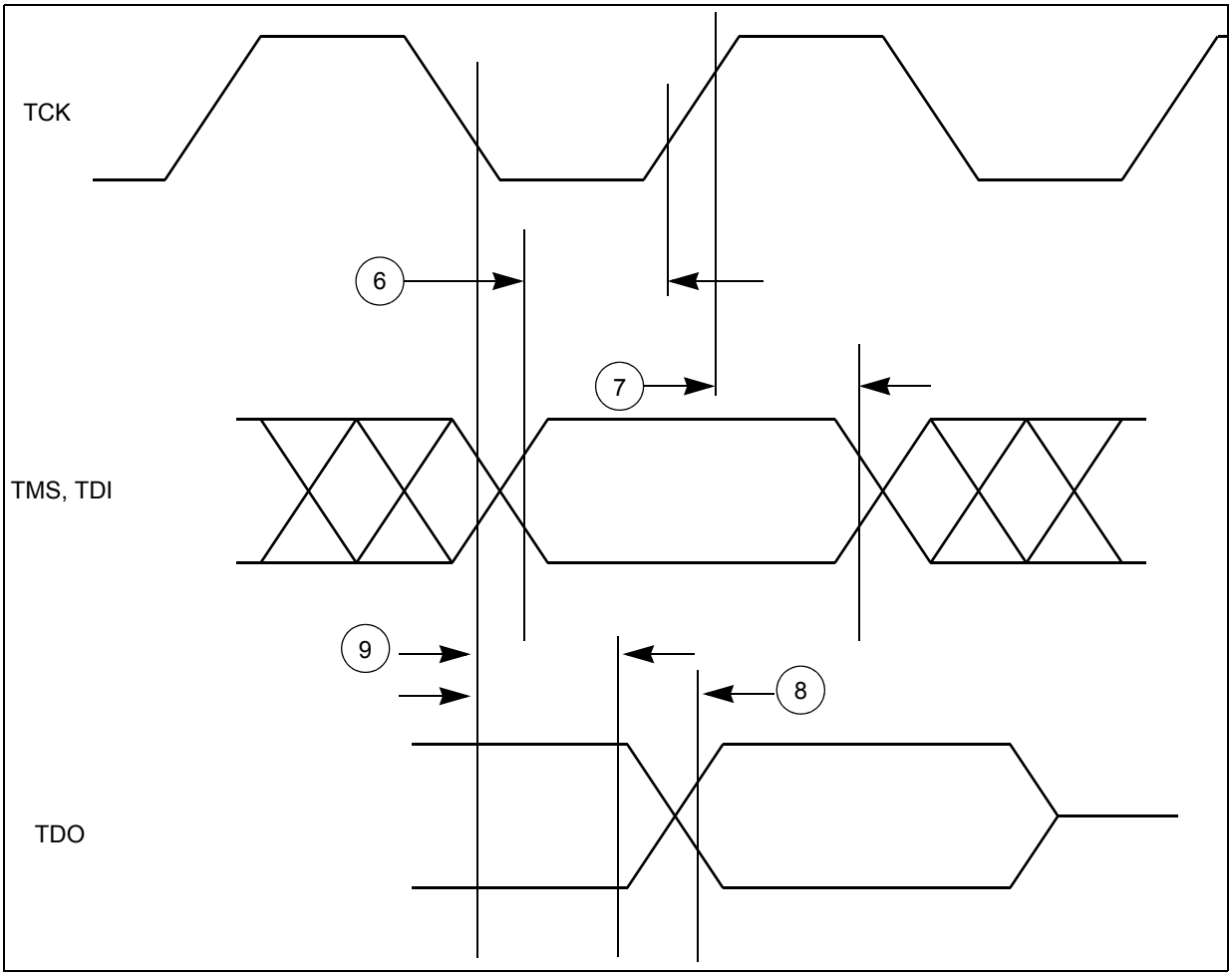


Figure 27. Nexus TDI, TMS, TDO timing



3.18.4 External interrupt timing (IRQ pin)

Table 40. External interrupt timing[1]

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	CC	D	IRQ pulse width low	—	4	—	t_{CYC}
2	t_{IPWH}	CC	D	IRQ pulse width high	—	4	—	t_{CYC}
3	t_{ICYC}	CC	D	IRQ edge to edge time[2]	—	4 + N [3]	—	t_{CYC}

1. IRQ timing specified at f_{SYS} = 64 MHz and $V_{DD\_HV\_IOx}$ = 3.0 V to 5.5 V, $T_A = T_L$ to T_H, and CL = 200pF with SRC = 0b00.
2. Applies when IRQ pins are configured for rising edge or falling edge events, but not both.
3. N= ISR time to clear the flag.

6 Revision history

Table 44 summarizes revisions to this document.

Table 44. Document revision history

Date	Revision	Substantive changes
21-Dec-2010	1	Initial release
18-Oct-2011	2	In the Feature list: Revised the first bullet. Changed “Up to 82 GPIO” to “Up to 80 GPIO” Changed “and 82 GPIO” to “and 49 GPIO” Changed “FlexRay module“ to “1 FlexRay™ module”. Added *Section 1.5: Feature details* *Table 4: SPC56xP54x/SPC56xP60x series block summary*, added FlexRay entry. In the “LQFP176 pinout (top view)” figure: – Pin 104 now is TDI, was PB[5] – Pin 107 now is TDO, was PB[4] – Pin 71 now is NC, was OKOUT – Pin 72 now is NC, was OKOUT_B – Pin 87 now is NC, was NBYPASS_HV – Pin 88 now is NC, was IPP_LIVI_B_VDDIO *Table 7: Pin muxing*: PB[6] was clk_out_div5, is now clk_out_div256 Removed PB[4] and PB[5] rows In the A[3] row, changed ABS[2] to ABS[1] *Section 3.11: DC electrical characteristics*, added “Peripherals supply current (5 V and 3.3 V)” table *Table 14: EMI testing specifications*, removed all references to SAE Replaced both *Table 12: Thermal characteristics for 144-pin LQFP* and *Table 13: Thermal characteristics for 100-pin LQFP* *Table 30: PLLMRFM electrical specifications (V_{DDPLL} = 1.08 V to 1.32 V, V_{SS} = V_{SSPLL} = 0 V, TA = TL to TH)*, changed the max value of f_{SYS} from 120 to 64 *Table 33: Program and erase specifications*: Removed all TBC changed the initial max value of T_{BKPRG} (Code Flash) from 3.3 to 6.6 s changed the max value of T_{BKPRG} (Data Flash) from 1.9 to 4.1 s changed the max value of $T_{wprogram}$ (Data Flash) from 300 to 500 µs Added t_{ESRT} row *Table 17: Voltage regulator electrical characteristics*, updated $V_{DD\_LV\_REGCOR}$ values Updated *Table 18: Low voltage monitor electrical characteristics* Updated *Table 21: Supply current (5.0 V, NVUSRO[PAD3V5V]=0)* and *Table 23: Supply current (3.3 V, NVUSRO[PAD3V5V]=1)* Removed “NVUSRO[OSCILLATOR_MARGIN] field description” section. Removed orderable parts tables.