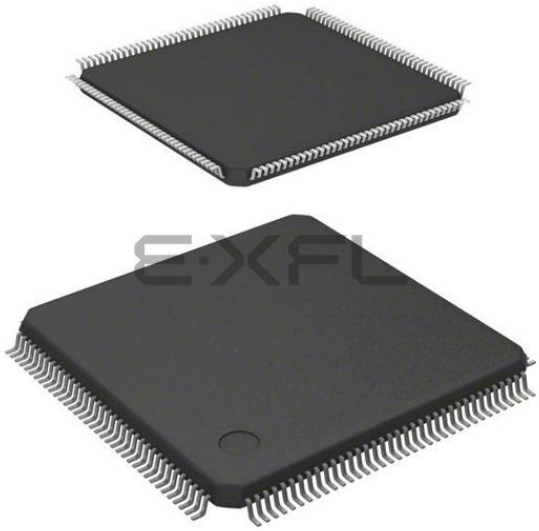

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 26x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p60l5cefay

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1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the SPC56xP54x/SPC56xP60x series of microcontroller units (MCUs). It also describes the device features and highlights important electrical and physical characteristics. For functional characteristics, refer to the device reference manual.

1.2 Description

This 32-bit system-on-chip (SoC) automotive microcontroller family is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address chassis applications specifically the airbag application.

This family is one of a series of next-generation integrated automotive microcontrollers based on the Power Architecture technology.

The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category. It operates up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

1.3 Device comparison

Table 2 provides a summary of different members of the SPC56xP54x/SPC56xP60x family and their features—relative to Full-featured version—to enable a comparison among the family members and an understanding of the range of functionality offered within this family.

Table 2. SPC56xP54x/SPC56xP60x device comparison

Feature	SPC560P54	SPC560P60	SPC56AP54	SPC56AP60
Code Flash memory (with ECC)	768 KB	1 MB	768 KB	1 MB
Data Flash / EE (with ECC)	64 KB			
SRAM (with ECC)	64 KB	80 KB	64 KB	80 KB
Processor core	32-bit e200z0h		32-bit Dual e200z0h	
Instruction set	VLE			
CPU performance	0-64 MHz			
FMPLL (frequency-modulated phase-locked loop) modules	1			
INTC (interrupt controller) channels	148			
PIT (periodic interrupt timer)	1 (includes four 32-bit timers)			

Table 2. SPC56xP54x/SPC56xP60x device comparison (continued)

Feature		SPC560P54	SPC560P60	SPC56AP54	SPC56AP60
Enhanced DMA (direct memory access) channels		16			
FlexRay		Yes (64 message buffer)			
FlexCAN (controller area network)		3(1),(2)			
Safety port		Yes (via third FlexCAN module)			
FCCU (fault collection and control unit)		Yes(3)			
CTU (cross triggering unit)		Yes			
eTimer channels		2 × 6			
FlexPWM (pulse-width modulation) channels		No			
Analog-to-digital converters (ADC)		One (10-bit, 27-channel)(4)			
LINFlex modules		2 (1 × Master/Slave, 1 × Master only)(5)			
DSPI (deserial serial peripheral interface) modules		5(6)			
CRC (cyclic redundancy check) units		2(7)			
JTAG interface		Yes			
Nexus port controller (NPC)		Yes (Level 2+)(8)			
Supply	Digital power supply(9)	3.3 V or 5 V single supply with external transistor			
	Analog power supply	3.3 V or 5 V			
	Internal RC oscillator	16 MHz			
	External crystal oscillator	4–40 MHz			
Packages		LQFP100 LQFP144			LQFP100 LQFP144 LQFP176(10)
Temperature	Standard ambient temperature	–40 to 125 °C			

1. Each FlexCAN module has 32 message buffers.
2. One FlexCAN module can act as a Safety Port with a bit rate as high as 7.5 Mbit/s.
3. Enhanced FCCU version.
4. Same amount of ADC channels as on SPC560P44/50 not considering the internally connected ones. 26 channels on LQFP144 and 16 channels on LQFP100.
5. LinFlex_1 is Master Only.
6. Increased number of CS for DSPI_1.
7. Upgraded specification with addition of 8-bits polynomial (CRC-8 VDA CAN) support and 3rd context.
8. Improved debugging capability with data trace capability and increased Nexus throughput available on emulation package.
9. 3.3 V range and 5 V range correspond to different orderable parts.
10. Software development package only. Not available for production.

The crossbar provides the following features:

- 6 master ports:
  - 2 e200z0 core complex Instruction ports
  - 2 e200z0 core complex Load/Store Data ports
  - eDMA
  - FlexRay
- 6 slave ports:
  - 2 Flash memory (code flash and data flash)
  - 2 SRAM (48 KB + 32 KB)
  - 2 PBRIDGE
- 32-bit internal address, 32-bit internal data paths
- Fixed Priority Arbitration based on Port Master
- Temporary dynamic priority elevation of masters

1.5.3 Enhanced direct memory access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is utilized to minimize the overall block size.

The eDMA module provides the following features:

- 16 channels support independent 8, 16 or 32-bit single value or block transfers
- Supports variable sized queues and circular queues
- Source and destination address registers are independently configured to post-increment or remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- DMA transfers possible between system memories, DSPIs, ADC, eTimer and CTU
- Programmable DMA Channel Multiplexer for assignment of any DMA source to any available DMA channel with up to 30 potential request sources
- eDMA abort operation through software

1.5.4 On-chip flash memory with ECC

The SPC56xP54x/SPC56xP60x provides up to 1024 KB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used for instruction and/or data storage. The flash memory module interfaces the system bus to a dedicated flash memory array controller. It supports a 32-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains a four-entry, 4x128-bit prefetch buffers. Prefetch buffer hits allow no-wait responses. Normal flash memory array accesses are registered and are forwarded to the system bus on the following cycle, incurring 2 wait states.

  - Watchpoint triggering, watchpoint triggers program tracing
  - DDR
- Auxiliary Output Port
  - 4 MDO (Message Data Out) pins
  - MCKO (Message Clock Out) pin
  - 2 $\overline{\text{MSEO}}$ (Message Start/End Out) pins
  - $\overline{\text{EVTO}}$ (Event Out) pin
- Auxiliary Input Port
  - $\overline{\text{EVTI}}$ (Event In) pin[a]

1.5.28 IEEE 1149.1 (JTAG) controller

The JTAG controller (JTAGC) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE standard.

The JTAG controller provides the following features:

- IEEE Test Access Port (TAP) interface with four pins (TDI, TMS, TCK, TDO)
- Selectable modes of operation include JTAGC/debug or normal system operation.
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD
- A 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC, ACCESS_AUX_TAP_CORE0, ACCESS_AUX_TAP_CORE1, ACCESS_AUX_TAP_NASPS_0, ACCESS_AUX_TAP_NASPS_1
- Three test data registers: a bypass register, a boundary scan register, and a device identification register.
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry.

1.5.29 On-chip voltage regulator (VREG)

The on-chip voltage regulator module provides the following features:

- Uses external NPN transistor
- Regulates external 3.3 V to 5.0 V down to 1.2 V for the core logic
- Low voltage detection on the internal 1.2 V and I/O voltage 3.3 V

a. At least one TCK clock is necessary for the EVTI signal to be recognized by the MCU.

Table 6. System pins (continued)

Symbol	Description	Direction	Pad Speed[1]		Pin		
			SRC=0	SRC=1	LQFP 100	LQFP 144	LQFP 176[2]
MDO5	Nexus Message Data Output—line 5	Output Only	Fast		—	—	8
MDO6	Nexus Message Data Output—line 6	Output Only	Fast		—	—	9
MDO7	Nexus Message Data Output—line 7	Output Only	Fast		—	—	110
MDO8	Nexus Message Data Output—line 8	Output Only	Fast		—	—	111
MDO9	Nexus Message Data Output—line 9	Output Only	Fast		—	—	112
MDO10	Nexus Message Data Output—line 10	Output Only	Fast		—	—	166
MDO11	Nexus Message Data Output—line 11	Output Only	Fast		—	—	171
RDY	Nexus ready output	Output Only	—	—	—	—	172
NMI	Non-Maskable Interrupt	Input Only	—	—	1	1	1
XTAL	Analog output of the oscillator amplifier circuit. Needs to be grounded if oscillator is used in bypass mode.	—	—	—	18	29	37
EXTAL	Analog input of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode.	—	—	—	19	30	38
TMS[3]	JTAG state machine control	Input Only	—	—	59	87	105
TCK[3]	JTAG clock	Input Only	—	—	60	88	106
TDI[3]	JTAG data input	Input Only	—	—	58	86	104
TDO[3]	JTAG data output	Output Only	—	—	61	89	107
Reset pin							
$\overline{\text{RESET}}$[4]	Bidirectional reset with Schmitt trigger characteristics and noise filter	Bidirectional	Medium	—	20	31	39
Test pin							
$V_{PP\ TEST}$	Pin for testing purpose only. To be tied to ground in normal operating mode.	—	—	—	74	107	131
V_{REG_BYPASS}	Pin for testing purpose only. To be tied to ground in normal operating mode.	—	—	—	34	51	59

1. SRC values refer to the value assigned to the Slew Rate Control bits of the pad configuration register.

Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
B[9]	PCR[25]	ALT0 ALT1 ALT2 ALT3 —	GPIO[25] — — — AN[11]	SIUL — — — ADC_0	Input Only	—	—	35	52	60
B[10]	PCR[26]	ALT0 ALT1 ALT2 ALT3 —	GPIO[26] — — — AN[12]	SIUL — — — ADC_0	Input Only	—	—	36	53	61
B[11]	PCR[27]	ALT0 ALT1 ALT2 ALT3 —	GPIO[27] — — — AN[13]	SIUL — — — ADC_0	Input Only	—	—	37	54	62
B[12]	PCR[28]	ALT0 ALT1 ALT2 ALT3 —	GPIO[28] — — — AN[14]	SIUL — — — ADC_0	Input Only	—	—	38	55	63
B[13]	PCR[29]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[29] — — — AN[16] RXD	SIUL — — — ADC_0 LINFlex_1	Input Only	—	—	42	60	68
B[14]	PCR[30]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[30] — — — AN[17] ETC[4] EIRQ[19]	SIUL — — — ADC_0 eTimer_0 SIUL	Input Only	—	—	44	64	76
B[15]	PCR[31]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[31] — — — AN[18] EIRQ[20]	SIUL — — — ADC_0 SIUL	Input Only	—	—	43	62	70

Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
C[15]	PCR[47]	ALT0 ALT1 ALT2 ALT3 —	GPIO[47] CA_TR_EN ETC[0] — EXT_IN	SIUL FlexRay_0 eTimer_1 — CTU_0	I/O O I/O — I	Slow	Symmetric	85	124	148
Port D										
D[0]	PCR[48]	ALT0 ALT1 ALT2 ALT3	GPIO[48] CA_TX ETC[1] —	SIUL FlexRay_0 eTimer_1 —	I/O O I/O —	Slow	Symmetric	86	125	149
D[1]	PCR[49]	ALT0 ALT1 ALT2 ALT3 —	GPIO[49] CS4_1 ETC[2] EXT_TRG CA_RX	SIUL DSPI_1 eTimer_1 CTU_0 FlexRay_0	I/O O I/O O I	Slow	Medium	3	3	3
D[2]	PCR[50]	ALT0 ALT1 ALT2 ALT3 —	GPIO[50] CS5_1 ETC[3] — CB_RX	SIUL DSPI_1 eTimer_1 — FlexRay_0	I/O O I/O — I	Slow	Medium	97	140	168
D[3]	PCR[51]	ALT0 ALT1 ALT2 ALT3	GPIO[51] CB_TX ETC[4] —	SIUL FlexRay_0 eTimer_1 —	I/O O I/O —	Slow	Symmetric	89	128	152
D[4]	PCR[52]	ALT0 ALT1 ALT2 ALT3	GPIO[52] CB_TR_EN ETC[5] —	SIUL FlexRay_0 eTimer_1 —	I/O O I/O —	Slow	Symmetric	90	129	153
D[5]	PCR[53]	ALT0 ALT1 ALT2 ALT3	GPIO[53] CS3_0 — SOUT_3	SIUL DSPI_0 — DSPI_3	I/O O — O	Slow	Medium	22	33	41
D[6]	PCR[54]	ALT0 ALT1 ALT2 ALT3	GPIO[54] CS2_0 SCK_3 SOUT_4	SIUL DSPI_0 DSPI_3 DSPI_4	I/O O I/O O	Slow	Medium	23	34	42

Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
Port E										
E[0]	PCR[64]	ALT0 ALT1 ALT2 ALT3 —	GPIO[64] — — — AN[21]	SIUL — — — ADC_0	Input Only	—	—	46	68	80
E[1]	PCR[65]	ALT0 ALT1 ALT2 ALT3 —	GPIO[65] — — — AN[4]	SIUL — — — ADC_0	Input Only	—	—	27	39	47
E[2]	PCR[66]	ALT0 ALT1 ALT2 ALT3 —	GPIO[66] — — — AN[5]	SIUL — — — ADC_0	Input Only	—	—	32	49	57
E[3]	PCR[67]	ALT0 ALT1 ALT2 ALT3 —	GPIO[67] — — — AN[6]	SIUL — — — ADC_0	Input Only	—	—	—	40	48
E[4]	PCR[68]	ALT0 ALT1 ALT2 ALT3 —	GPIO[68] — — — AN[7]	SIUL — — — ADC_0	Input Only	—	—	—	42	50
E[5]	PCR[69]	ALT0 ALT1 ALT2 ALT3 —	GPIO[69] — — — AN[8]	SIUL — — — ADC_0	Input Only	—	—	—	44	52
E[6]	PCR[70]	ALT0 ALT1 ALT2 ALT3 —	GPIO[70] — — — AN[9]	SIUL — — — ADC_0	Input Only	—	—	—	46	54

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using *Equation 3*:

Equation 3 $T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T= thermocouple temperature on top of the package (°C)

Ψ_{JT}= thermal characterization parameter (°C/W)

P_D= power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

3.5.1.1 References

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134 U.S.A.
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at jedec.org web site.

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2. G. Kromann, S. Shidore, and S. Addison, *Thermal Modeling of a PBGA for Air-Cooled Applications*, Electronic Packaging and Production, pp. 53-58, March 1998.

3. B. Joiner and V. Adams, *Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling*, Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

Table 17. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$V_{DD\_LV\_REGCOR}$	CC	P	Output voltage under maximum load run supply current configuration	Post-trimming	1.15	—	1.32	V
C_{DEC1}	SR	—	External decoupling/stability ceramic capacitor	BJT from *Table 16*. 3 capacitances (i.e. X7R or X8R capacitors) with nominal value of 10 µF	19.5	30	—	µF
				BJT BC817, one capacitance of 22 µF	14.3	22		µF
R_{REG}	SR	—	Resulting ESR of all three capacitors of C_{DEC1}	BJT from *Table 16*. 3x10 µF. Absolute maximum value between 100 kHz and 10 MHz	—	—	50	mΩ
			Resulting ESR of the unique capacitor C_{DEC1}	BJT BC817, 1x 22 µF. Absolute maximum value between 100 kHz and 10 MHz	10	—	40	mΩ
C_{DEC2}	SR	—	External decoupling/stability ceramic capacitor	4 capacitances (i.e. X7R or X8R capacitors) with nominal value of 440 nF	1200	1760	—	nF
C_{DEC3}	SR	—	External decoupling/stability ceramic capacitor on $V_{DD\_HV\_REG}$	3 capacitances (i.e. X7R or X8R capacitors) with nominal value of 10 µF; C_{DEC3} has to be equal or greater than C_{DEC1}	19.5	30	—	µF
L_{Reg}	SR	—	Resulting ESL of $V_{DD\_HV\_REG}$, BCTRL and $V_{DD\_LV\_CORx}$ pins	—	—	—	15	nH

3.8.2 Voltage monitor electrical characteristics

The device implements a Power On Reset module to ensure correct power-up initialization, as well as three low voltage detectors to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the 5.0V ± 10% range
- LVDLVCOR monitors low voltage digital power domain

2. “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self clocked mode.
3. Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.
4. f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.
5. This value is determined by the crystal manufacturer and board design.
6. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.
7. Proper PC board layout procedures must be followed to achieve specifications.
8. Values are obtained with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).
9. Short term jitter is measured on the clock rising edge at cycle n and cycle n+4.
10. This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this PLL, load capacitors should not exceed these limits.
11. This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
12. This value is true when operating at frequencies above 60 MHz, otherwise f_{CS} is 2% (above 64 MHz).
13. Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

3.14 16 MHz RC oscillator electrical characteristics

Table 31. 16 MHz RC oscillator electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
f_{RC}	P	RC oscillator frequency	T_A = 25 °C	—	16	—	MHz
Δ_{RCMVAR}	P	Fast internal RC oscillator variation over temperature and supply with respect to f_{RC} at T_A = 25 °C in high-frequency configuration	—	–6	—	6	%
$\Delta_{RCMTRIM}$	T	Post Trim Accuracy: The variation of the PTF(1) from the 16 MHz	T_A = 25 °C	–1	—	1	%
$\Delta_{RCMSTEP}$	T	Fast internal RC oscillator trimming step	T_A = 25 °C	—	1.6	—	%

1. PTF = Post Trimming Frequency: The frequency of the output clock after trimming at typical supply voltage and temperature

3.15 Analog-to-Digital converter (ADC) electrical characteristics

The device provides a 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

3.15.2 ADC conversion characteristics

Table 32. ADC conversion characteristics

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
V_{INAN}	SR	Analog input voltage[2]	—	$V_{SS\_HV\_AD}$ – 0.3	—	$V_{SS\_HV\_AD}$ + 0.3	V
f_{CK}	SR	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_clk[3] frequency)	—	3[4]	—	60	MHz
f_s	SR	Sampling frequency	—	—	—	1.53	MHz
t_{ADC_S}	D	Sample time[5]	f_{ADC} = 20 MHz, INPSAMP = 3	125	—	—	ns
			f_{ADC} = 9 MHz, INPSAMP = 255	—	—	28.2	µs
t_{ADC_C}	P	Conversion time[6]	f_{ADC} = 20 MHz[7], INPCMP = 1	0.650	—	—	µs
C_S[8]	D	ADC input sampling capacitance	—	—	—	2.5	pF
C_{P1}[8]	D	ADC input pin capacitance 1	—	—	—	3	pF
C_{P2}[8]	D	ADC input pin capacitance 2	—	—	—	1	pF
C_{P3}[8]	D	ADC input pin capacitance 3	—	—	—	1	pF
R_{SW1}[8]	D	Internal resistance of analog source	$V_{DD\_HV\_AD}$ = 5 V ±10%	—	—	0.6	kΩ
			$V_{DD\_HV\_AD}$ = 3.3 V ±10%	—	—	3	kΩ
R_{SW2}[8]	D	Internal resistance of analog source	$V_{DD\_HV\_AD}$ = 5 V ±10%	—	—	2.15	kΩ
			$V_{DD\_HV\_AD}$ = 3.3 V ±10%	—	—	3.6	kΩ
R_{AD}[8]	D	Internal resistance of analog source	—	—	—	2	kΩ
I_{INJ}	T	Input current injection	Current injection on one ADC input, different from the converted one. Remains within TUE spec.	–5	—	5	mA
INL	P	Integral Non Linearity	No overload	—	±1.5	—	LSB
DNL	P	Differential Non Linearity	No overload	–1.0	—	1.0	LSB
OFS	T	Offset error	—	—	±1	—	LSB
GNE	T	Gain error	—	—	±1	—	LSB
TUE	P	Total unadjusted error without current injection	16 precision channels	–2.5	—	2.5	LSB

Table 32. ADC conversion characteristics (continued)

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
TUE	T	Total unadjusted error with current injection	16 precision channels	–3	—	3	LSB
TUE	T	Total unadjusted error with current injection	10 standard channels	–4	—	4	LSB

1. V_{DD} = 3.3 V to 3.6 V / 4.5 V to 5.5 V, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified and analog input voltage from $V_{SS\_HV\_AD}$ to $V_{DD\_HV\_AD}$.
2. V_{INAN} may exceed V_{SS_ADC} and V_{DD_ADC} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.
3. AD_clk clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
4. When configured to allow 60 MHz ADC, the minimum ADC clock speed is 9 MHz, below which precision is lost.
5. During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC_S}. After the end of the sample time t_{ADC_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC_S} depend on programming.
6. This parameter includes the sample time t_{ADC_S}.
7. 20 MHz ADC clock. Specific prescaler is programmed on MC_PLL_CLK to provide 20 MHz clock to the ADC.
8. See *Figure 16*.

3.16 Flash memory electrical characteristics

Table 33. Program and erase specifications

Symbol		Parameter	Conditions	Value				Unit
				Min	Typ[1]	Initial max[2]	Max[3]	
$T_{wprogram}$	P	Word Program (32 bits) Time[4]	Data Flash	—	30	70	500	µs
$T_{dwprogram}$	P	Double Word (64 bits) Program Time[4]	Code Flash	—	18	50	500	µs
T_{BKPRG}	P	Bank Program (64 KB)[4, 5]	Data Flash	—	0.49	1.2	4.1	s
	P	Bank Program (1056 KB)[4, 5]	Code Flash	—	2.6	6.6	66	s
T_{MDPRG}	P	Module Program (512 KB)[4]	Code Flash	—	1.3	1.65	33	s
$T_{16kpperase}$	P	16 KB Block Pre-program and Erase Time	Code Flash	—	200	500	5000	ms
			Data Flash		700	800		
$T_{32kpperase}$	P	32 KB Block Pre-program and Erase Time	Code Flash	—	300	600	5000	ms
$T_{64kpperase}$	P	64 KB Block Pre-program and Erase Time	Code Flash	—	400	900	5000	ms
$T_{128kpperase}$	P	128 KB Block Pre-program and Erase Time	Code Flash	—	600	1300	5000	ms
t_{ESRT}	P	Erase Suspend Request Rate[6]	Code Flash	20	—	—	—	ms
			Data Flash	10				

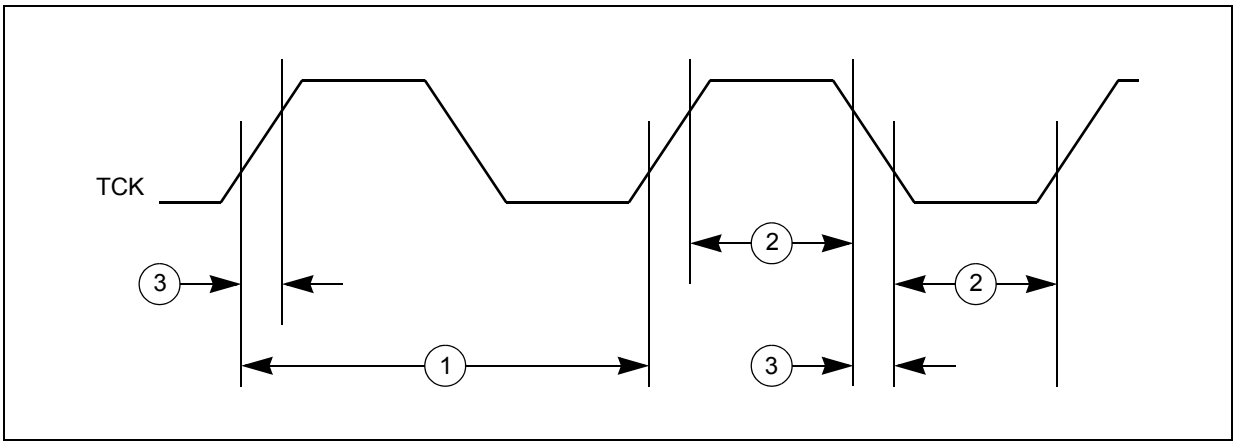
1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3.18.2 IEEE 1149.1 interface timing

Table 38. JTAG pin AC electrical characteristics

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	CC	D	TCK cycle time	—	100	—	ns
2	t_{JDC}	CC	D	TCK clock pulse width (measured at $V_{DD\_HV\_IOx}/2$)	—	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40% – 70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	—	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO data valid	—	—	40	ns
7	t_{TDOI}	CC	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	CC	D	TCK low to TDO high impedance	—	40	—	ns
9	t_{BSDV}	CC	D	TCK falling edge to output valid	—	—	50	ns
10	t_{BSDVZ}	CC	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
11	t_{BSDHZ}	CC	D	TCK falling edge to output high impedance	—	—	50	ns
12	t_{BSDST}	CC	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
13	t_{BSDHT}	CC	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

Figure 22. JTAG test clock input timing



4 Package characteristics

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.2 Package mechanical data

4.2.1 LQFP144 mechanical outline drawing

Figure 38. LQFP144 package mechanical drawing

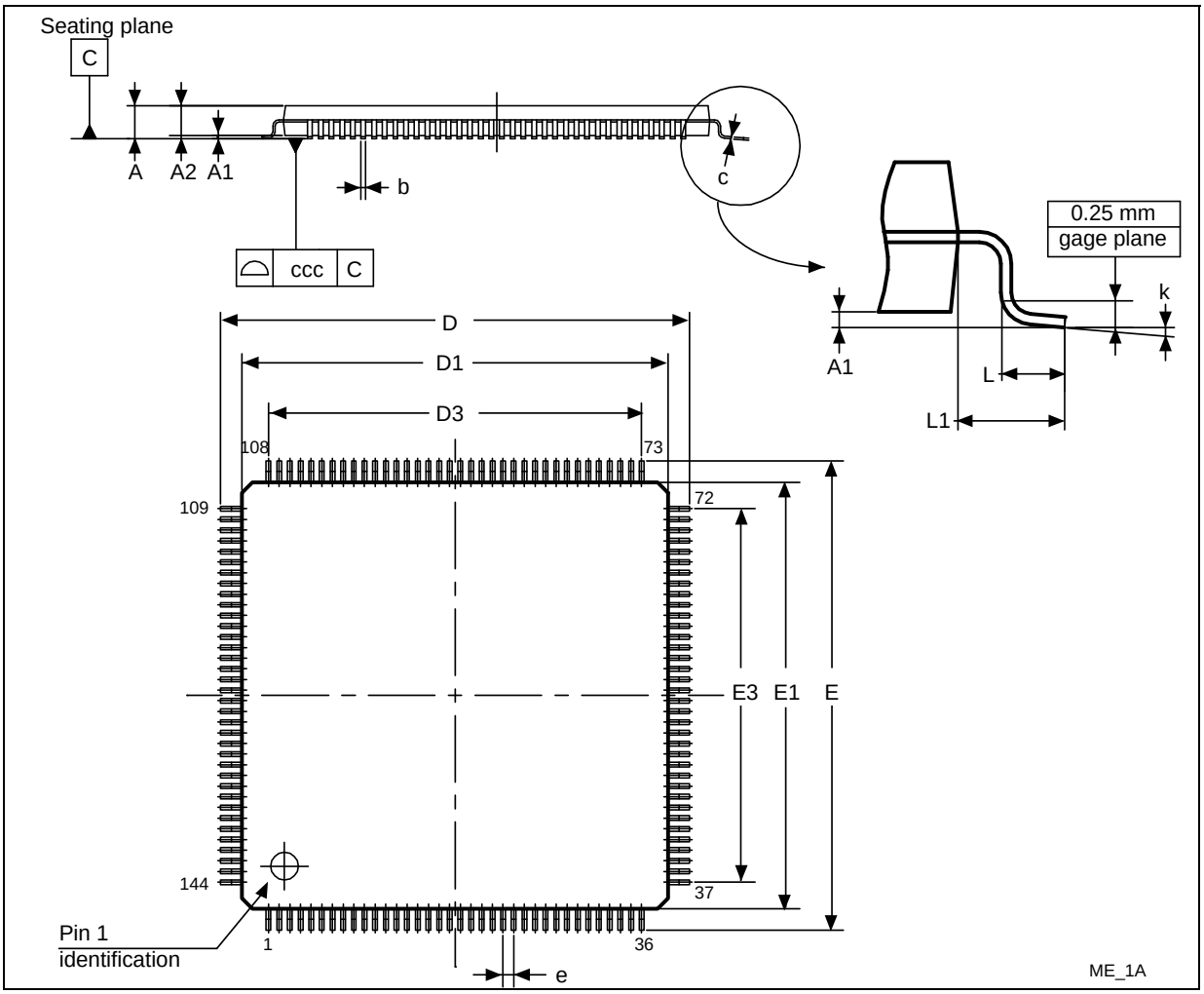


Table 42. LQFP144 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	—	17.500	—	—	0.6890	—
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	—	17.500	—	—	0.6890	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0°	3.5 °	0.0 °	7.0 °
ccc[2]	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Tolerance.

4.2.2 LQFP100 mechanical outline drawing

Figure 39. LQFP100 package mechanical drawing

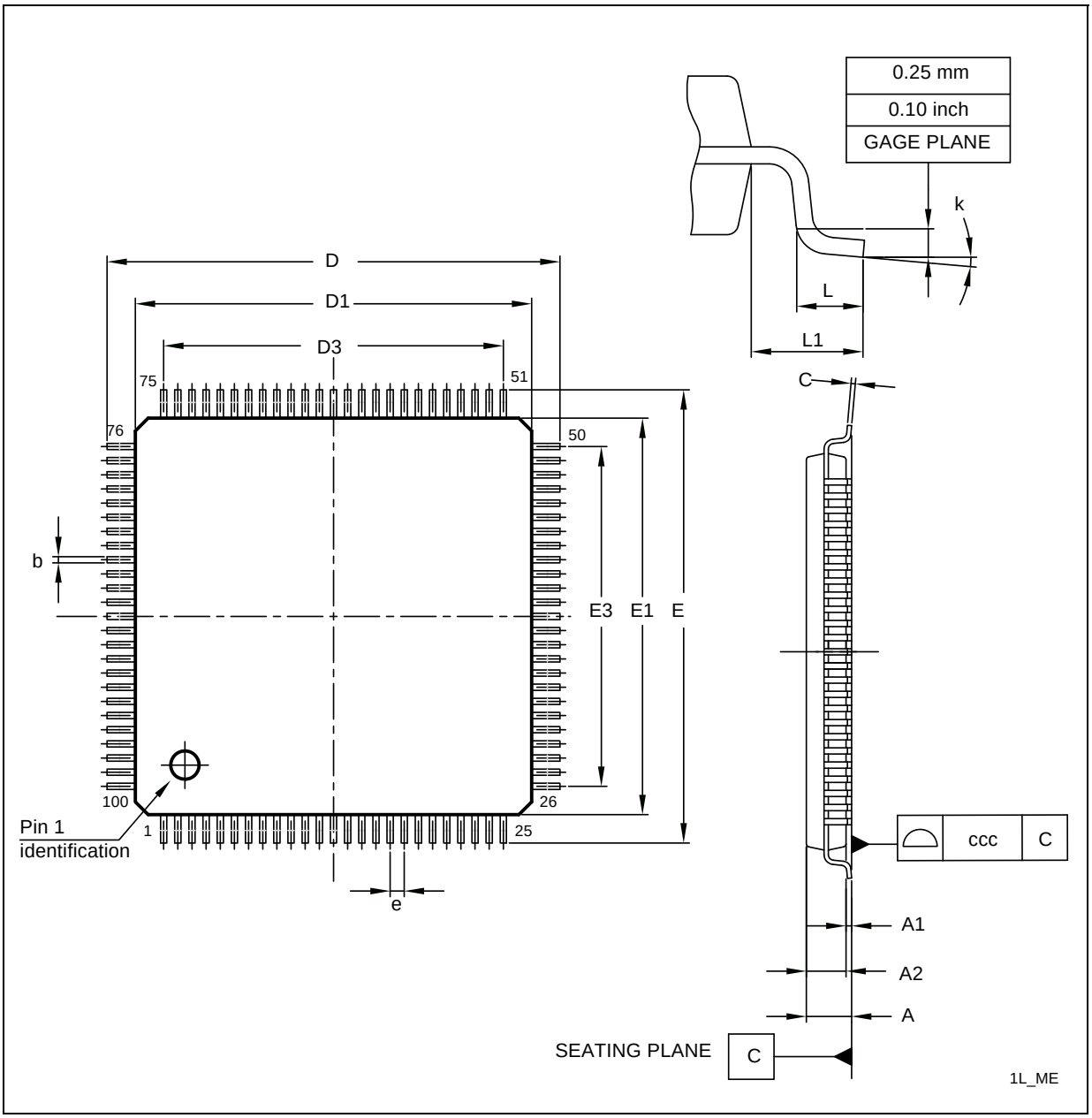


Table 43. LQFP100 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571

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