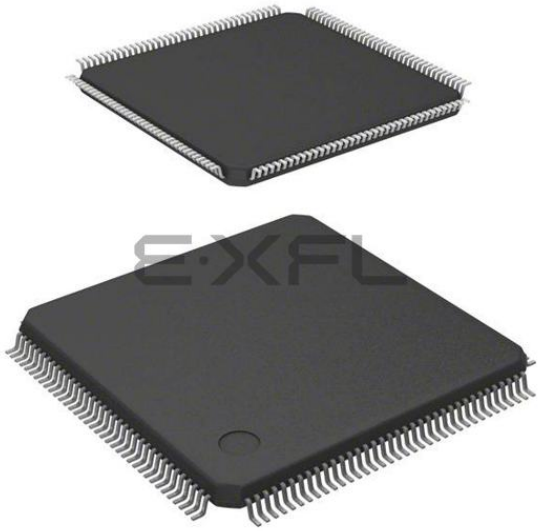

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 26x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc56ap54l5cefay

1.5 Feature details

1.5.1 High performance e200z0h core processor

The e200z0h Power Architecture core provides the following features:

- High performance e200z0 core processor for managing peripherals and interrupts
- Single issue 4-stage pipeline in-order execution 32-bit Power Architecture CPU
- Harvard architecture
- Variable length encoding (VLE), allowing mixed 16-bit and 32-bit instructions
  - Results in smaller code size footprint
  - Minimizes impact on performance
- Branch processing acceleration using lookahead instruction buffer
- Load/store unit
  - 1-cycle load latency
  - Misaligned access support
  - No load-to-use pipeline bubbles
- Thirty-two 32-bit general purpose registers (GPRs)
- Separate instruction bus and load/store bus Harvard architecture
- Hardware vectored interrupt support
- Reservation instructions for implementing read-modify-write constructs
- Long cycle time instructions, except for guarded loads, do not increase interrupt latency
- Extensive system development support through Nexus debug port
- Non maskable Interrupt support

1.5.2 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between six master ports and six slave ports. The crossbar supports a 32-bit address bus width and a 32-bit data bus width.

The crossbar allows for two concurrent transactions to occur from any master port to any slave port; but one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grant it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters are treated with equal priority and will be granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

The crossbar provides the following features:

- 6 master ports:
  - 2 e200z0 core complex Instruction ports
  - 2 e200z0 core complex Load/Store Data ports
  - eDMA
  - FlexRay
- 6 slave ports:
  - 2 Flash memory (code flash and data flash)
  - 2 SRAM (48 KB + 32 KB)
  - 2 PBRIDGE
- 32-bit internal address, 32-bit internal data paths
- Fixed Priority Arbitration based on Port Master
- Temporary dynamic priority elevation of masters

1.5.3 Enhanced direct memory access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is utilized to minimize the overall block size.

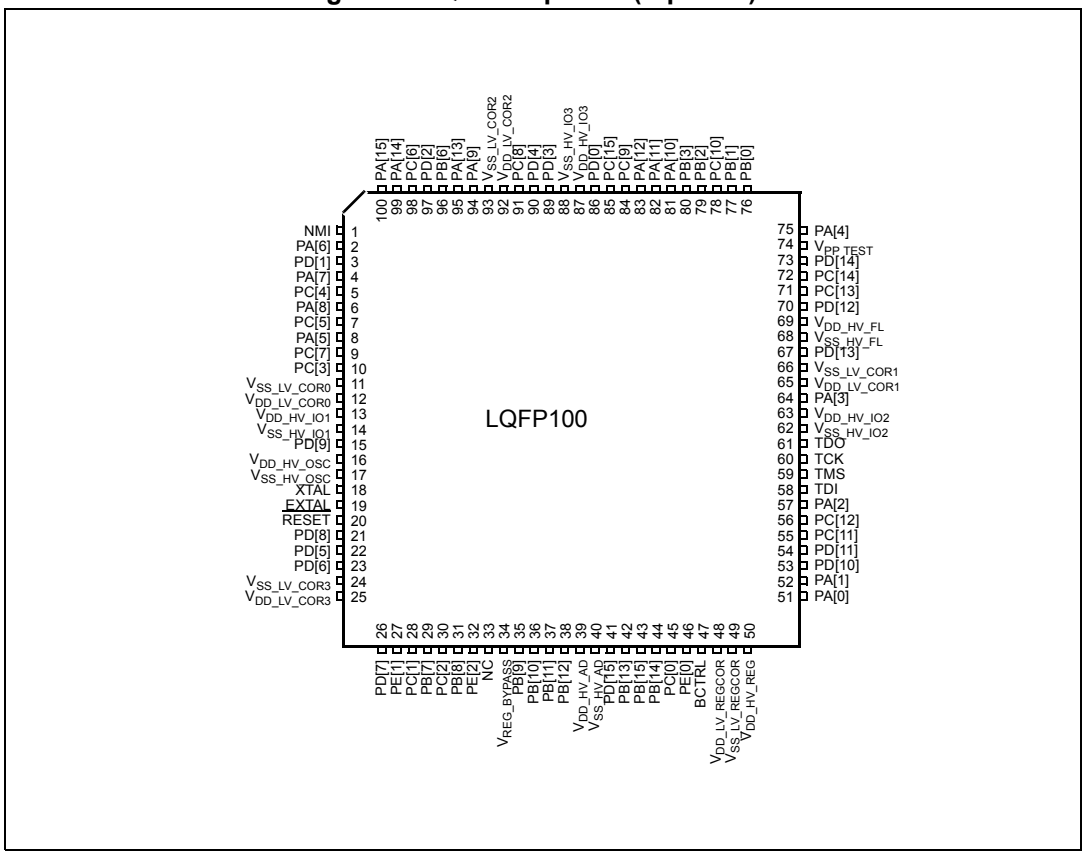
The eDMA module provides the following features:

- 16 channels support independent 8, 16 or 32-bit single value or block transfers
- Supports variable sized queues and circular queues
- Source and destination address registers are independently configured to post-increment or remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- DMA transfers possible between system memories, DSPIs, ADC, eTimer and CTU
- Programmable DMA Channel Multiplexer for assignment of any DMA source to any available DMA channel with up to 30 potential request sources
- eDMA abort operation through software

1.5.4 On-chip flash memory with ECC

The SPC56xP54x/SPC56xP60x provides up to 1024 KB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used for instruction and/or data storage. The flash memory module interfaces the system bus to a dedicated flash memory array controller. It supports a 32-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains a four-entry, 4x128-bit prefetch buffers. Prefetch buffer hits allow no-wait responses. Normal flash memory array accesses are registered and are forwarded to the system bus on the following cycle, incurring 2 wait states.

Figure 4. LQFP100 pinout (top view)[d]



2.2 Pin descriptions

The following sections provide signal descriptions and related information about the functionality and configuration of the SPC56xP54x/SPC56xP60x devices.

2.2.1 Power supply and reference voltage pins

Table 5 lists the power supply and reference voltage for the SPC56xP54x/SPC56xP60x devices.

Table 5. Supply pins

Supply		Pin		
Symbol	**Description**	**LQFP 100**	**LQFP 144**	**LQFP 176[1]**
VREG control and power supply pins				
BCTRL	Voltage regulator external NPN Ballast base control pin	47	69	81

d. Availability of port pin alternate functions depends on product selection.

Table 6. System pins (continued)

Symbol	Description	Direction	Pad Speed[1]		Pin		
			SRC=0	SRC=1	LQFP 100	LQFP 144	LQFP 176[2]
MDO5	Nexus Message Data Output—line 5	Output Only	Fast		—	—	8
MDO6	Nexus Message Data Output—line 6	Output Only	Fast		—	—	9
MDO7	Nexus Message Data Output—line 7	Output Only	Fast		—	—	110
MDO8	Nexus Message Data Output—line 8	Output Only	Fast		—	—	111
MDO9	Nexus Message Data Output—line 9	Output Only	Fast		—	—	112
MDO10	Nexus Message Data Output—line 10	Output Only	Fast		—	—	166
MDO11	Nexus Message Data Output—line 11	Output Only	Fast		—	—	171
RDY	Nexus ready output	Output Only	—	—	—	—	172
NMI	Non-Maskable Interrupt	Input Only	—	—	1	1	1
XTAL	Analog output of the oscillator amplifier circuit. Needs to be grounded if oscillator is used in bypass mode.	—	—	—	18	29	37
EXTAL	Analog input of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode.	—	—	—	19	30	38
TMS[3]	JTAG state machine control	Input Only	—	—	59	87	105
TCK[3]	JTAG clock	Input Only	—	—	60	88	106
TDI[3]	JTAG data input	Input Only	—	—	58	86	104
TDO[3]	JTAG data output	Output Only	—	—	61	89	107
Reset pin							
$\overline{\text{RESET}}$[4]	Bidirectional reset with Schmitt trigger characteristics and noise filter	Bidirectional	Medium	—	20	31	39
Test pin							
$V_{PP\ TEST}$	Pin for testing purpose only. To be tied to ground in normal operating mode.	—	—	—	74	107	131
V_{REG_BYPASS}	Pin for testing purpose only. To be tied to ground in normal operating mode.	—	—	—	34	51	59

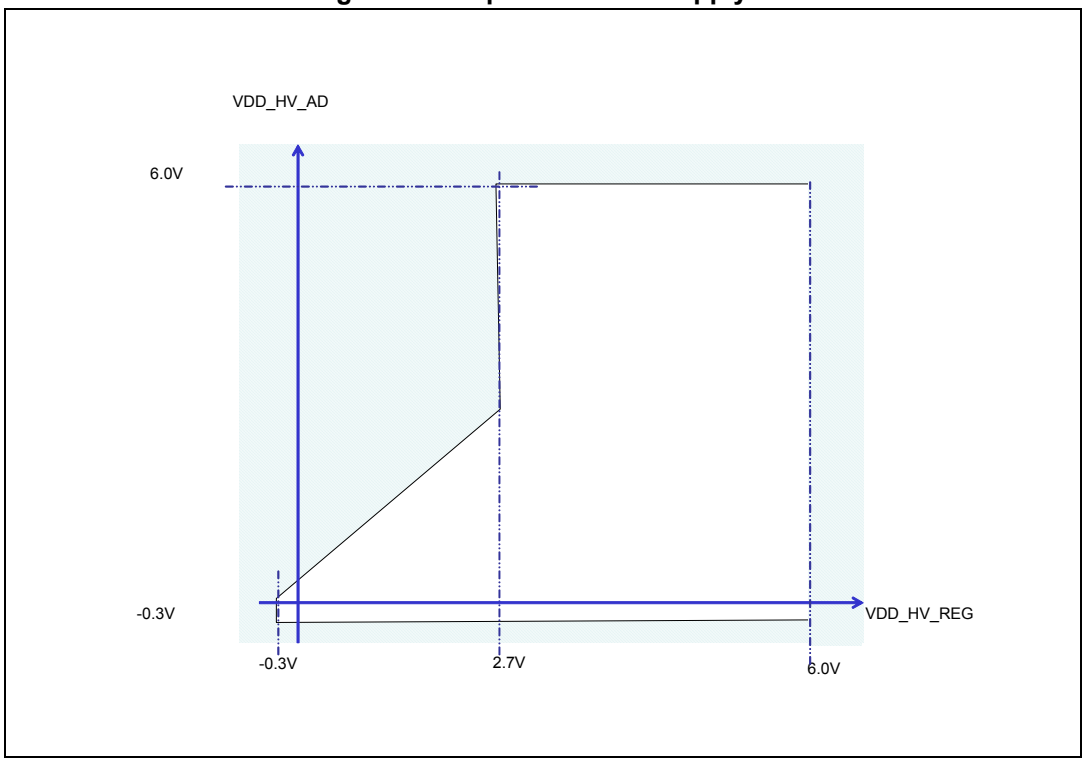
1. SRC values refer to the value assigned to the Slew Rate Control bits of the pad configuration register.

3.3 Absolute maximum ratings

Table 9. Absolute maximum ratings(1)

Symbol		Parameter	Conditions	Min	Max(2)	Unit
V_{SS_HV}	SR	Digital ground	—	0	0	V
$V_{DD\_HV\_IOx}$(3)	SR	3.3 V / 5.0 V input/output supply voltage with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
$V_{DD\_HV\_FL}$	SR	3.3 V / 5.0 V code and data flash memory supply voltage with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3	
$V_{SS\_HV\_FL}$	SR	Code and data flash memory ground with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
$V_{DD\_HV\_OSC}$	SR	3.3 V / 5.0 V crystal oscillator amplifier supply voltage with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3	
$V_{SS\_HV\_OSC}$	SR	3.3 V / 5.0 V crystal oscillator amplifier reference voltage with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
$V_{DD\_HV\_REG}$	SR	3.3 V / 5.0 V voltage regulator supply voltage with respect to ground (V_{SS_HV})	—	– 0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	– 0.3	$V_{DD\_HV\_IOx}$ + 0.3	
$V_{DD\_HV\_AD}$	SR	3.3 V / 5.0 V ADC supply and high reference voltage with respect to ground (V_{SS_HV})	$V_{DD\_HV\_REG}$ < 2.7 V	– 0.3	$V_{DD\_HV\_REG}$ + 0.3	V
			$V_{DD\_HV\_REG}$ > 2.7 V	– 0.3	6.0	
$V_{SS\_HV\_AD}$	SR	ADC ground and low reference voltage with respect to ground (V_{SS_HV})	—	–0.1	0.1	V
TV_{DD}	SR	Slope characteristics on all V_{DD} during power up(4) with respect to ground (V_{SS_HV})	—	3.0(5)	500 x 10^3 (0.5 [V/µs])	V/s
V_{IN}	SR	Voltage on any pin with respect to ground ($V_{SS\_HV\_IOx}$) with respect to ground (V_{SS_HV})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3	
V_{INAN}	SR	Analog input voltage	$V_{DD\_HV\_REG}$ < 2.7 V	$V_{SS\_HV\_AD}$ – 0.3	$V_{DD\_HV\_AD}$ + 0.3	V
			$V_{DD\_HV\_REG}$ > 2.7 V	$V_{SS\_HV\_AD}$	$V_{DD\_HV\_AD}$	V
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA

Figure 6. Independent ADC supply[e]



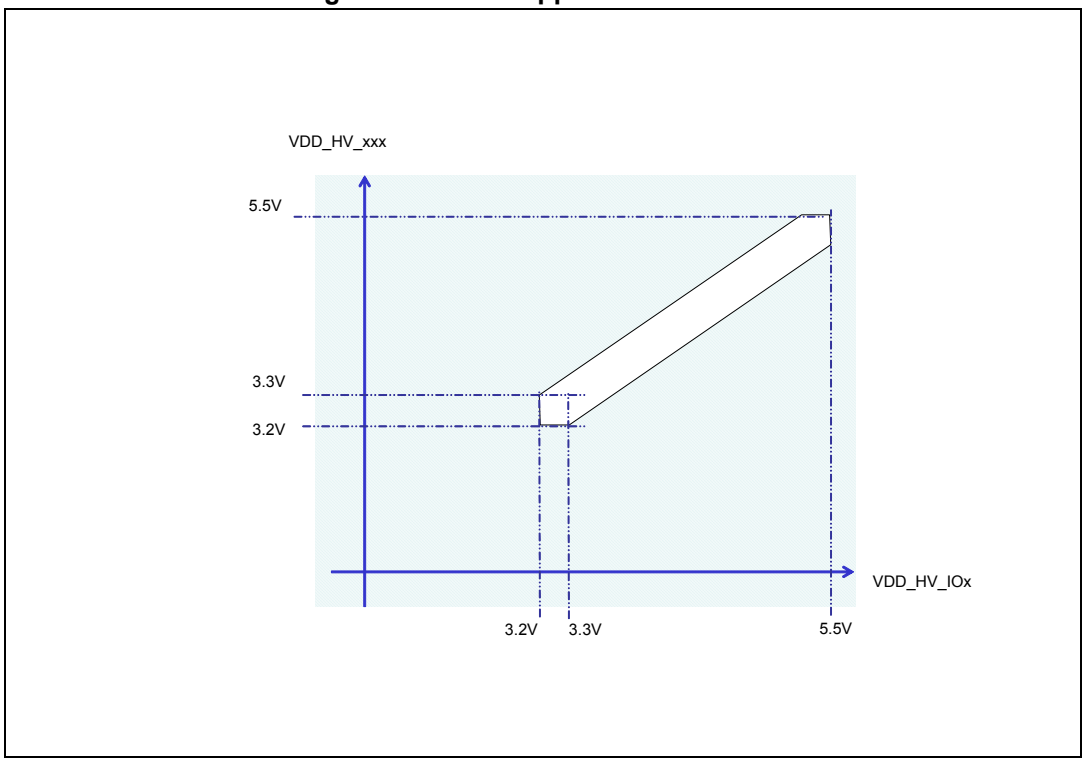
3.4 Recommended operating conditions

Table 10. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Min	Max[1]	Unit
V_{SS_HV}	SR	Digital ground	—	0	0	V
$V_{DD\_HV\_IOx}$[2]	SR	5.0 V input/output supply voltage	—	4.5	5.5	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_FL}$	SR	5.0 V code and data flash memory supply voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$ – 0.1	$V_{DD\_HV\_IOx}$ + 0.1	
$V_{SS\_HV\_FL}$	SR	Code and data flash memory ground	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	5.0 V crystal oscillator amplifier supply voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$ – 0.1	$V_{DD\_HV\_IOx}$ + 0.1	
$V_{SS\_HV\_OSC}$	SR	5.0 V crystal oscillator amplifier reference voltage	—	0	0	V

e. Device design targets the removal of this conditions. To be confirmed by design during device validation.

Figure 7. Power supplies constraints[f]



The SPC56xP54x/SPC56xP60x supply architecture provides an ADC supply that is managed independently of standard V_{DD_HV} supply. *Figure 8* shows the constraints of the ADC power supply.

f. IO AC and DC characteristics are guaranteed only in the range 3.0 V–3.6 V when PAD3V5V is low, and in the range 4.5 V–5.5 V when PAD3V5V is high.

Table 13. Thermal characteristics for 100-pin LQFP

Symbol		Parameter	Conditions	Typical value	Unit
$R_{\theta JA}$	D	Thermal resistance junction-to-ambient, natural convection(1)	Single layer board—1s	47.3	°C/W
	D		Four layer board—2s2p	35.6	°C/W
$R_{\theta JB}$	D	Thermal resistance junction-to-board(2)	Four layer board—2s2p	19.1	°C/W
$R_{\theta JCtop}$	D	Thermal resistance junction-to-case (top)(3)	Single layer board—1s	9.1	°C/W
Ψ_{JB}	D	Junction-to-board, natural convection(4)	Operating conditions	19.1	°C/W
Ψ_{JC}	D	Junction-to-case, natural convection(5)	Operating conditions	1.1	°C/W

1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-7. Thermal test board meets JEDEC specification for this package.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.
5. Thermal characterization parameter indicating the temperature difference between the case and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

3.5.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from *Equation 1*:

Equation 1 $T_J = T_A + (R_{\theta JA} \times P_D)$

where:

T_A= ambient temperature for the package (^oC)

$R_{\theta JA}$= junction to ambient thermal resistance ($^oC/W$)

P_D= power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in *Equation 2* as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

Equation 2 $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$= junction to case thermal resistance (°C/W)

$R_{\theta CA}$= case to ambient thermal resistance (°C/W)

Table 20. DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V]=0) (continued)

Symbol		Parameter	Conditions	Min	Max	Unit
I_{PU}	P	Equivalent pull-up current	$V_{IN} = V_{IL}$	–130	—	µA
			$V_{IN} = V_{IH}$	—	–10	
I_{PD}	P	Equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	µA
			$V_{IN} = V_{IH}$	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = –40 to 125 °C	–1	1	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_A = –40 to 125 °C	–0.5	0.5	µA
C_{IN}	D	Input capacitance	—	—	10	pF
I_{PU}	D	$\overline{\text{RESET}}$, equivalent pull-up current	$V_{IN} = V_{IL}$	–130	—	µA
			$V_{IN} = V_{IH}$	—	–10	
I_{PD}	D	$\overline{\text{RESET}}$, equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	µA
			$V_{IN} = V_{IH}$	—	130	

1. “SR” parameter values must not exceed the absolute maximum ratings shown in *Table 9*.

3.11.2 DC electrical characteristics (3.3 V)

Table 22 gives the DC electrical characteristics at 3.3 V (3.0 V < $V_{DD\_HV\_IOx}$ < 3.6 V, NVUSRO[PAD3V5V]=1) as described in *Figure 14*.

Figure 14. I/O input DC electrical characteristics definition

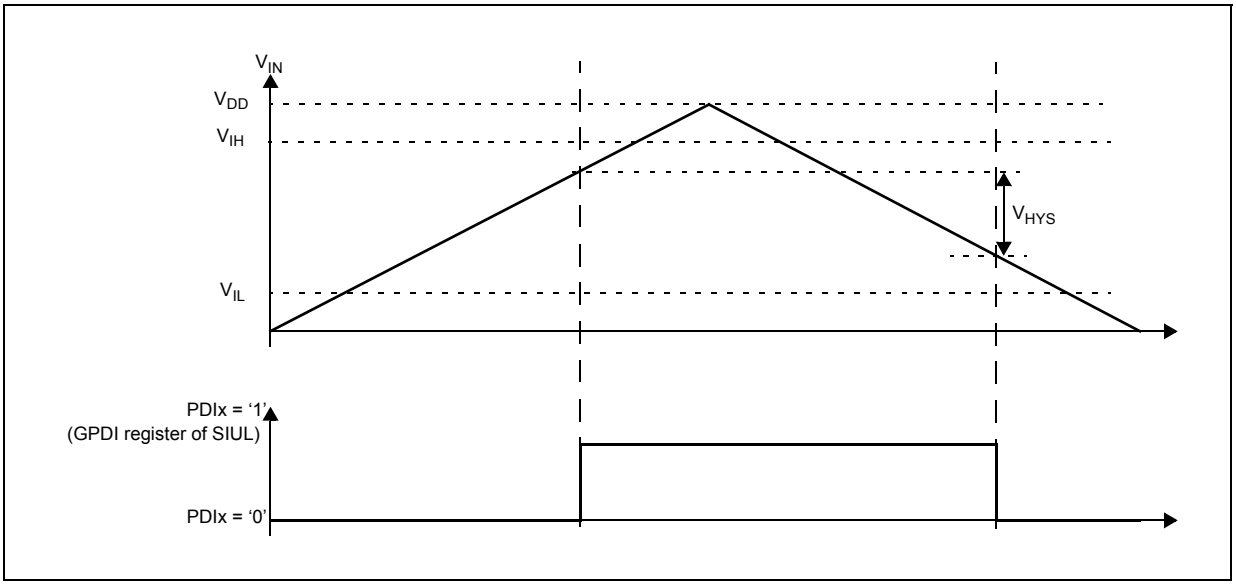
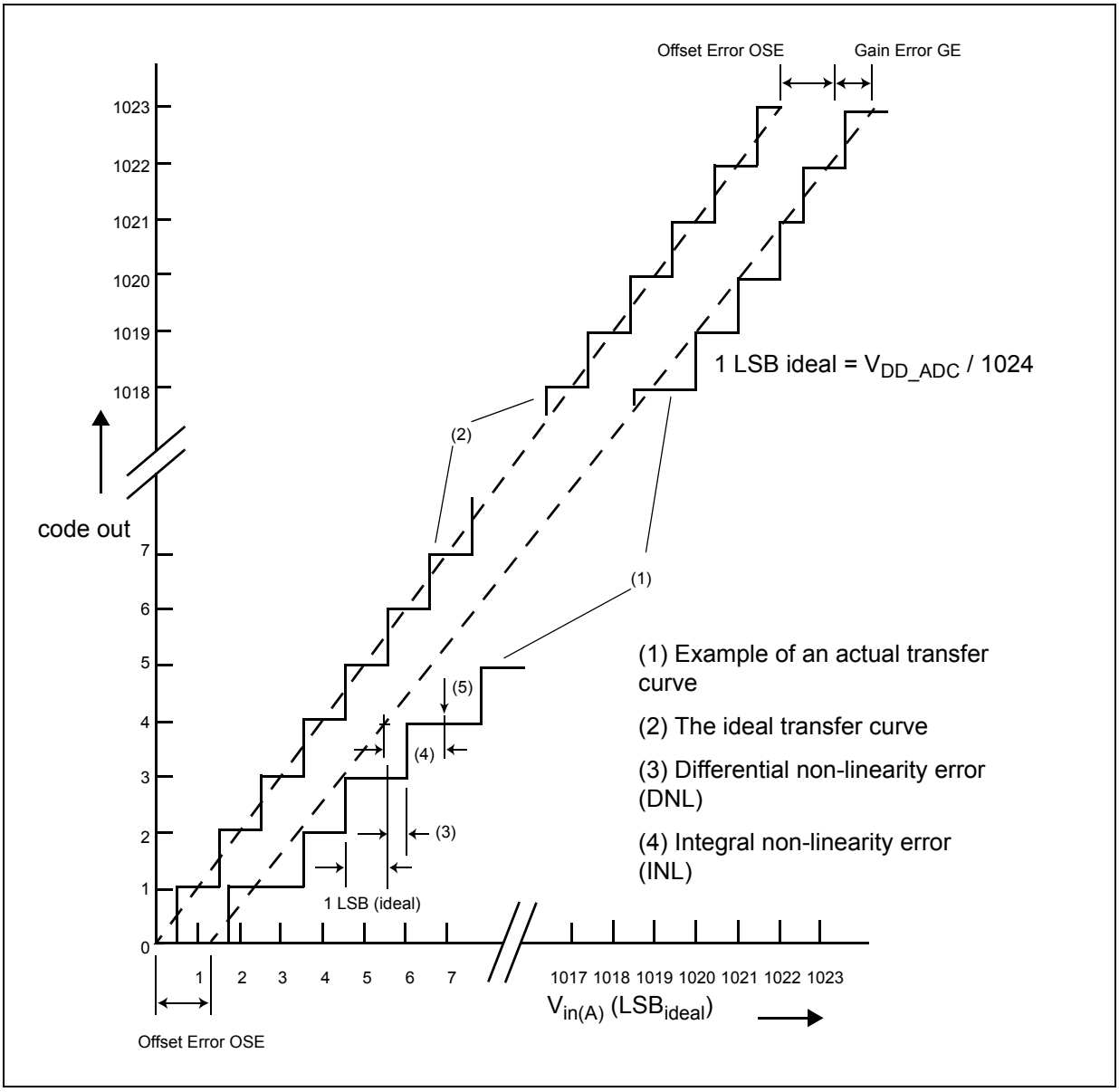


Table 22. DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V]=1)(1)

Symbol		Parameter	Conditions	Min	Max	Unit
V_{IL}	D	Minimum low level input voltage	—	–0.1(2)	—	V
V_{IL}	P	Maximum low level input voltage	—	—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IH}	P	Minimum high level input voltage	—	0.65 $V_{DD\_HV\_IOx}$	—	V
V_{IH}	D	Maximum high level input voltage	—	—	$V_{DD\_HV\_IOx}$ + 0.1(2)	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IOx}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 2 mA	—	0.5	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –2 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_F}	P	Fast, high level output voltage	I_{OL} = 11 mA	—	0.5	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –11 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_SYM}	P	Symmetric, high level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_SYM}	P	Symmetric, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
I_{PU}	P	Equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	

Figure 15. ADC characteristics and error definitions



3.15.1 Input impedance and ADC accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high-frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuate the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the source impedance value of the transducer or circuit supplying the analog signal to be measured.

The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

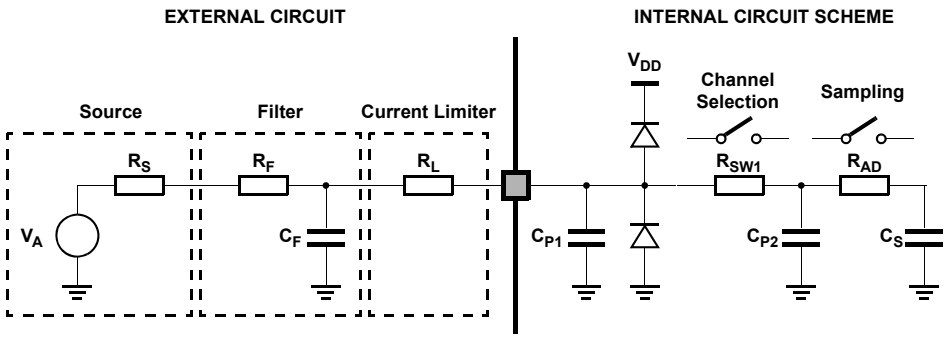
In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: being C_S and C_{P2} substantially two switched capacitances, with a frequency equal to the ADC conversion rate, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with $C_S + C_{P2}$ equal to 3 pF, a resistance of 330 kΩ is obtained ($R_{EQ} = 1 / (fc \times (C_S + C_{P2}))$, where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on $C_S + C_{P2}$) and the sum of $R_S + R_F$, the external circuit must be designed to respect the *Equation 4*:

Equation 4

$$V_A \times \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 4 generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

Figure 16. Input equivalent circuit (precise channels)



R_S Source Impedance

R_F Filter Resistance

C_F Filter Capacitance

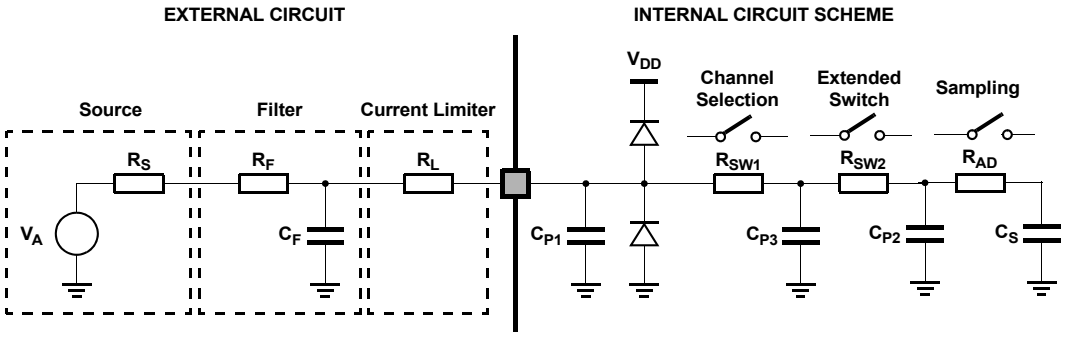
R_L Current Limiter Resistance

R_{SW1} Channel Selection Switch Impedance

R_{AD}Sampling Switch Impedance

C_P Pin Capacitance (two contributions, C_{P1} and C_{P2})

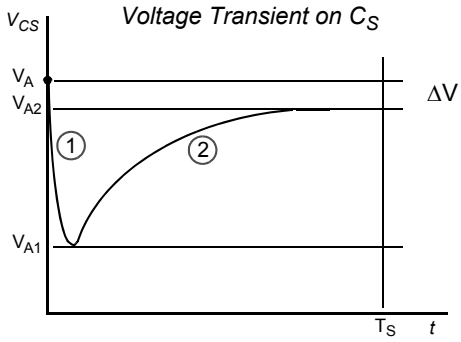
Figure 17. Input equivalent circuit (extended channels)



R_S: Source impedance
R_F: Filter resistance
C_F: Filter capacitance
R_L: Current limiter resistance
R_{SW1}: Channel selection switch impedance (two contributions, R_{SW1} and R_{SW2})
R_{AD}: Sampling switch impedance
C_P: Pin capacitance (two contributions, C_{P1}, C_{P2} and C_{P3})
C_S: Sampling capacitance

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in *Figure 16*): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

Figure 18. Transient behavior during sampling phase



$\Delta V < 0.5$ LSB

$\tau_1 < (R_{SW} + R_{AD})\, C_S << T_S$

$\tau_2 = R_L\,(C_S + C_{P1} + C_{P2})$

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Equation 5

$$\tau_1 = (R_{SW} + R_{AD}) \times \frac{C_P \times C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Equation 6

$$\tau_1 < (R_{SW} + R_{AD}) \times C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to *Equation 7*:

Equation 7

$$V_{A1} \times (C_S + C_{P1} + C_{P2}) = V_A \times (C_{P1} + C_{P2})$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Equation 8

$$\tau_2 < R_L \times (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraint on R_L sizing is obtained:

Equation 9

$$8.5 \times \tau_2 = 8.5 \times R_L \times (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. *Equation 10* must be respected (charge balance assuming now C_S already charged at V_{A1}):

Equation 10

$$V_{A2} \times (C_S + C_{P1} + C_{P2} + C_F) = V_A \times C_F + V_{A1} \times (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on

3.15.2 ADC conversion characteristics

Table 32. ADC conversion characteristics

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
V_{INAN}	SR	Analog input voltage[2]	—	$V_{SS\_HV\_AD}$ – 0.3	—	$V_{SS\_HV\_AD}$ + 0.3	V
f_{CK}	SR	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_clk[3] frequency)	—	3[4]	—	60	MHz
f_s	SR	Sampling frequency	—	—	—	1.53	MHz
t_{ADC_S}	D	Sample time[5]	f_{ADC} = 20 MHz, INPSAMP = 3	125	—	—	ns
			f_{ADC} = 9 MHz, INPSAMP = 255	—	—	28.2	µs
t_{ADC_C}	P	Conversion time[6]	f_{ADC} = 20 MHz[7], INPCMP = 1	0.650	—	—	µs
C_S[8]	D	ADC input sampling capacitance	—	—	—	2.5	pF
C_{P1}[8]	D	ADC input pin capacitance 1	—	—	—	3	pF
C_{P2}[8]	D	ADC input pin capacitance 2	—	—	—	1	pF
C_{P3}[8]	D	ADC input pin capacitance 3	—	—	—	1	pF
R_{SW1}[8]	D	Internal resistance of analog source	$V_{DD\_HV\_AD}$ = 5 V ±10%	—	—	0.6	kΩ
			$V_{DD\_HV\_AD}$ = 3.3 V ±10%	—	—	3	kΩ
R_{SW2}[8]	D	Internal resistance of analog source	$V_{DD\_HV\_AD}$ = 5 V ±10%	—	—	2.15	kΩ
			$V_{DD\_HV\_AD}$ = 3.3 V ±10%	—	—	3.6	kΩ
R_{AD}[8]	D	Internal resistance of analog source	—	—	—	2	kΩ
I_{INJ}	T	Input current injection	Current injection on one ADC input, different from the converted one. Remains within TUE spec.	–5	—	5	mA
INL	P	Integral Non Linearity	No overload	—	±1.5	—	LSB
DNL	P	Differential Non Linearity	No overload	–1.0	—	1.0	LSB
OFS	T	Offset error	—	—	±1	—	LSB
GNE	T	Gain error	—	—	±1	—	LSB
TUE	P	Total unadjusted error without current injection	16 precision channels	–2.5	—	2.5	LSB

Table 32. ADC conversion characteristics (continued)

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
TUE	T	Total unadjusted error with current injection	16 precision channels	–3	—	3	LSB
TUE	T	Total unadjusted error with current injection	10 standard channels	–4	—	4	LSB

1. V_{DD} = 3.3 V to 3.6 V / 4.5 V to 5.5 V, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified and analog input voltage from $V_{SS\_HV\_AD}$ to $V_{DD\_HV\_AD}$.
2. V_{INAN} may exceed V_{SS_ADC} and V_{DD_ADC} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.
3. AD_clk clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
4. When configured to allow 60 MHz ADC, the minimum ADC clock speed is 9 MHz, below which precision is lost.
5. During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC_S}. After the end of the sample time t_{ADC_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC_S} depend on programming.
6. This parameter includes the sample time t_{ADC_S}.
7. 20 MHz ADC clock. Specific prescaler is programmed on MC_PLL_CLK to provide 20 MHz clock to the ADC.
8. See *Figure 16*.

3.16 Flash memory electrical characteristics

Table 33. Program and erase specifications

Symbol		Parameter	Conditions	Value				Unit
				Min	Typ[1]	Initial max[2]	Max[3]	
$T_{wprogram}$	P	Word Program (32 bits) Time[4]	Data Flash	—	30	70	500	µs
$T_{dwprogram}$	P	Double Word (64 bits) Program Time[4]	Code Flash	—	18	50	500	µs
T_{BKPRG}	P	Bank Program (64 KB)[4, 5]	Data Flash	—	0.49	1.2	4.1	s
	P	Bank Program (1056 KB)[4, 5]	Code Flash	—	2.6	6.6	66	s
T_{MDPRG}	P	Module Program (512 KB)[4]	Code Flash	—	1.3	1.65	33	s
$T_{16kpperase}$	P	16 KB Block Pre-program and Erase Time	Code Flash	—	200	500	5000	ms
			Data Flash		700	800		
$T_{32kpperase}$	P	32 KB Block Pre-program and Erase Time	Code Flash	—	300	600	5000	ms
$T_{64kpperase}$	P	64 KB Block Pre-program and Erase Time	Code Flash	—	400	900	5000	ms
$T_{128kpperase}$	P	128 KB Block Pre-program and Erase Time	Code Flash	—	600	1300	5000	ms
t_{ESRT}	P	Erase Suspend Request Rate[6]	Code Flash	20	—	—	—	ms
			Data Flash	10				

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

Figure 36. DSPI modified transfer format timing — slave, CPHA = 1

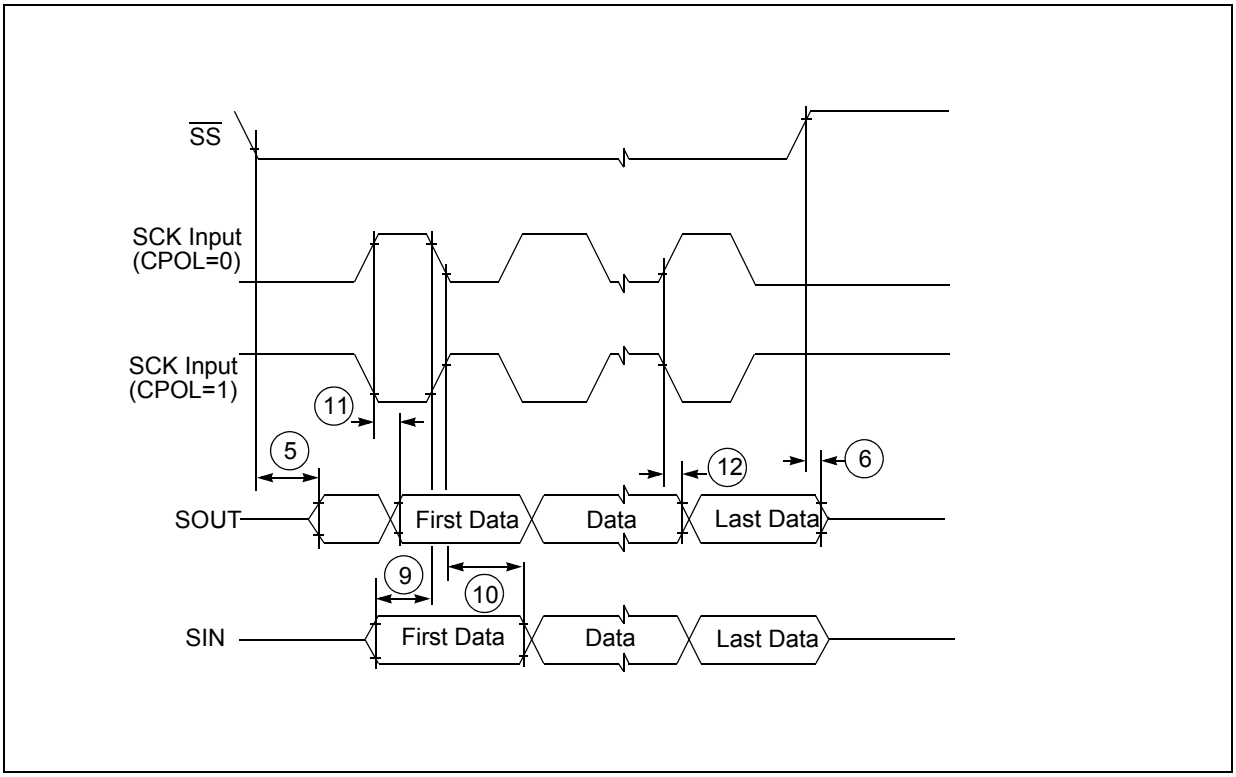
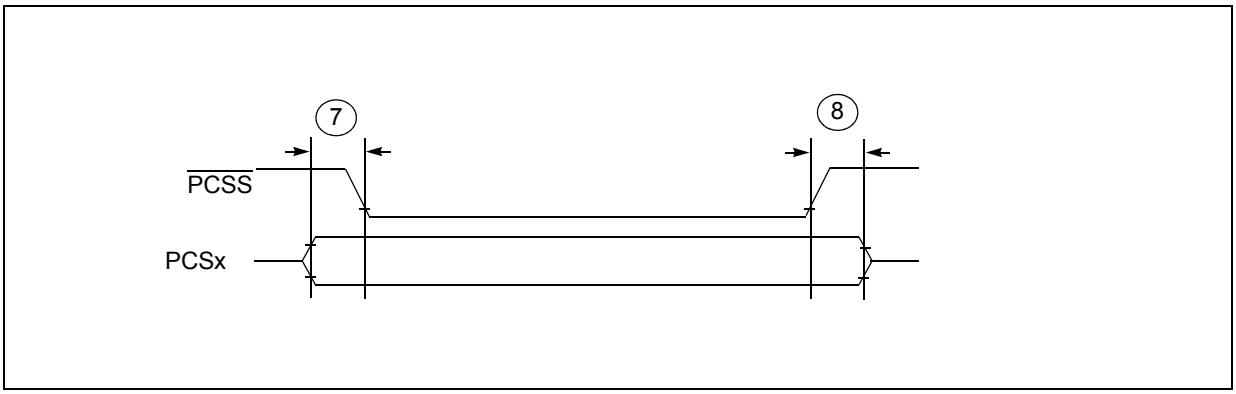


Figure 37. DSPI PCS strobe (PCSS) timing



4 Package characteristics

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.2 Package mechanical data

4.2.1 LQFP144 mechanical outline drawing

Figure 38. LQFP144 package mechanical drawing

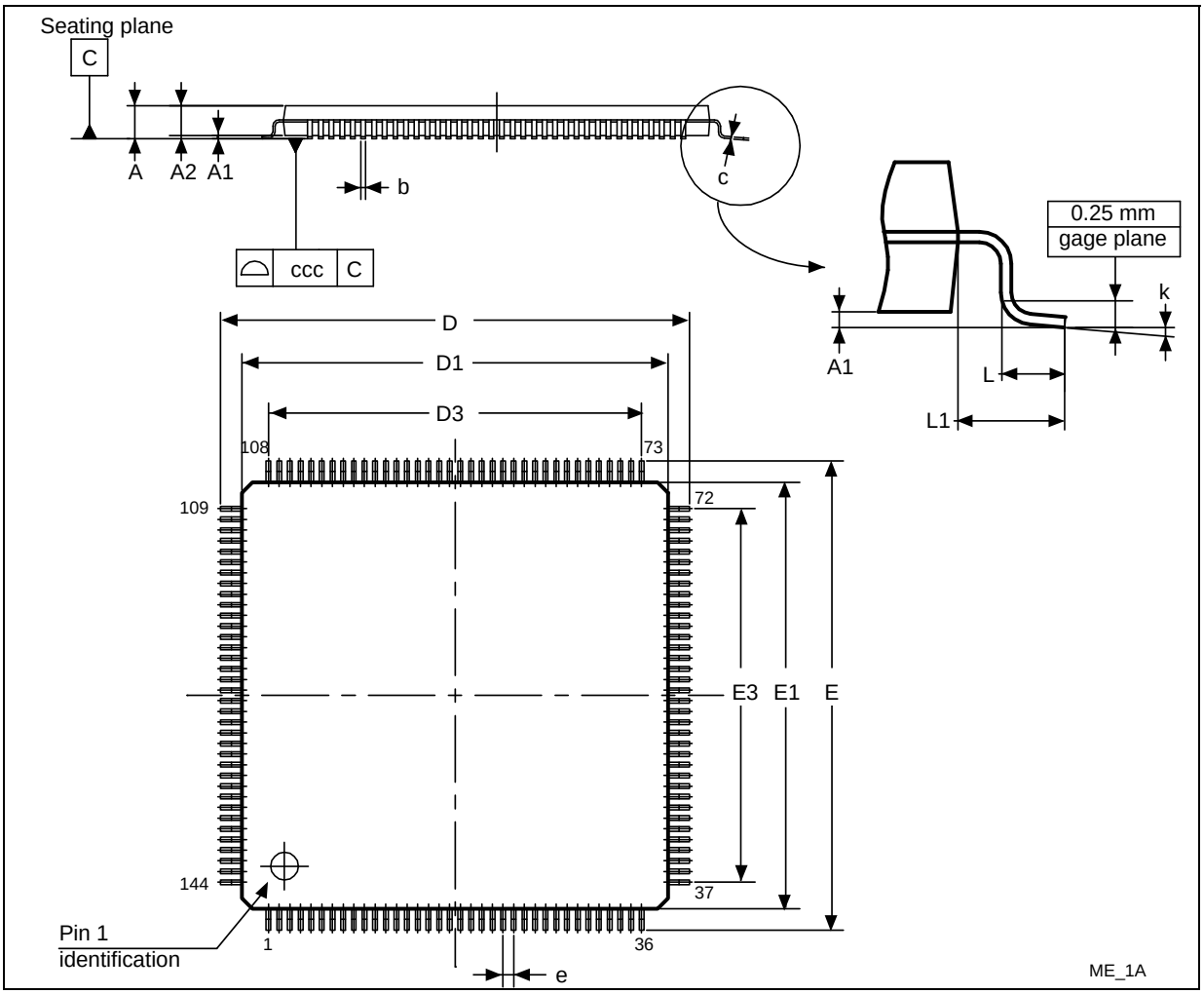


Table 42. LQFP144 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	—	17.500	—	—	0.6890	—
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	—	17.500	—	—	0.6890	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0°	3.5 °	0.0 °	7.0 °
ccc[2]	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Tolerance.

4.2.2 LQFP100 mechanical outline drawing

Figure 39. LQFP100 package mechanical drawing

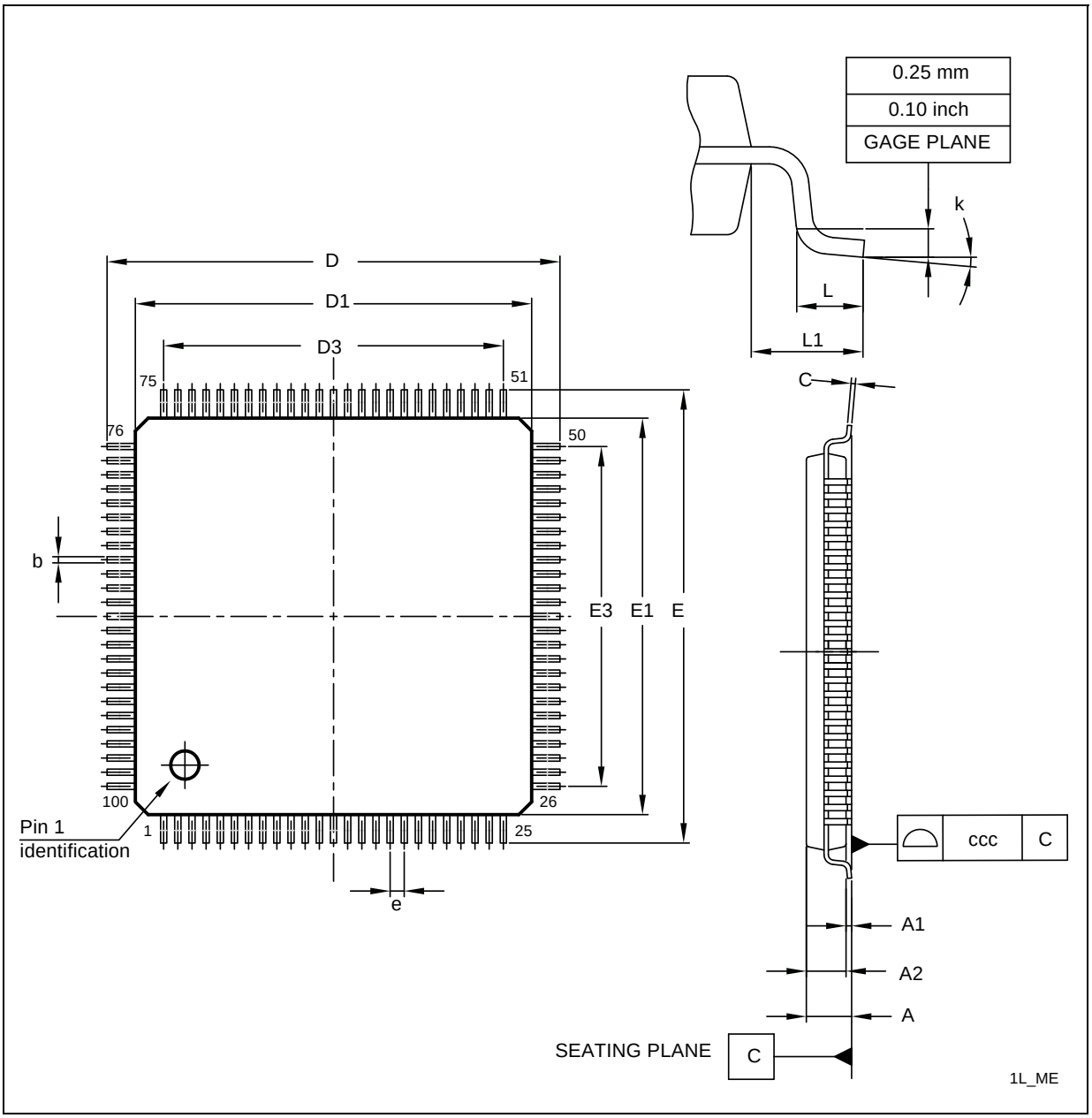


Table 43. LQFP100 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571