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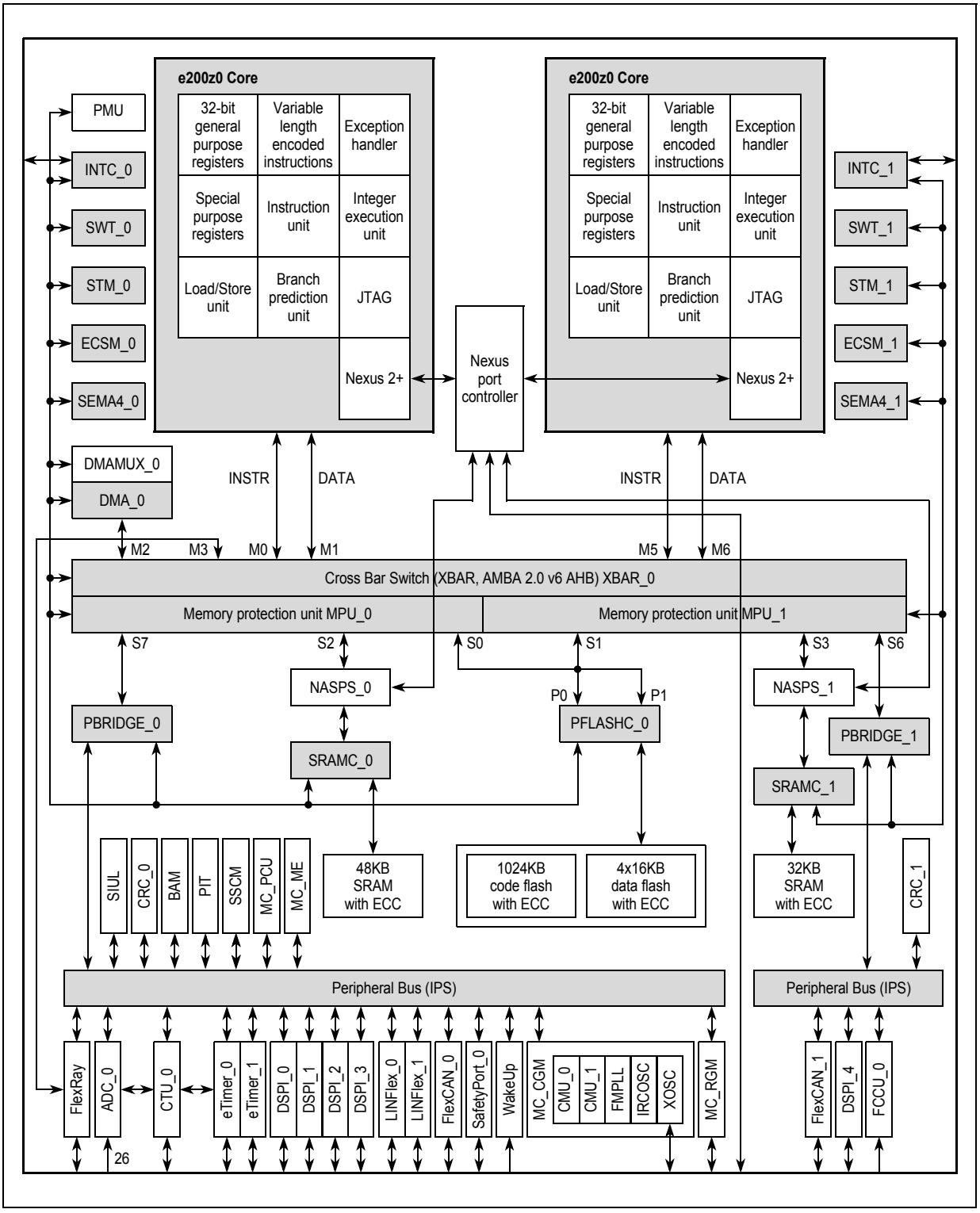
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	49
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc56ap60l3beaar

Figure 1. SPC56xP54x/SPC56xP60x block diagram



1.5 Feature details

1.5.1 High performance e200z0h core processor

The e200z0h Power Architecture core provides the following features:

- High performance e200z0 core processor for managing peripherals and interrupts
- Single issue 4-stage pipeline in-order execution 32-bit Power Architecture CPU
- Harvard architecture
- Variable length encoding (VLE), allowing mixed 16-bit and 32-bit instructions
  - Results in smaller code size footprint
  - Minimizes impact on performance
- Branch processing acceleration using lookahead instruction buffer
- Load/store unit
  - 1-cycle load latency
  - Misaligned access support
  - No load-to-use pipeline bubbles
- Thirty-two 32-bit general purpose registers (GPRs)
- Separate instruction bus and load/store bus Harvard architecture
- Hardware vectored interrupt support
- Reservation instructions for implementing read-modify-write constructs
- Long cycle time instructions, except for guarded loads, do not increase interrupt latency
- Extensive system development support through Nexus debug port
- Non maskable Interrupt support

1.5.2 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between six master ports and six slave ports. The crossbar supports a 32-bit address bus width and a 32-bit data bus width.

The crossbar allows for two concurrent transactions to occur from any master port to any slave port; but one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grant it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters are treated with equal priority and will be granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

The INTC provides the following features:

- Unique 9-bit vector for each separate interrupt source
- 8 software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority.
  - Modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources.
- 2 external high priority interrupts directly accessing the main core and IOP critical interrupt mechanism

The INTC module is replicated for each processor.

1.5.7 System clocks and clock generation

The following list summarizes the system clock and clock generation on the SPC56xP54x/SPC56xP60x:

- Lock detect circuitry continuously monitors lock status
- Loss of clock (LOC) detection for PLL outputs
- Programmable output clock divider (÷1, ÷2, ÷4, ÷8)
- Programmable output clock divider (÷1, ÷2, ÷3 to ÷256)
- eTimer module running at the same frequency as the e200z0h core
- On-chip oscillator with automatic level control
- Internal 16 MHz RC oscillator for rapid start-up and safe mode
  - Supports frequency trimming by user application

1.5.8 Frequency modulated phase-locked loop (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 40 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The FMPLL multiplication factor, output clock divider ratio are all software configurable.

The FMPLL has the following major features:

- Input clock frequency from 4 MHz to 40 MHz
- Voltage controlled oscillator (VCO) range from 256 MHz to 512 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- Modulation enabled/disabled through software

The default booting scheme is the one which uses the internal flash memory (an internal pull-down is used to select this mode). The alternate option allows the user to boot via FlexCAN or LINFlex (using the boot assist module software).

A censorship scheme is provided to protect the contents of the flash memory and offer increased security for the entire device.

A password mechanism is designed to grant the legitimate user access to the non-volatile memory.

1.5.16.1 Boot assist module (BAM)

The BAM is a block of read-only one-time programmed memory and is identical for all SPC56xP54x/SPC56xP60x devices that are based on the e200z0h core. The BAM program is executed every time the device is powered on if the alternate boot mode has been selected by the user.

The BAM provides the following features:

- Serial bootloading via FlexCAN or LINFlex.
- BAM can accept a password via the used serial communication channel to grant the legitimate user access to the non-volatile memory.

1.5.17 Error correction status module (ECSM)

The ECSM on this device features the following:

- Platform configuration and revision
- ECC error reporting for flash memory and SRAM
- ECC error injection for SRAM

The ECSM module is replicated for each processor.

1.5.18 FlexCAN

The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. FlexCAN module contains 32 message buffers.

The FlexCAN module provides the following features:

- Full implementation of the CAN protocol specification, Version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - 0 to 8 bytes data length
  - Programmable bit rate as fast as 1 Mbit/s
- 32 message buffers of 0 to 8 bytes data length
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- 3 programmable mask registers

Table 5. Supply pins (continued)

Supply		Pin		
Symbol	Description	LQFP 100	LQFP 144	LQFP 176[1]
$V_{SS\_LV\_COR0}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR0}$ pin.	11	17	25
$V_{DD\_LV\_COR1}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR1}$ pin.	65	93	117
$V_{SS\_LV\_COR1}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR1}$ pin.	66	94	118
$V_{DD\_LV\_COR2}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR2}$ pin.	92	131	155
$V_{SS\_LV\_COR2}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR\ 2}$ pin.	93	132	156
$V_{DD\_LV\_COR3}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR3}$ pin.	25	36	44
$V_{SS\_LV\_COR3}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR\ 3}$ pin.	24	35	43

1. LQFP176 available only as development package.
2. See datasheet Voltage Regulator Electrical Characteristics section for more details.

2.2.2 System pins

Table 6 and *Table 7* contain information on pin functions for the SPC56xP54x/SPC56xP60x devices. The pins listed in *Table 6* are single-function pins. The pins shown in *Table 7* are multi-function pins, programmable via their respective Pad Configuration Register (PCR) values.

Table 6. System pins

Symbol	Description	Direction	Pad Speed[1]		Pin		
			SRC=0	SRC=1	LQFP 100	LQFP 144	LQFP 176[2]
Dedicated pins							
MDO0	Nexus Message Data Output—line 0	Output Only	Fast		—	9	17
MDO4	Nexus Message Data Output—line 4	Output Only	Fast		—	—	7

Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
Port B										
B[0]	PCR[16]	ALT0 ALT1 ALT2 ALT3 —	GPIO[16] TXD ETC[2] DEBUG[0] EIRQ[15]	SIUL FlexCAN_0 eTimer_1 SSCM SIUL	I/O O I/O — I	Slow	Medium	76	109	133
B[1]	PCR[17]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[17] CS7_1 ETC[3] DEBUG[1] RXD EIRQ[16]	SIUL DSPI_1 eTimer_1 SSCM FlexCAN_0 SIUL	I/O O I/O — I I	Slow	Medium	77	110	134
B[2]	PCR[18]	ALT0 ALT1 ALT2 ALT3 —	GPIO[18] TXD SOUT_4 DEBUG[2] EIRQ[17]	SIUL LINFlex_0 DSPI_4 SSCM SIUL	I/O O I/O — I	Slow	Medium	79	114	138
B[3]	PCR[19]	ALT0 ALT1 ALT2 ALT3 —	GPIO[19] — SCK_4 DEBUG[3] RXD	SIUL — DSPI_4 SSCM LINFlex_0	I/O — I/O — I	Slow	Medium	80	116	140
B[6]	PCR[22]	ALT0 ALT1 ALT2 ALT3 —	GPIO[22] clk_out CS2_2 clk_out_div256 EIRQ[18]	SIUL MC_CGL DSPI_2 MC_CGL SIUL	I/O O O O I	Slow	Medium	96	138	162
B[7]	PCR[23]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[23] — — — AN[0] RXD	SIUL — — — ADC_0 LINFlex_0	Input Only	—	—	29	43	51
B[8]	PCR[24]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[24] — — — AN[1] ETC[5]	SIUL — — — ADC_0 eTimer_0	Input Only	—	—	31	47	55

Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
E[7]	PCR[71]	ALT0 ALT1 ALT2 ALT3 —	GPIO[71] — — — AN[10]	SIUL — — — ADC_0	Input Only	—	—	—	48	56
E[8]	PCR[72]	ALT0 ALT1 ALT2 ALT3 —	GPIO[72] — — — AN[22]	SIUL — — — ADC_0	Input Only	—	—	—	59	67
E[9]	PCR[73]	ALT0 ALT1 ALT2 ALT3 —	GPIO[73] — — — AN[23]	SIUL — — — ADC_0	Input Only	—	—	—	61	69
E[10]	PCR[74]	ALT0 ALT1 ALT2 ALT3 —	GPIO[74] — — — AN[24]	SIUL — — — ADC_0	Input Only	—	—	—	63	75
E[11]	PCR[75]	ALT0 ALT1 ALT2 ALT3 —	GPIO[75] — — — AN[25]	SIUL — — — ADC_0	Input Only	—	—	—	65	77
E[12]	PCR[76]	ALT0 ALT1 ALT2 ALT3 —	GPIO[76] — — — AN[26]	SIUL — — — ADC_0	Input Only	—	—	—	67	79
E[13]	PCR[77]	ALT0 ALT1 ALT2 ALT3 —	GPIO[77] SCK_3 — — EIRQ[25]	SIUL DSPI_3 — — SIUL	I/O I/O — — I	Slow	Medium	—	117	141
E[14]	PCR[78]	ALT0 ALT1 ALT2 ALT3 —	GPIO[78] SOUT_3 — — EIRQ[26]	SIUL DSPI_3 — — SIUL	I/O O — — I	Slow	Medium	—	119	143

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using *Equation 3*:

Equation 3 $T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T= thermocouple temperature on top of the package (°C)

Ψ_{JT}= thermal characterization parameter (°C/W)

P_D= power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

3.5.1.1 References

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134 U.S.A.
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at jedec.org web site.

1. C.E. Triplett and B. Joiner, *An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module*, Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.

2. G. Kromann, S. Shidore, and S. Addison, *Thermal Modeling of a PBGA for Air-Cooled Applications*, Electronic Packaging and Production, pp. 53-58, March 1998.

3. B. Joiner and V. Adams, *Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling*, Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

Table 17. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$V_{DD\_LV\_REGCOR}$	CC	P	Output voltage under maximum load run supply current configuration	Post-trimming	1.15	—	1.32	V
C_{DEC1}	SR	—	External decoupling/stability ceramic capacitor	BJT from *Table 16*. 3 capacitances (i.e. X7R or X8R capacitors) with nominal value of 10 µF	19.5	30	—	µF
				BJT BC817, one capacitance of 22 µF	14.3	22		µF
R_{REG}	SR	—	Resulting ESR of all three capacitors of C_{DEC1}	BJT from *Table 16*. 3x10 µF. Absolute maximum value between 100 kHz and 10 MHz	—	—	50	mΩ
			Resulting ESR of the unique capacitor C_{DEC1}	BJT BC817, 1x 22 µF. Absolute maximum value between 100 kHz and 10 MHz	10	—	40	mΩ
C_{DEC2}	SR	—	External decoupling/stability ceramic capacitor	4 capacitances (i.e. X7R or X8R capacitors) with nominal value of 440 nF	1200	1760	—	nF
C_{DEC3}	SR	—	External decoupling/stability ceramic capacitor on $V_{DD\_HV\_REG}$	3 capacitances (i.e. X7R or X8R capacitors) with nominal value of 10 µF; C_{DEC3} has to be equal or greater than C_{DEC1}	19.5	30	—	µF
L_{Reg}	SR	—	Resulting ESL of $V_{DD\_HV\_REG}$, BCTRL and $V_{DD\_LV\_CORx}$ pins	—	—	—	15	nH

3.8.2 Voltage monitor electrical characteristics

The device implements a Power On Reset module to ensure correct power-up initialization, as well as three low voltage detectors to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the 5.0V ± 10% range
- LVDLVCOR monitors low voltage digital power domain

Table 18. Low voltage monitor electrical characteristics

Symbol		Parameter	Conditions[1]	Value		Unit
				Min	Max	
V_{PORH}	T	Power-on reset threshold	—	1.5	2.7	V
V_{PORUP}	P	Supply for functional POR module	T_A = 25°C	1.0	—	V
$V_{REGLVDMOK\_H}$	P	Regulator low voltage detector high threshold	—	—	2.95	V
$V_{REGLVDMOK\_L}$	P	Regulator low voltage detector low threshold	—	2.6	—	V
$V_{FLLVDMOK\_H}$	P	Flash memory low voltage detector high threshold	—	—	2.95	V
$V_{FLLVDMOK\_L}$	P	Flash memory low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDMOK\_H}$	P	I/O low voltage detector high threshold	—	—	2.95	V
$V_{IOLVDMOK\_L}$	P	I/O low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDM5OK\_H}$	P	I/O 5V low voltage detector high threshold	—	—	4.4	V
$V_{IOLVDM5OK\_L}$	P	I/O 5V low voltage detector low threshold	—	3.8	—	V
$V_{MLVDDOK\_H}$	P	Digital supply low voltage detector high	—	—	1.15	V
$V_{MLVDDOK\_L}$	P	Digital supply low voltage detector low	—	1.08	—	V

1. V_{DD} = 3.3V ± 10% / 5.0V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified.

3.9 Power Up/Down sequencing

To prevent an overstress event or a malfunction within and outside the device, the SPC56xP54x/SPC56xP60x implements the following sequence to ensure each module is started only when all conditions for switching it ON are available:

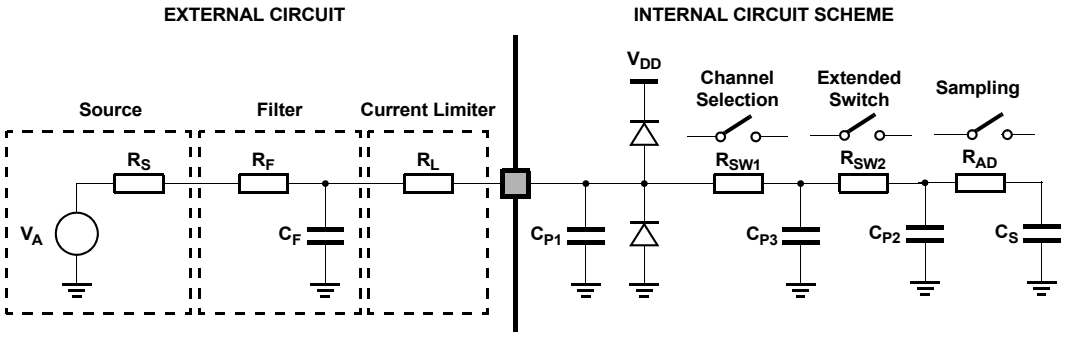
1. A POWER_ON module working on voltage regulator supply controls the correct start-up of the regulator. This is a key module ensuring safe configuration for all voltage regulator functionality when supply is below 1.5V. Associated POWER_ON (or POR) signal is active low.
   - Several low voltage detectors, working on voltage regulator supply monitor the voltage of the critical modules (voltage regulator, I/Os, flash memory and low voltage domain). LVDs are gated low when POWER_ON is active.
   - A POWER_OK signal is generated when all critical supplies monitored by the LVD are available. This signal is active high and released to all modules including I/Os, flash memory and RC16 oscillator needed during power-up phase and reset phase. When POWER_OK is low the associated modules are set into a safe state.

Table 24. Peripherals supply current (5 V and 3.3 V)(1)

Symbol		Parameter	Conditions		Value		Unit
					Typ	Max	
$I_{DD\_HV(CAN)}$	T	CAN (FlexCAN) supply current on VDD_HV_REG	500 Kbyte/s	Total (static + dynamic) consumption: – FlexCAN in loop-back mode – XTAL@ 8 MHz used as CAN engine clock source – Message sending period is 580 µs	21.6 * f_{periph}	28.1* f_{periph}	µA
$I_{DD\_HV(SCI)}$	T	SCI (LINFlex) supply current on VDD_HV_REG	Total (static + dynamic) consumption: – LIN mode – Baudrate: 115.2 Kbyte/s		10.8 * f_{periph}	14.1 * f_{periph}	
$I_{DD\_HV(SPI)}$	T	SPI (DSPI) supply current on VDD_HV_REG	Ballast dynamic consumption (continuous communication): – Baudrate: 2 Mbit/s – Transmission every 8 µs – Frame: 16 bits		4.8 * f_{periph}	6.3 * f_{periph}	
$I_{DD\_HV(ADC)}$	T	ADC supply current on VDD_HV_REG	VDD = 5.5 V	Ballast dynamic consumption (continuous conversion)	120 * f_{periph}	156 * f_{periph}	
$I_{DD\_HV\_ADC(ADC)}$	T	ADC supply current on VDD_HV_ADC	VDD = 5.5 V	Analog dynamic consumption (continuous conversion)	0.005 * f_{periph} + 2.8	0.007 * f_{periph} + 3.4	mA
$I_{DD\_HV(eTimer)}$	T	eTimer supply current on VDD_HV_REG	PWM signals generation on all 1 channel @10kHz	Dynamic consumption does not change varying the frequency	1.8	2.4	mA
$I_{DD\_HV(FlexRay)}$	T	FlexRay supply current on VDD_HV_REG	Static consumption		4.2 * f_{periph}	5.5 * f_{periph}	µA

1. Operating conditions: f_{periph} = 8 MHz to 64 MHz

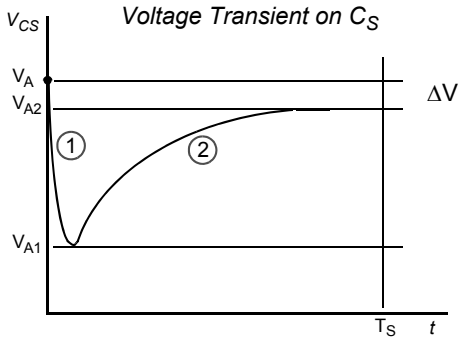
Figure 17. Input equivalent circuit (extended channels)



R_S: Source impedance
R_F: Filter resistance
C_F: Filter capacitance
R_L: Current limiter resistance
R_{SW1}: Channel selection switch impedance (two contributions, R_{SW1} and R_{SW2})
R_{AD}: Sampling switch impedance
C_P: Pin capacitance (two contributions, C_{P1}, C_{P2} and C_{P3})
C_S: Sampling capacitance

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in *Figure 16*): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

Figure 18. Transient behavior during sampling phase



$\Delta V < 0.5$ LSB

$\tau_1 < (R_{SW} + R_{AD})\, C_S << T_S$

$\tau_2 = R_L\,(C_S + C_{P1} + C_{P2})$

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Equation 5

$$\tau_1 = (R_{SW} + R_{AD}) \times \frac{C_P \times C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Equation 6

$$\tau_1 < (R_{SW} + R_{AD}) \times C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to *Equation 7*:

Equation 7

$$V_{A1} \times (C_S + C_{P1} + C_{P2}) = V_A \times (C_{P1} + C_{P2})$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Equation 8

$$\tau_2 < R_L \times (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraint on R_L sizing is obtained:

Equation 9

$$8.5 \times \tau_2 = 8.5 \times R_L \times (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. *Equation 10* must be respected (charge balance assuming now C_S already charged at V_{A1}):

Equation 10

$$V_{A2} \times (C_S + C_{P1} + C_{P2} + C_F) = V_A \times C_F + V_{A1} \times (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on

Table 32. ADC conversion characteristics (continued)

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
TUE	T	Total unadjusted error with current injection	16 precision channels	–3	—	3	LSB
TUE	T	Total unadjusted error with current injection	10 standard channels	–4	—	4	LSB

1. V_{DD} = 3.3 V to 3.6 V / 4.5 V to 5.5 V, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified and analog input voltage from $V_{SS\_HV\_AD}$ to $V_{DD\_HV\_AD}$.
2. V_{INAN} may exceed V_{SS_ADC} and V_{DD_ADC} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.
3. AD_clk clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
4. When configured to allow 60 MHz ADC, the minimum ADC clock speed is 9 MHz, below which precision is lost.
5. During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC_S}. After the end of the sample time t_{ADC_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC_S} depend on programming.
6. This parameter includes the sample time t_{ADC_S}.
7. 20 MHz ADC clock. Specific prescaler is programmed on MC_PLL_CLK to provide 20 MHz clock to the ADC.
8. See *Figure 16*.

3.16 Flash memory electrical characteristics

Table 33. Program and erase specifications

Symbol		Parameter	Conditions	Value				Unit
				Min	Typ[1]	Initial max[2]	Max[3]	
$T_{wprogram}$	P	Word Program (32 bits) Time[4]	Data Flash	—	30	70	500	µs
$T_{dwprogram}$	P	Double Word (64 bits) Program Time[4]	Code Flash	—	18	50	500	µs
T_{BKPRG}	P	Bank Program (64 KB)[4, 5]	Data Flash	—	0.49	1.2	4.1	s
	P	Bank Program (1056 KB)[4, 5]	Code Flash	—	2.6	6.6	66	s
T_{MDPRG}	P	Module Program (512 KB)[4]	Code Flash	—	1.3	1.65	33	s
$T_{16kpperase}$	P	16 KB Block Pre-program and Erase Time	Code Flash	—	200	500	5000	ms
			Data Flash		700	800		
$T_{32kpperase}$	P	32 KB Block Pre-program and Erase Time	Code Flash	—	300	600	5000	ms
$T_{64kpperase}$	P	64 KB Block Pre-program and Erase Time	Code Flash	—	400	900	5000	ms
$T_{128kpperase}$	P	128 KB Block Pre-program and Erase Time	Code Flash	—	600	1300	5000	ms
t_{ESRT}	P	Erase Suspend Request Rate[6]	Code Flash	20	—	—	—	ms
			Data Flash	10				

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3. The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
4. Actual hardware programming times. This does not include software overhead.
5. Typical bank programming time assumes that all cells are programmed in a single pulse. In reality some cells will require more than one pulse, adding a small overhead to total bank programming time (see Initial Max column).
6. Time between erase suspend resume and next erase suspend.

Table 34. Flash memory module life

Symbol		Parameter	Conditions	Value		Unit
				Min	Typ	
P/E	C	Number of program/erase cycles per block for 16 KB blocks over the operating temperature range (T_J)	—	100000	100000	cycles
P/E	C	Number of program/erase cycles per block for 32 KB blocks over the operating temperature range (T_J)	—	10000	100000	cycles
P/E	C	Number of program/erase cycles per block for 64 KB blocks over the operating temperature range (T_J)	—	10000	100000	cycles
P/E	C	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	—	1000	100000	cycles
Retention	C	Minimum data retention at 85 °C average ambient temperature(1)	Blocks with 0 – 1000 P/E cycles	20	—	years
			Blocks with 10000 P/E cycles	10	—	years
			Blocks with 100000 P/E cycles	5	—	years

1. Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

Table 35. Flash read access timing

Symbol	C	Parameter	Conditions(1)	Max	Unit
Fmax	C	Maximum working frequency for Code Flash at given number of WS in worst conditions	2 wait states	66	MHz
			0 wait states	22	
Fmax	C	Maximum working frequency for Data Flash at given number of WS in worst conditions	8 wait states	66	MHz

1. VDD = 3.3 V ± 10% / 5.0 V ± 10%, TA = –40 to 125 °C, unless otherwise specified.

Figure 20. Start-up reset requirements(g)

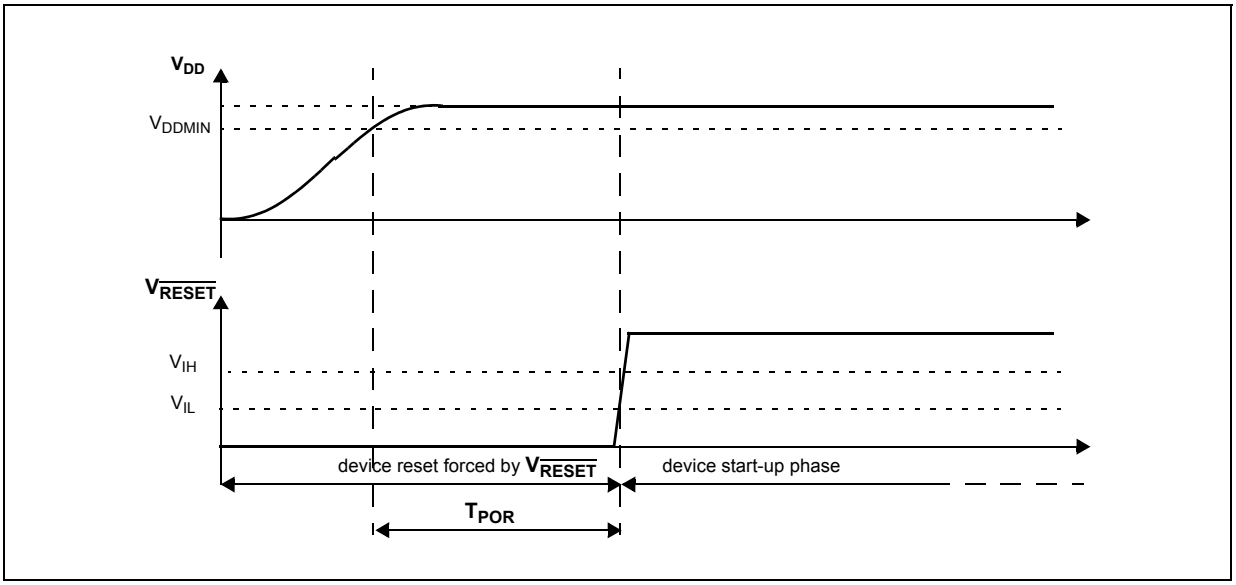
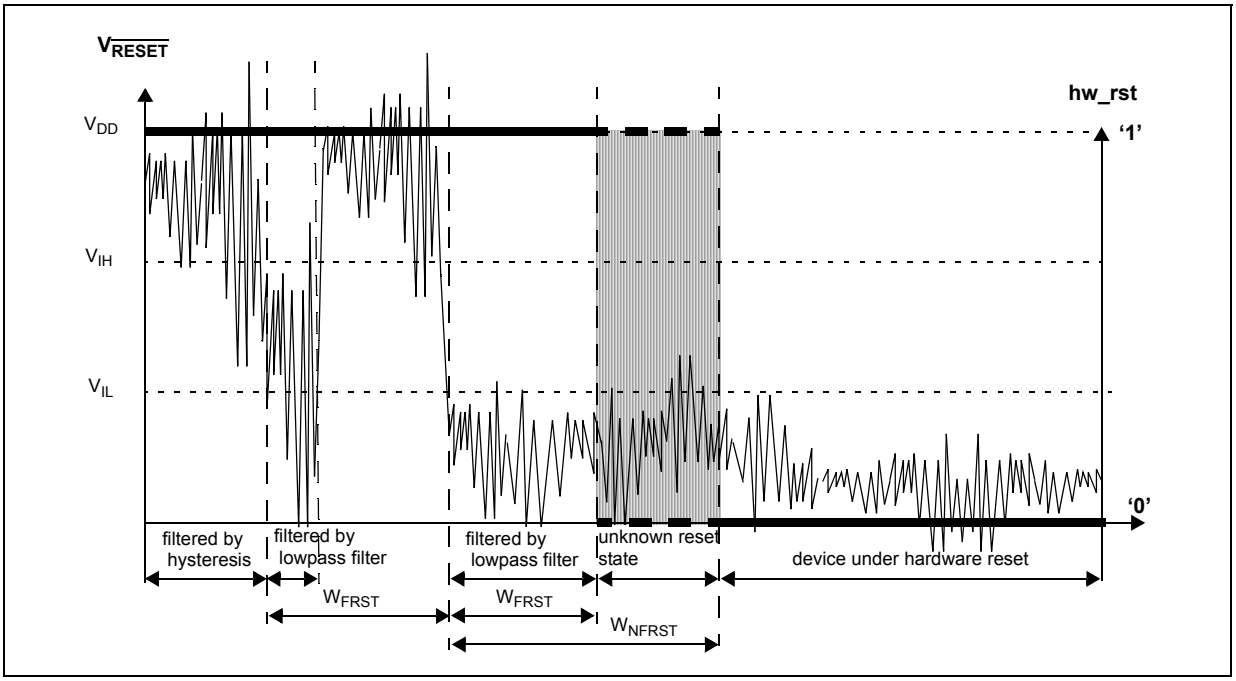


Figure 21. Noise filtering on reset signal



g. The output drive provided is open drain and hence must be terminated by an external resistor of value 1 kΩ.

Figure 23. JTAG test access port timing

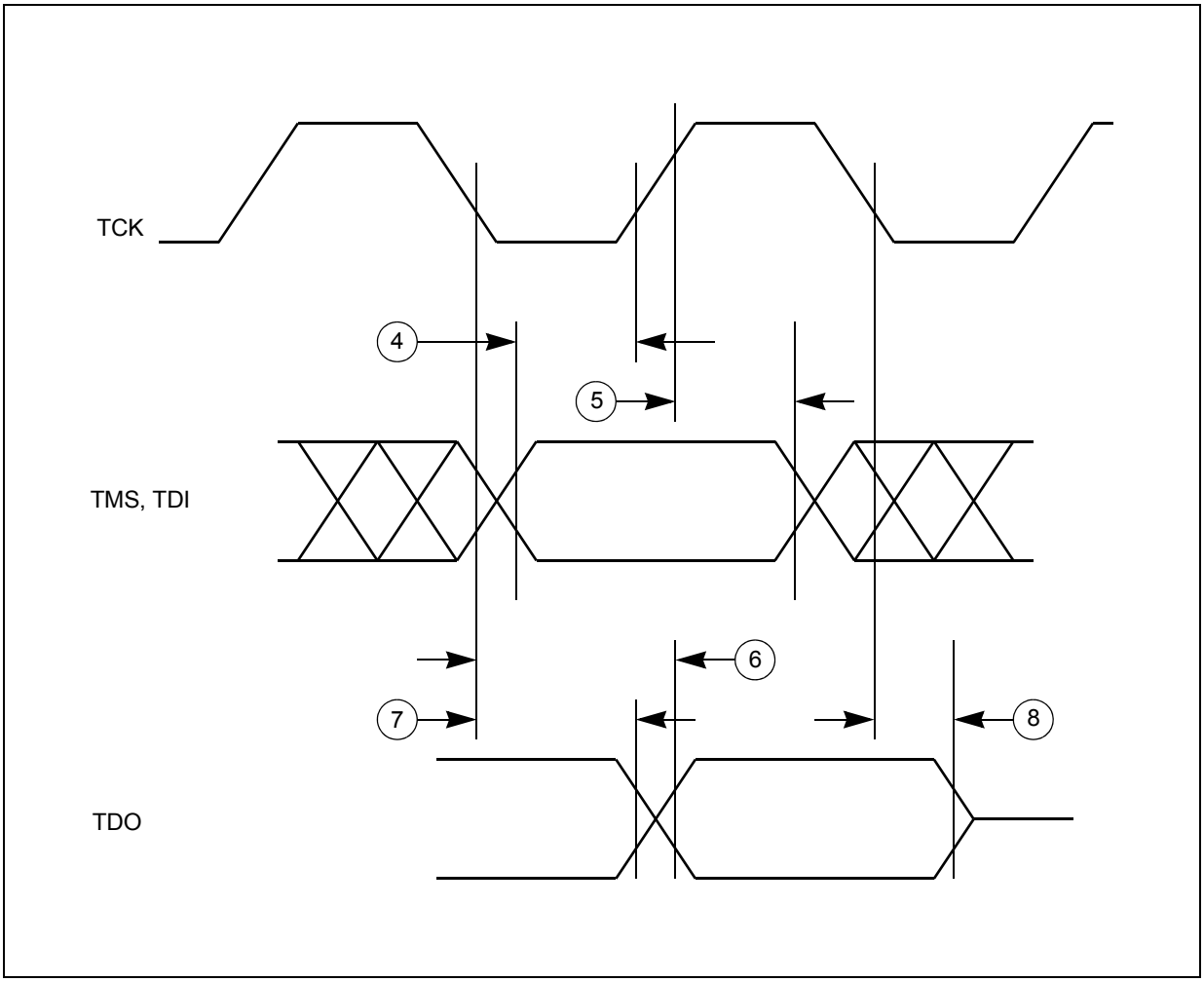


Table 41. DSPI timing[1] (continued)

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
12	t_{HO}	CC	D	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
					Slave	6	—	
					Master (MTFE = 1, CPHA = 0)	6	—	
					Master (MTFE = 1, CPHA = 1)	–2	—	

1. All timing are provided with 50pF capacitance on output, 1ns transition time on input signal

Figure 29. DSPI classic SPI timing — master, CPHA = 0

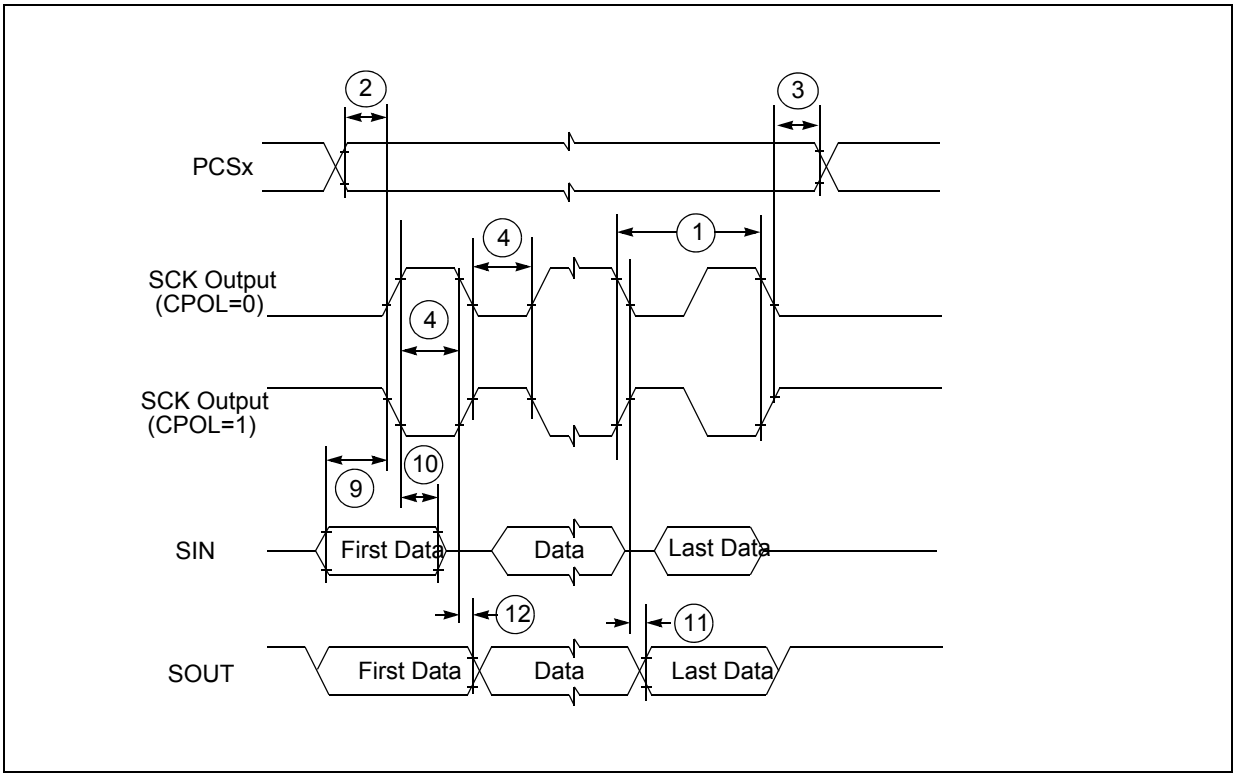


Figure 30. DSPI classic SPI timing — master, CPHA = 1

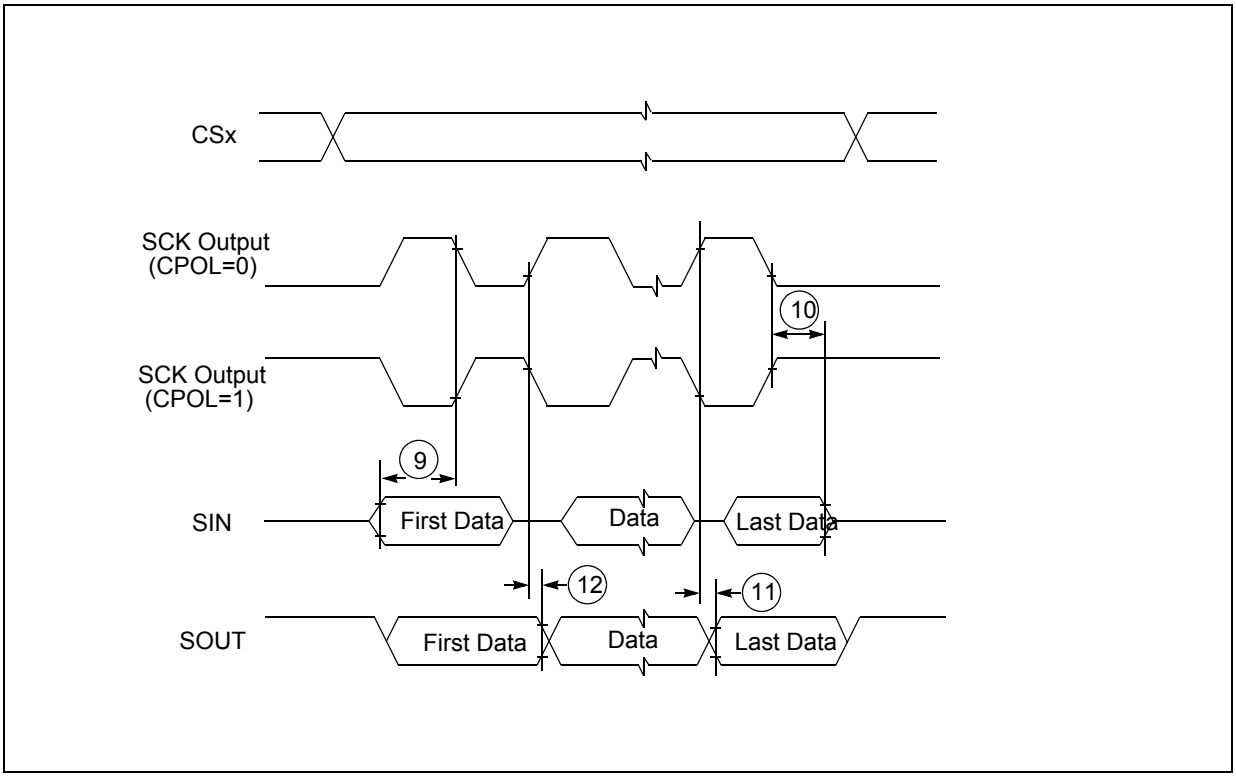


Figure 31. DSPI classic SPI timing — slave, CPHA = 0

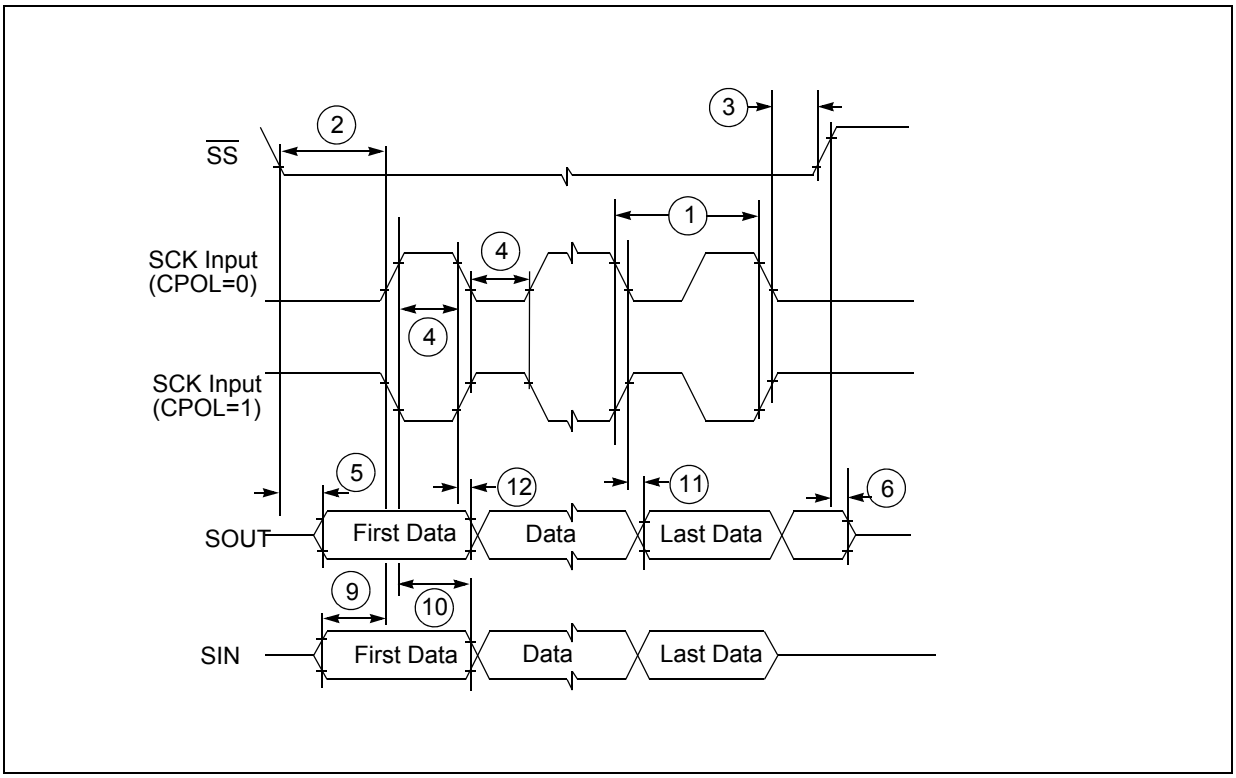


Table 44. Document revision history (continued)

Date	Revision	Substantive changes
15-May-2012	3	Removed “Enhanced Full-featured” version. In the cover page, added “(1 × Master/Slave, 1 × Master Only)“ at the end of the bullet “2 LINFlex modules (LIN 2.1)” *Table 2: SPC56xP54x/SPC56xP60x device comparison*, updated the value of “LINFLEX module” to “2 (1 × Master/Slave, 1 × Master only)” *Section 1.5.4: On-chip flash memory with ECC* replaced two occurrences of “3 wait states” to “2 wait states” replaced 60 MHz to 64 MHz *Section 1.5.21: Serial communication interface module (LINFlex)*, updated first bullet to “Supports LIN Master mode (on both modules), LIN Slave mode (on one module) and UART mode” *Section 1.5.24: Analog-to-digital converter (ADC)*, removed bullet concerning the analog watchdogs from Normal mode features. *Table 5: Supply pins*, removed V_{REG_BYPASS} row. *Table 6: System pins*: added V_{REG_BYPASS} row added a footnote about $\overline{RESET}$ *Table 9: Absolute maximum ratings*: changed typical value of TV_{DD} to 0.25 and added a footnote added V_{INAN} entry Updated *Section 3.8.1: Voltage regulator electrical characteristics* Updated *Table 14: EMI testing specifications* *Table 18: Low voltage monitor electrical characteristics*, changed maximum value of $V_{MLVDDOK\_H}$ to 1.15 *Table 20: DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V]=0)*, added IPU and IPD rows for $\overline{RESET}$ pin. *Table 21: Supply current (5.0 V, NVUSRO[PAD3V5V]=0)*: added maximum values of $I_{DD\_LV\_CORE}$ for: RUN, HALT, and STOP mode updated values and parameter classification of I_{DD_FLASH} *Table 22: DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V]=1)*, added IPU and IPD rows for $\overline{RESET}$ pin. *Table 23: Supply current (3.3 V, NVUSRO[PAD3V5V]=1)*: added maximum values of $I_{DD\_LV\_CORE}$ for: RUN, HALT, and STOP mode updated values and parameter classification of I_{DD_FLASH} Added *Table 26: I/O consumption* *Table 31: 16 MHz RC oscillator electrical characteristics*, changed minimum and maximum values of Δ_{RCMVAR} respectively to -6 and 6. Renamed *Figure 16: Input equivalent circuit (precise channels)* (was “Input equivalent circuit”) Added *Figure 17: Input equivalent circuit (extended channels)* *Section 3.15.1: Input impedance and ADC accuracy*, updated *Equation 4* and *Equation 10* *Table 32: ADC conversion characteristics*, added V_{INAN}, C_{P3} and R_{SW2} rows