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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	49
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc56ap60l3cefbr

Table 1. Device summary

Package	Part number	
	768 KB Flash	1 MB Flash
LQFP144	SPC560P54L5 SPC56AP54L5	SPC560P60L5 SPC56AP60L5
LQFP100	SPC560P54L3 SPC56AP54L3	SPC560P60L3 SPC56AP60L3

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1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the SPC56xP54x/SPC56xP60x series of microcontroller units (MCUs). It also describes the device features and highlights important electrical and physical characteristics. For functional characteristics, refer to the device reference manual.

1.2 Description

This 32-bit system-on-chip (SoC) automotive microcontroller family is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address chassis applications specifically the airbag application.

This family is one of a series of next-generation integrated automotive microcontrollers based on the Power Architecture technology.

The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category. It operates up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

1.3 Device comparison

Table 2 provides a summary of different members of the SPC56xP54x/SPC56xP60x family and their features—relative to Full-featured version—to enable a comparison among the family members and an understanding of the range of functionality offered within this family.

Table 2. SPC56xP54x/SPC56xP60x device comparison

Feature	SPC560P54	SPC560P60	SPC56AP54	SPC56AP60
Code Flash memory (with ECC)	768 KB	1 MB	768 KB	1 MB
Data Flash / EE (with ECC)	64 KB			
SRAM (with ECC)	64 KB	80 KB	64 KB	80 KB
Processor core	32-bit e200z0h		32-bit Dual e200z0h	
Instruction set	VLE			
CPU performance	0-64 MHz			
FMPLL (frequency-modulated phase-locked loop) modules	1			
INTC (interrupt controller) channels	148			
PIT (periodic interrupt timer)	1 (includes four 32-bit timers)			

Table 2. SPC56xP54x/SPC56xP60x device comparison (continued)

Feature		SPC560P54	SPC560P60	SPC56AP54	SPC56AP60
Enhanced DMA (direct memory access) channels		16			
FlexRay		Yes (64 message buffer)			
FlexCAN (controller area network)		3(1),(2)			
Safety port		Yes (via third FlexCAN module)			
FCCU (fault collection and control unit)		Yes(3)			
CTU (cross triggering unit)		Yes			
eTimer channels		2 × 6			
FlexPWM (pulse-width modulation) channels		No			
Analog-to-digital converters (ADC)		One (10-bit, 27-channel)(4)			
LINFlex modules		2 (1 × Master/Slave, 1 × Master only)(5)			
DSPI (deserial serial peripheral interface) modules		5(6)			
CRC (cyclic redundancy check) units		2(7)			
JTAG interface		Yes			
Nexus port controller (NPC)		Yes (Level 2+)(8)			
Supply	Digital power supply(9)	3.3 V or 5 V single supply with external transistor			
	Analog power supply	3.3 V or 5 V			
	Internal RC oscillator	16 MHz			
	External crystal oscillator	4–40 MHz			
Packages		LQFP100 LQFP144			LQFP100 LQFP144 LQFP176(10)
Temperature	Standard ambient temperature	–40 to 125 °C			

1. Each FlexCAN module has 32 message buffers.
2. One FlexCAN module can act as a Safety Port with a bit rate as high as 7.5 Mbit/s.
3. Enhanced FCCU version.
4. Same amount of ADC channels as on SPC560P44/50 not considering the internally connected ones. 26 channels on LQFP144 and 16 channels on LQFP100.
5. LinFlex_1 is Master Only.
6. Increased number of CS for DSPI_1.
7. Upgraded specification with addition of 8-bits polynomial (CRC-8 VDA CAN) support and 3rd context.
8. Improved debugging capability with data trace capability and increased Nexus throughput available on emulation package.
9. 3.3 V range and 5 V range correspond to different orderable parts.
10. Software development package only. Not available for production.

Table 4. SPC56xP54x/SPC56xP60x series block summary

Block	Function
Analog-to-digital converter (ADC)	Multi-channel, 10-bit analog-to-digital converter
Boot assist module (BAM)	Block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Controller area network (FlexCAN)	Supports the standard CAN communications protocol
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Crossbar switch (XBAR)	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 32-bit data bus width.
Cyclic redundancy checker (CRC) unit	Is dedicated to the computation of CRC off-loading the CPU. Each context has a separate CRC computation engine in order to allow the concurrent computation of the CRC of multiple data streams.
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced direct memory access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via "*n*" programmable channels
Enhanced timer (eTimer)	Provides enhanced programmable up/down modulo counting
Error correction status module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
External oscillator (XOSC)	Provides an output clock used as input reference for FMPLL_0 or as reference clock for specific modules depending on system needs
Fault collection and control unit (FCCU)	Provides functional safety to the device
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexRay (FlexRay communication controller)	Provides high-speed distributed control for advanced automotive applications
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications

The default booting scheme is the one which uses the internal flash memory (an internal pull-down is used to select this mode). The alternate option allows the user to boot via FlexCAN or LINFlex (using the boot assist module software).

A censorship scheme is provided to protect the contents of the flash memory and offer increased security for the entire device.

A password mechanism is designed to grant the legitimate user access to the non-volatile memory.

1.5.16.1 Boot assist module (BAM)

The BAM is a block of read-only one-time programmed memory and is identical for all SPC56xP54x/SPC56xP60x devices that are based on the e200z0h core. The BAM program is executed every time the device is powered on if the alternate boot mode has been selected by the user.

The BAM provides the following features:

- Serial bootloading via FlexCAN or LINFlex.
- BAM can accept a password via the used serial communication channel to grant the legitimate user access to the non-volatile memory.

1.5.17 Error correction status module (ECSM)

The ECSM on this device features the following:

- Platform configuration and revision
- ECC error reporting for flash memory and SRAM
- ECC error injection for SRAM

The ECSM module is replicated for each processor.

1.5.18 FlexCAN

The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. FlexCAN module contains 32 message buffers.

The FlexCAN module provides the following features:

- Full implementation of the CAN protocol specification, Version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - 0 to 8 bytes data length
  - Programmable bit rate as fast as 1 Mbit/s
- 32 message buffers of 0 to 8 bytes data length
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- 3 programmable mask registers

1.5.21 Serial communication interface module (LINFlex)

The LINFlex on the SPC56xP54x/SPC56xP60x features the following:

- Supports LIN Master mode (on both modules), LIN Slave mode (on one module) and UART mode
- LIN state machine compliant to LIN1.3, 2.0, and 2.1 Specifications
- Handles LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store Identifier and up to 8 data bytes
  - Supports message length as long as 64 bytes
  - Detection and flagging of LIN errors: Sync field; Delimiter; ID parity; Bit; Framing; Checksum and Time-out errors
  - Classic or extended checksum calculation
  - Configurable Break duration as long as 36-bit times
  - Programmable Baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features: Loop back; Self Test; LIN bus stuck dominant detection
  - Interrupt-driven operation with 16 interrupt sources
- LIN slave mode features
  - Autonomous LIN header handling
  - Autonomous LIN response handling
- UART mode
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit or 9-bit words)
  - Error detection and flagging
  - Parity, Noise and Framing errors
  - Interrupt-driven operation with four interrupt sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - 2 receiver wake-up methods

1.5.22 Deserial serial peripheral interface (DSPI)

The deserial serial peripheral interface (DSPI) module provides a synchronous serial interface for communication between the SPC56xP54x/SPC56xP60x MCU and external devices.

Table 5. Supply pins (continued)

Supply		Pin		
Symbol	**Description**	**LQFP 100**	**LQFP 144**	**LQFP 176(1)**
$V_{DD\_HV\_REG}$ (3.3 V or 5.0 V)	Voltage regulator supply voltage	50	72	86
$V_{DD\_LV\_REGCOR}$	1.2 V decoupling(2) pins for core logic supply and voltage regulator feedback. Decoupling capacitor must be connected between this pins and $V_{SS\_LV\_REGCOR}$.	48	70	82
$V_{SS\_LV\_REGCOR}$	1.2 V decoupling(2) pins for core logic GND and voltage regulator feedback. Decoupling capacitor must be connected between this pins and $V_{DD\_LV\_REGCOR}$.	49	71	85
ADC0 reference and supply voltage				
$V_{DD\_HV\_AD}$	ADC supply and high reference voltage	39	56	64
$V_{SS\_HV\_AD}$	ADC ground and low reference voltage	40	57	65
Power supply pins (3.3 V or 5.0 V)				
$V_{DD\_HV\_IO0}$	Input/Output supply voltage	—	6	14
$V_{SS\_HV\_IO0}$	Input/Output ground	—	7	15
$V_{DD\_HV\_IO1}$	Input/Output supply voltage	13	21	29
$V_{SS\_HV\_IO1}$	Input/Output ground	14	22	30
$V_{DD\_HV\_IO2}$	Input/Output supply voltage	63	91	115
$V_{SS\_HV\_IO2}$	Input/Output ground	62	90	114
$V_{DD\_HV\_IO3}$	Input/Output supply voltage	87	126	150
$V_{SS\_HV\_IO3}$	Input/Output ground	88	127	151
$V_{DD\_HV\_IO4}$	Input/Output supply voltage	—	—	169
$V_{SS\_HV\_IO4}$	Input/Output ground	—	—	170
$V_{DD\_HV\_IO5}$	Input/Output supply voltage	—	—	5
$V_{SS\_HV\_IO5}$	Input/Output ground	—	—	6
$V_{DD\_HV\_IO6}$	Input/Output supply voltage	—	—	108
$V_{SS\_HV\_IO6}$	Input/Output ground	—	—	109
$V_{DD\_HV\_FL}$	Code and data flash supply voltage	69	97	121
$V_{SS\_HV\_FL}$	Code and data flash supply ground	68	96	120
$V_{DD\_HV\_OSC}$	Crystal oscillator amplifier supply voltage	16	27	35
$V_{SS\_HV\_OSC}$	Crystal oscillator amplifier ground	17	28	36
Power supply pins (1.2 V)				
$V_{DD\_LV\_COR0}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR0}$ pin.	12	18	26

Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
Port B										
B[0]	PCR[16]	ALT0 ALT1 ALT2 ALT3 —	GPIO[16] TXD ETC[2] DEBUG[0] EIRQ[15]	SIUL FlexCAN_0 eTimer_1 SSCM SIUL	I/O O I/O — I	Slow	Medium	76	109	133
B[1]	PCR[17]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[17] CS7_1 ETC[3] DEBUG[1] RXD EIRQ[16]	SIUL DSPI_1 eTimer_1 SSCM FlexCAN_0 SIUL	I/O O I/O — I I	Slow	Medium	77	110	134
B[2]	PCR[18]	ALT0 ALT1 ALT2 ALT3 —	GPIO[18] TXD SOUT_4 DEBUG[2] EIRQ[17]	SIUL LINFlex_0 DSPI_4 SSCM SIUL	I/O O I/O — I	Slow	Medium	79	114	138
B[3]	PCR[19]	ALT0 ALT1 ALT2 ALT3 —	GPIO[19] — SCK_4 DEBUG[3] RXD	SIUL — DSPI_4 SSCM LINFlex_0	I/O — I/O — I	Slow	Medium	80	116	140
B[6]	PCR[22]	ALT0 ALT1 ALT2 ALT3 —	GPIO[22] clk_out CS2_2 clk_out_div256 EIRQ[18]	SIUL MC_CGL DSPI_2 MC_CGL SIUL	I/O O O O I	Slow	Medium	96	138	162
B[7]	PCR[23]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[23] — — — AN[0] RXD	SIUL — — — ADC_0 LINFlex_0	Input Only	—	—	29	43	51
B[8]	PCR[24]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[24] — — — AN[1] ETC[5]	SIUL — — — ADC_0 eTimer_0	Input Only	—	—	31	47	55

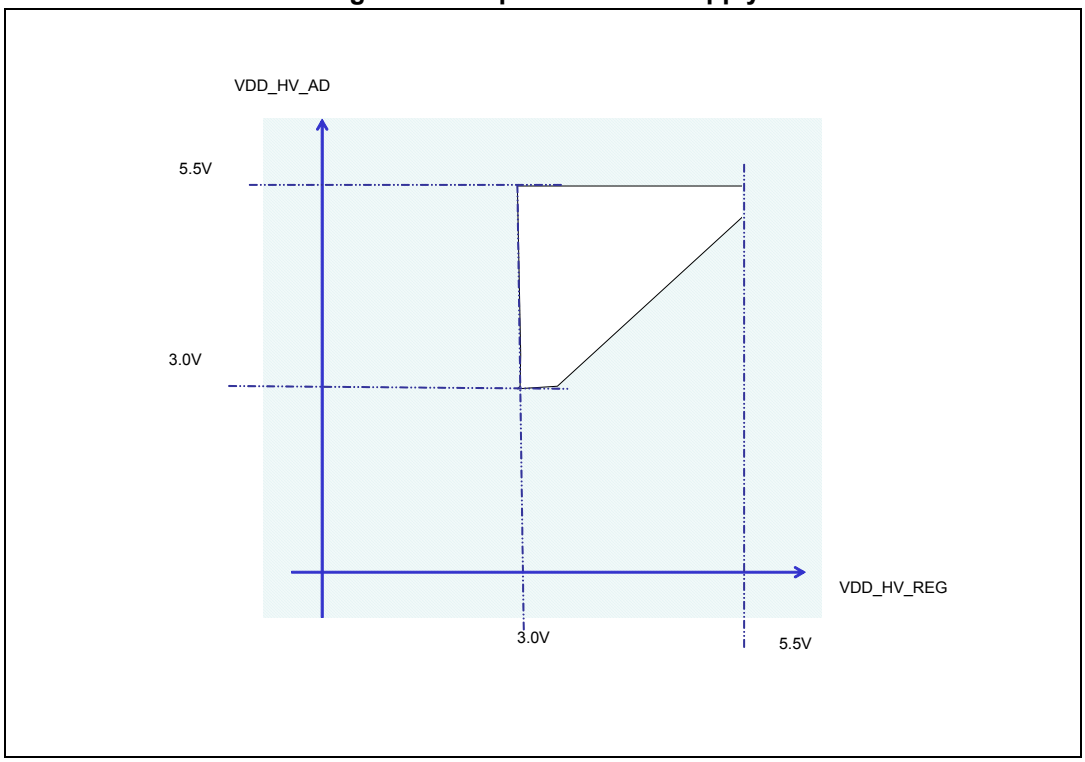
Table 11. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Min	Max(1)	Unit
$V_{DD\_HV\_REG}$	SR	3.3 V voltage regulator supply voltage	—	3.0	3.6	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$ – 0.1	$V_{DD\_HV\_IOx}$ + 0.1	
$V_{DD\_HV\_AD}$	SR	3.3 V ADC supply and high reference voltage	—	3.0	5.5	V
			Relative to $V_{DD\_HV\_REG}$	$V_{DD\_HV\_REG}$ – 0.1	5.5	
$V_{SS\_HV\_AD}$	SR	ADC ground and low reference voltage	—	0	0	V
$V_{DD\_LV\_REGCOR}$(3),(4)	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_REGCOR}$(3)	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_CORx}$(3),(4)	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_CORx}$(3)	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	—	–40	125	°C

1. Parametric figures can be out of specification when voltage drops below 4.5 V, however, guaranteeing the full functionality. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.
2. The difference between each couple of voltage supplies must be less than 100 mV, $|V_{DD\_HV\_IOy} – V_{DD\_HV\_IOx}| < 100$ mV.
3. To be connected to emitter of external NPN. Low voltage supplies are not under user control—these are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds ($V_{SS\_LV\_xxx}$) must be shorted to high voltage grounds ($V_{SS\_HV\_xxx}$) and the low voltage supply pins ($V_{DD\_LV\_xxx}$) must be connected to the external ballast emitter.
4. The low voltage supplies ($V_{DD\_LV\_xxx}$) are not all independent.
$V_{DD\_LV\_COR1}$ and $V_{DD\_LV\_COR2}$ are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash memory module. Similarly, $V_{SS\_LV\_COR1}$ and $V_{SS\_LV\_COR2}$ are internally shorted.
$V_{DD\_LV\_REGCOR}$ and $V_{DD\_LV\_REGCORx}$ are physically shorted internally, as are $V_{SS\_LV\_REGCOR}$ and $V_{SS\_LV\_CORx}$.

Figure 7 shows the constraints of the different power supplies.

Figure 8. Independent ADC supply



3.5 Thermal characteristics

Table 12. Thermal characteristics for 144-pin LQFP

Symbol		Parameter	Conditions	Typical value	Unit
$R_{\theta JA}$	D	Thermal resistance junction-to-ambient, natural convection(1)	Single layer board—1s	53.4	°C/W
	D		Four layer board—2s2p	43.9	°C/W
$R_{\theta JB}$	D	Thermal resistance junction-to-board(2)	Four layer board—2s2p	29.6	°C/W
$R_{\theta JCtop}$	D	Thermal resistance junction-to-case (top)(3)	Single layer board—1s	9.3	°C/W
Ψ_{JB}	D	Junction-to-board, natural convection(4)	Operating conditions	29.8	°C/W
Ψ_{JC}	D	Junction-to-case, natural convection(5)	Operating conditions	1.3	°C/W

1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-7. Thermal test board meets JEDEC specification for this package.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.
5. Thermal characterization parameter indicating the temperature difference between the case and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

Table 20. DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V]=0) (continued)

Symbol		Parameter	Conditions	Min	Max	Unit
I_{PU}	P	Equivalent pull-up current	$V_{IN} = V_{IL}$	–130	—	µA
			$V_{IN} = V_{IH}$	—	–10	
I_{PD}	P	Equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	µA
			$V_{IN} = V_{IH}$	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = –40 to 125 °C	–1	1	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_A = –40 to 125 °C	–0.5	0.5	µA
C_{IN}	D	Input capacitance	—	—	10	pF
I_{PU}	D	$\overline{\text{RESET}}$, equivalent pull-up current	$V_{IN} = V_{IL}$	–130	—	µA
			$V_{IN} = V_{IH}$	—	–10	
I_{PD}	D	$\overline{\text{RESET}}$, equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	µA
			$V_{IN} = V_{IH}$	—	130	

1. “SR” parameter values must not exceed the absolute maximum ratings shown in *Table 9*.

3.11.2 DC electrical characteristics (3.3 V)

Table 22 gives the DC electrical characteristics at 3.3 V (3.0 V < $V_{DD\_HV\_IOx}$ < 3.6 V, NVUSRO[PAD3V5V]=1) as described in *Figure 14*.

Figure 14. I/O input DC electrical characteristics definition

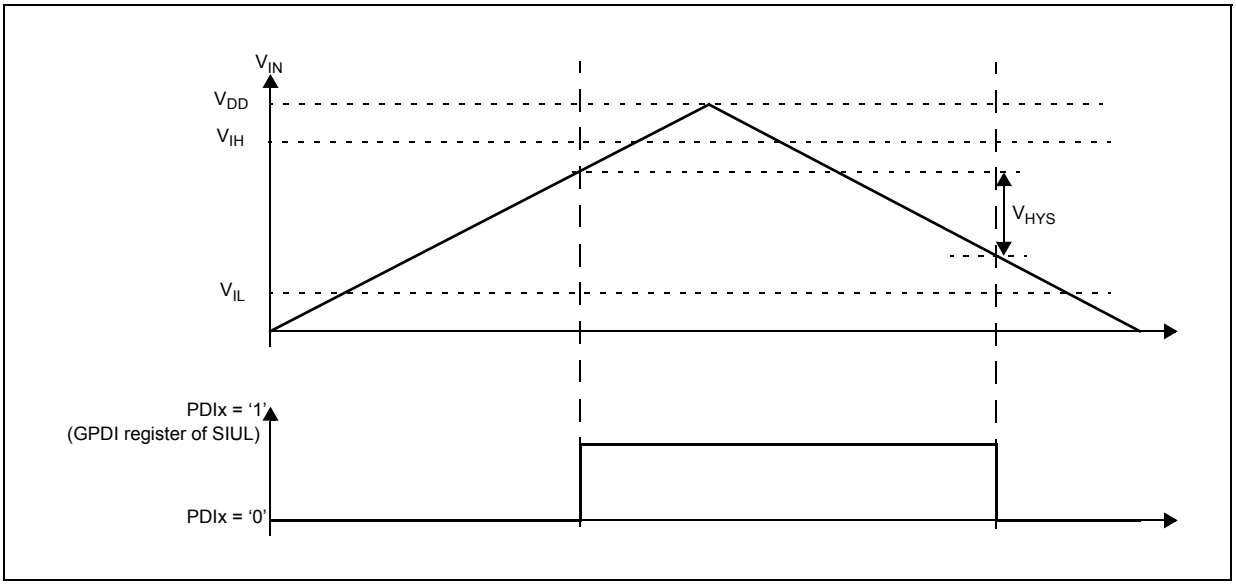


Table 22. DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V]=1)(1)

Symbol		Parameter	Conditions	Min	Max	Unit
V_{IL}	D	Minimum low level input voltage	—	–0.1(2)	—	V
V_{IL}	P	Maximum low level input voltage	—	—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IH}	P	Minimum high level input voltage	—	0.65 $V_{DD\_HV\_IOx}$	—	V
V_{IH}	D	Maximum high level input voltage	—	—	$V_{DD\_HV\_IOx}$ + 0.1(2)	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IOx}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 2 mA	—	0.5	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –2 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_F}	P	Fast, high level output voltage	I_{OL} = 11 mA	—	0.5	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –11 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_SYM}	P	Symmetric, high level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_SYM}	P	Symmetric, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
I_{PU}	P	Equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	

Table 22. DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V]=1)(1) (continued)

Symbol		Parameter	Conditions	Min	Max	Unit
I_{PD}	P	Equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	µA
			$V_{IN} = V_{IH}$	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = –40 to 125 °C	—	1	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_A = –40 to 125 °C	—	0.5	µA
C_{IN}	D	Input capacitance	—	—	10	pF
I_{PU}	D	$\overline{\text{RESET}}$, equivalent pull-up current	$V_{IN} = V_{IL}$	–130	—	µA
			$V_{IN} = V_{IH}$	—	–10	
I_{PD}	D	$\overline{\text{RESET}}$, equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	µA
			$V_{IN} = V_{IH}$	—	130	

1. These specifications are design targets and subject to change per device characterization.
2. “SR” parameter values must not exceed the absolute maximum ratings shown in *Table 9*.

3.11.3 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in *Table 25*.

Table 25. I/O supply segment

Package	Supply segment						
	1	2	3	4	5	6	7
LQFP144	pin8 – pin20	pin23 – pin38	pin39 – pin55	pin58 – pin68	pin73 – pin89	pin92 – pin125	pin128 – pin5
LQFP100	pin15 – pin26	pin27 – pin38	pin41 – pin46	pin51 – pin61	pin64 – pin86	pin89 – pin10	—

Table 26. I/O consumption

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{SWTSLW}[2]	CC	D	Dynamic I/O current for SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16	
I_{SWTMED}[2]	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	29	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	17	
I_{SWTFST}[2]	CC	D	Dynamic I/O current for FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	110	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
I_{RMSSLW}	CC	D	Root medium square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.3	mA
				C_L = 25 pF, 4 MHz		—	—	3.2	
				C_L = 100 pF, 2 MHz		—	—	6.6	
				C_L = 25 pF, 2 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.6	
				C_L = 25 pF, 4 MHz		—	—	2.3	
				C_L = 100 pF, 2 MHz		—	—	4.7	
I_{RMSMED}	CC	D	Root medium square I/O current for MEDIUM configuration	C_L = 25 pF, 13 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	mA
				C_L = 25 pF, 40 MHz		—	—	13.4	
				C_L = 100 pF, 13 MHz		—	—	18.3	
				C_L = 25 pF, 13 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	5	
				C_L = 25 pF, 40 MHz		—	—	8.5	
				C_L = 100 pF, 13 MHz		—	—	11	

Table 26. I/O consumption (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{RMSFST}	CC	D	Root medium square I/O current for FAST configuration	C_L = 25 pF, 40 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	22	mA
				C_L = 25 pF, 64 MHz		—	—	33	
				C_L = 100 pF, 40 MHz		—	—	56	
				C_L = 25 pF, 40 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C_L = 25 pF, 64 MHz		—	—	20	
				C_L = 100 pF, 40 MHz		—	—	35	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

3.12 Main oscillator electrical characteristics

The SPC56xP54x/SPC56xP60x provides an oscillator/resonator driver.

Table 27. Main oscillator electrical characteristics (5.0 V, NVUSRO[PAD3V5V]=0)

Symbol		Parameter	Min	Max	Unit
f_{OSC}	SR	Oscillator frequency	4	40	MHz
g_m	P	Transconductance	6.5	25	mA/V
V_{OSC}	T	Oscillation amplitude on EXTAL pin	1	—	V
t_{OSCSU}	T	Start-up time[1],[2]	8	—	ms

1. The start-up time is dependent upon crystal characteristics, board leakage, etc., high ESR and excessive capacitive loads can cause long start-up time.
2. Value captured when amplitude reaches 90% of EXTAL.

Table 28. Main oscillator electrical characteristics (3.3 V, NVUSRO[PAD3V5V]=1)

Symbol		Parameter	Min	Max	Unit
f_{OSC}	SR	Oscillator frequency	4	40	MHz
g_m	P	Transconductance	4	20	mA/V
V_{OSC}	T	Oscillation amplitude on EXTAL pin	1	—	V
t_{OSCSU}	T	Start-up time[1],[2]	8	—	ms

1. The start-up time is dependent upon crystal characteristics, board leakage, etc., high ESR and excessive capacitive loads can cause long start-up time.
2. Value captured when amplitude reaches 90% of EXTAL.

2. “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self clocked mode.
3. Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.
4. f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.
5. This value is determined by the crystal manufacturer and board design.
6. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.
7. Proper PC board layout procedures must be followed to achieve specifications.
8. Values are obtained with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).
9. Short term jitter is measured on the clock rising edge at cycle n and cycle n+4.
10. This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this PLL, load capacitors should not exceed these limits.
11. This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
12. This value is true when operating at frequencies above 60 MHz, otherwise f_{CS} is 2% (above 64 MHz).
13. Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

3.14 16 MHz RC oscillator electrical characteristics

Table 31. 16 MHz RC oscillator electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
f_{RC}	P	RC oscillator frequency	T_A = 25 °C	—	16	—	MHz
Δ_{RCMVAR}	P	Fast internal RC oscillator variation over temperature and supply with respect to f_{RC} at T_A = 25 °C in high-frequency configuration	—	–6	—	6	%
$\Delta_{RCMTRIM}$	T	Post Trim Accuracy: The variation of the PTF(1) from the 16 MHz	T_A = 25 °C	–1	—	1	%
$\Delta_{RCMSTEP}$	T	Fast internal RC oscillator trimming step	T_A = 25 °C	—	1.6	—	%

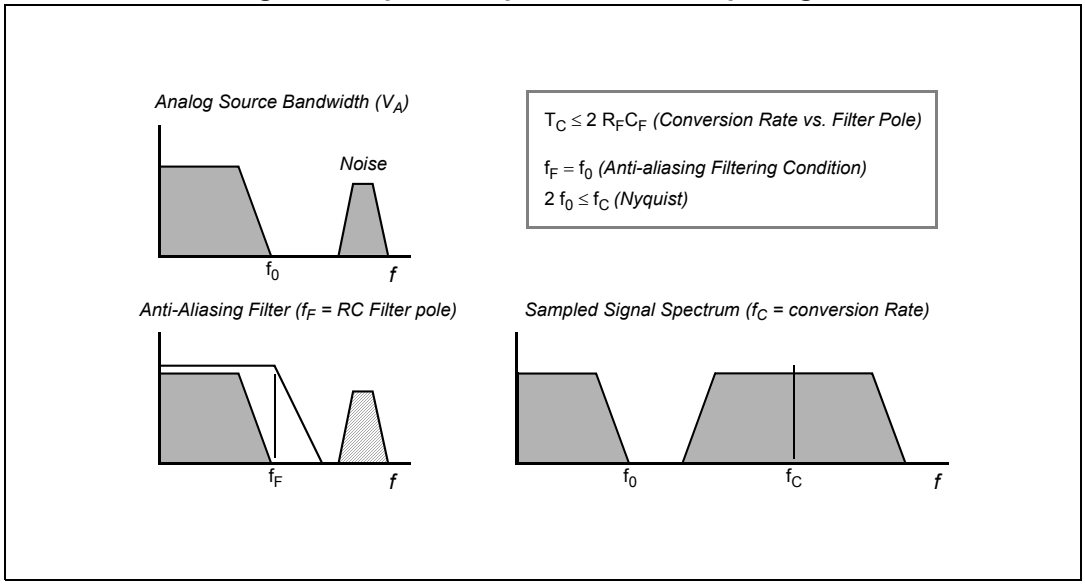
1. PTF = Post Trimming Frequency: The frequency of the output clock after trimming at typical supply voltage and temperature

3.15 Analog-to-Digital converter (ADC) electrical characteristics

The device provides a 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

C_S with respect to the ideal source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing.

Figure 19. Spectral representation of input signal



Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive *Equation 11* between the ideal and real sampled voltage on C_S:

Equation 11

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Equation 12

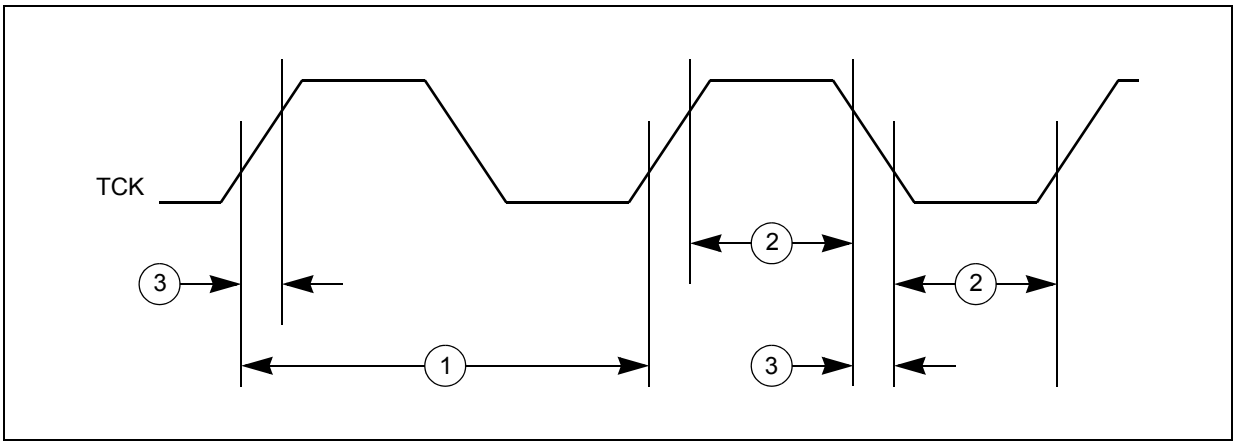
$$C_F > 2048 \times C_S$$

3.18.2 IEEE 1149.1 interface timing

Table 38. JTAG pin AC electrical characteristics

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	CC	D	TCK cycle time	—	100	—	ns
2	t_{JDC}	CC	D	TCK clock pulse width (measured at $V_{DD\_HV\_IOx}/2$)	—	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40% – 70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	—	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO data valid	—	—	40	ns
7	t_{TDOI}	CC	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	CC	D	TCK low to TDO high impedance	—	40	—	ns
9	t_{BSDV}	CC	D	TCK falling edge to output valid	—	—	50	ns
10	t_{BSDVZ}	CC	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
11	t_{BSDHZ}	CC	D	TCK falling edge to output high impedance	—	—	50	ns
12	t_{BSDST}	CC	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
13	t_{BSDHT}	CC	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

Figure 22. JTAG test clock input timing



6 Revision history

Table 44 summarizes revisions to this document.

Table 44. Document revision history

Date	Revision	Substantive changes
21-Dec-2010	1	Initial release
18-Oct-2011	2	In the Feature list: Revised the first bullet. Changed “Up to 82 GPIO” to “Up to 80 GPIO” Changed “and 82 GPIO” to “and 49 GPIO” Changed “FlexRay module“ to “1 FlexRay™ module”. Added *Section 1.5: Feature details* *Table 4: SPC56xP54x/SPC56xP60x series block summary*, added FlexRay entry. In the “LQFP176 pinout (top view)” figure: – Pin 104 now is TDI, was PB[5] – Pin 107 now is TDO, was PB[4] – Pin 71 now is NC, was OKOUT – Pin 72 now is NC, was OKOUT_B – Pin 87 now is NC, was NBYPASS_HV – Pin 88 now is NC, was IPP_LIVI_B_VDDIO *Table 7: Pin muxing*: PB[6] was clk_out_div5, is now clk_out_div256 Removed PB[4] and PB[5] rows In the A[3] row, changed ABS[2] to ABS[1] *Section 3.11: DC electrical characteristics*, added “Peripherals supply current (5 V and 3.3 V)” table *Table 14: EMI testing specifications*, removed all references to SAE Replaced both *Table 12: Thermal characteristics for 144-pin LQFP* and *Table 13: Thermal characteristics for 100-pin LQFP* *Table 30: PLLMRFM electrical specifications (V_{DDPLL} = 1.08 V to 1.32 V, V_{SS} = V_{SSPLL} = 0 V, TA = TL to TH)*, changed the max value of f_{SYS} from 120 to 64 *Table 33: Program and erase specifications*: Removed all TBC changed the initial max value of T_{BKPRG} (Code Flash) from 3.3 to 6.6 s changed the max value of T_{BKPRG} (Data Flash) from 1.9 to 4.1 s changed the max value of $T_{wprogram}$ (Data Flash) from 300 to 500 µs Added t_{ESRT} row *Table 17: Voltage regulator electrical characteristics*, updated $V_{DD\_LV\_REGCOR}$ values Updated *Table 18: Low voltage monitor electrical characteristics* Updated *Table 21: Supply current (5.0 V, NVUSRO[PAD3V5V]=0)* and *Table 23: Supply current (3.3 V, NVUSRO[PAD3V5V]=1)* Removed “NVUSRO[OSCILLATOR_MARGIN] field description” section. Removed orderable parts tables.