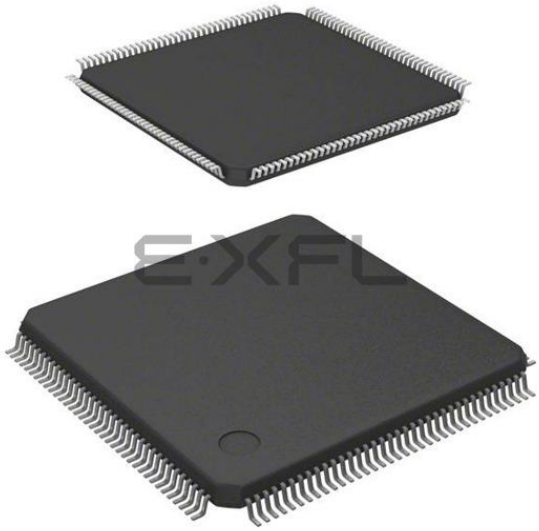

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 26x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc56ap60l5befar

Table 1. Device summary

Package	Part number	
	768 KB Flash	1 MB Flash
LQFP144	SPC560P54L5 SPC56AP54L5	SPC560P60L5 SPC56AP60L5
LQFP100	SPC560P54L3 SPC56AP54L3	SPC560P60L3 SPC56AP60L3

SPC56xP54x/SPC56xP60x is present on the market in two different options enabling different features: Full-featured, and Airbag configuration. *Table 3* shows the main differences between the two versions.

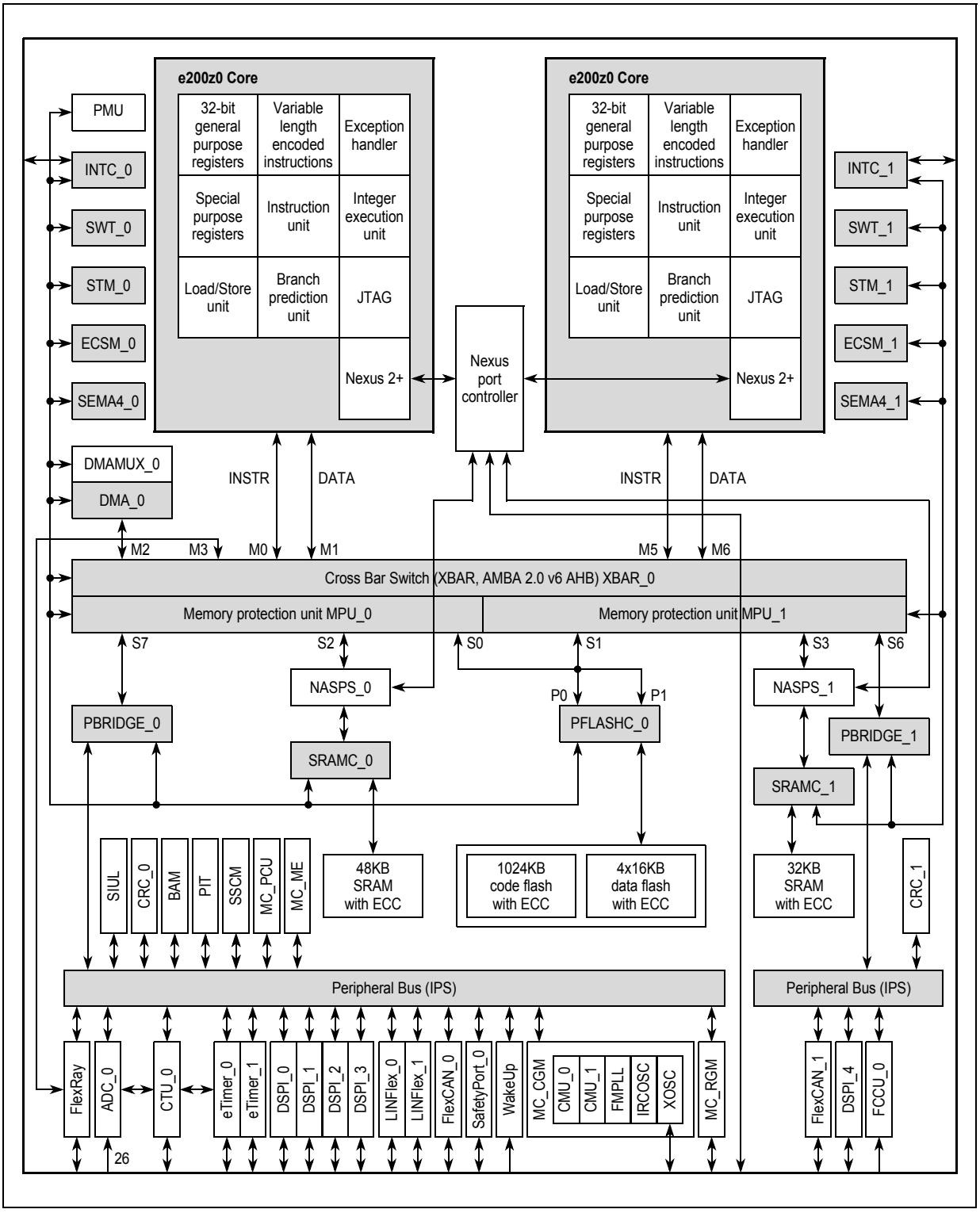
Table 3. SPC56xP54x/SPC56xP60x device configuration difference

Feature	Enhanced Full-featured	Full-featured	Airbag
FlexCAN (controller area network)	3	2	2
CTU (cross triggering unit)	Yes		No
FlexRay	Yes (64 message buffer)		No
DSPI (deserial serial peripheral interface) modules	5		4
CRC (cyclic redundancy check) unit	2		1

1.4 Block diagram

Figure 1 shows a top-level block diagram of the SPC56xP54x/SPC56xP60x MCU. *Table 4* summarizes the functions of the blocks.

Figure 1. SPC56xP54x/SPC56xP60x block diagram



The flash memory module provides the following features:

- Up to 1024 KB flash memory
  - 14 blocks (2×16 KB + 2×32 KB + 2×16 KB + 2×64 KB + 6×128 KB) code flash
  - 4 blocks (16 KB + 16 KB + 16 KB + 16 KB) data flash
  - Full Read While Write (RWW) capability between code and data flash
- Four 128-bit wide prefetch buffers to provide single cycle in-line accesses (prefetch buffers can be configured to prefetch code or data or both)
- Typical flash memory access time: 0 wait states for buffer hits, 2 wait states for page buffer miss at 64 MHz
- Hardware managed flash memory writes handled by 32-bit RISC Krypton engine
- Hardware and software configurable read and write access protections on a per-master basis.
- Configurable access timing allowing use in a wide range of system frequencies.
- Multiple-mapping support and mapping-based block access timing (0–31 additional cycles) allowing use for emulation of other memory types.
- Software programmable block program/erase restriction control.
- Erase of selected block(s)
- Read page size of 128 bits (4 words)
- 64-bit ECC with single-bit correction, double-bit detection for data integrity
- Embedded hardware program and erase algorithm
- Erase suspend, program suspend and erase-suspended program
- Censorship protection scheme to prevent flash memory content visibility
- Hardware support for EEPROM emulation

1.5.5 On-chip SRAM with ECC

The SPC56xP54x/SPC56xP60x SRAM module provides a general-purpose memory of up to 80 KB.

The SRAM module provides the following features:

- Supports read/write accesses mapped to the SRAM memory from any master
- Up to 80 KB general purpose RAM
  - 2 blocks (48 KB + 32 KB)
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory
- Typical SRAM access time: 0 wait state for reads and 32-bit writes; 1 wait state for 8- and 16-bit writes if back to back with a read to same memory block

1.5.6 Interrupt controller (INTC)

The INTC (interrupt controller) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To

The default booting scheme is the one which uses the internal flash memory (an internal pull-down is used to select this mode). The alternate option allows the user to boot via FlexCAN or LINFlex (using the boot assist module software).

A censorship scheme is provided to protect the contents of the flash memory and offer increased security for the entire device.

A password mechanism is designed to grant the legitimate user access to the non-volatile memory.

1.5.16.1 Boot assist module (BAM)

The BAM is a block of read-only one-time programmed memory and is identical for all SPC56xP54x/SPC56xP60x devices that are based on the e200z0h core. The BAM program is executed every time the device is powered on if the alternate boot mode has been selected by the user.

The BAM provides the following features:

- Serial bootloading via FlexCAN or LINFlex.
- BAM can accept a password via the used serial communication channel to grant the legitimate user access to the non-volatile memory.

1.5.17 Error correction status module (ECSM)

The ECSM on this device features the following:

- Platform configuration and revision
- ECC error reporting for flash memory and SRAM
- ECC error injection for SRAM

The ECSM module is replicated for each processor.

1.5.18 FlexCAN

The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. FlexCAN module contains 32 message buffers.

The FlexCAN module provides the following features:

- Full implementation of the CAN protocol specification, Version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - 0 to 8 bytes data length
  - Programmable bit rate as fast as 1 Mbit/s
- 32 message buffers of 0 to 8 bytes data length
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- 3 programmable mask registers

The DSPI modules provide these features:

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- Up to 28 chip select lines available
  - 8 each on DSPI_0 and DSPI_1
  - 4 each on DSPI_2, DSPI_3, and DSPI_4
- 8 clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for deglitching
- FIFOs for buffering up to 5 transfers on the transmit and receive side
- Queueing operation possible through use of the eDMA
- General purpose I/O functionality on pins when not used for SPI

1.5.23 eTimer

Two eTimer modules are provided, each with six 16-bit general purpose up/down timer/counter per module. The following features are implemented:

- Individual channel capability
  - Input capture trigger
  - Output compare
  - Double buffer (to capture rising edge and falling edge)
  - Separate prescaler for each counter
  - Selectable clock source
  - 0 % to 100% pulse measurement
  - Rotation direction flag (Quad decoder mode)
- Maximum count rate
  - Equals peripheral clock/2 — for external event counting
  - Equals peripheral clock — for internal clock counting
- Cascadeable counters
- Programmable count modulo
- Quadrature decode capabilities
- Counters can share available input pins
- Count once or repeatedly
- Preloadable counters
- Pins available as GPIO when timer functionality not in use

Table 5. Supply pins (continued)

Supply		Pin		
Symbol	Description	LQFP 100	LQFP 144	LQFP 176[1]
$V_{SS\_LV\_COR0}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR0}$ pin.	11	17	25
$V_{DD\_LV\_COR1}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR1}$ pin.	65	93	117
$V_{SS\_LV\_COR1}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR1}$ pin.	66	94	118
$V_{DD\_LV\_COR2}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR2}$ pin.	92	131	155
$V_{SS\_LV\_COR2}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR\ 2}$ pin.	93	132	156
$V_{DD\_LV\_COR3}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR3}$ pin.	25	36	44
$V_{SS\_LV\_COR3}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR\ 3}$ pin.	24	35	43

1. LQFP176 available only as development package.
2. See datasheet Voltage Regulator Electrical Characteristics section for more details.

2.2.2 System pins

Table 6 and *Table 7* contain information on pin functions for the SPC56xP54x/SPC56xP60x devices. The pins listed in *Table 6* are single-function pins. The pins shown in *Table 7* are multi-function pins, programmable via their respective Pad Configuration Register (PCR) values.

Table 6. System pins

Symbol	Description	Direction	Pad Speed[1]		Pin		
			SRC=0	SRC=1	LQFP 100	LQFP 144	LQFP 176[2]
Dedicated pins							
MDO0	Nexus Message Data Output—line 0	Output Only	Fast		—	9	17
MDO4	Nexus Message Data Output—line 4	Output Only	Fast		—	—	7

Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
Port C										
C[0]	PCR[32]	ALT0 ALT1 ALT2 ALT3 —	GPIO[32] — — — AN[19]	SIUL — — — ADC_0	Input Only	—	—	45	66	78
C[1]	PCR[33]	ALT0 ALT1 ALT2 ALT3 —	GPIO[33] — — — AN[2]	SIUL — — — ADC_0	Input Only	—	—	28	41	49
C[2]	PCR[34]	ALT0 ALT1 ALT2 ALT3 —	GPIO[34] — — — AN[3]	SIUL — — — ADC_0	Input Only	—	—	30	45	53
C[3]	PCR[35]	ALT0 ALT1 ALT2 ALT3 —	GPIO[35] CS1_0 ETC[4] TXD EIRQ[21]	SIUL DSPI_0 eTimer_1 LINFlex_1 SIUL	I/O O I/O O I	Slow	Medium	10	16	24
C[4]	PCR[36]	ALT0 ALT1 ALT2 ALT3 —	GPIO[36] CS0_0 — DEBUG[4] EIRQ[22]	SIUL DSPI_0 — SSCM SIUL	I/O I/O — — I	Slow	Medium	5	11	19
C[5]	PCR[37]	ALT0 ALT1 ALT2 ALT3 —	GPIO[37] SCK_0 SCK_4 DEBUG[5] EIRQ[23]	SIUL DSPI_0 DSPI_4 SSCM SIUL	I/O I/O I/O — I	Slow	Medium	7	13	21
C[6]	PCR[38]	ALT0 ALT1 ALT2 ALT3 —	GPIO[38] SOUT_0 — DEBUG[6] EIRQ[24]	SIUL DSPI_0 — SSCM SIUL	I/O O — — I	Slow	Medium	98	142	174

Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
E[15]	PCR[79]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[79] — — — SIN_3 EIRQ[27]	SIUL — — — DSPI_3 SIUL	I/O — — — I I	Slow	Medium	—	121	145
Port F										
F[0]	PCR[80]	ALT0 ALT1 ALT2 ALT3 —	GPIO[80] DBG_0 CS3_3 — EIRQ[28]	SIUL FlexRay_0 DSPI_3 — SIUL	I/O O O — I	Slow	Medium	—	133	157
F[1]	PCR[81]	ALT0 ALT1 ALT2 ALT3 —	GPIO[81] DBG_1 CS2_3 — EIRQ[29]	SIUL FlexRay_0 DSPI_3 — SIUL	I/O O O — I	Slow	Medium	—	135	159
F[2]	PCR[82]	ALT0 ALT1 ALT2 ALT3	GPIO[82] DBG_2 CS1_3 —	SIUL FlexRay_0 DSPI_3 —	I/O O O —	Slow	Medium	—	137	161
F[3]	PCR[83]	ALT0 ALT1 ALT2 ALT3	GPIO[83] DBG_3 CS0_3 —	SIUL FlexRay_0 DSPI_3 —	I/O O I/O —	Slow	Medium	—	139	167
F[4]	PCR[84]	ALT0 ALT1 ALT2 ALT3	— — MDO[3] —	— — nexus_0 —	— — O —	Slow	Fast	—	4	4
F[5]	PCR[85]	ALT0 ALT1 ALT2 ALT3	— — MDO[2] —	— — nexus_0 —	— — O —	Slow	Fast	—	5	13
F[6]	PCR[86]	ALT0 ALT1 ALT2 ALT3	GPIO[86] — MDO[1] —	SIUL — nexus_0 —	I/O — O —	Slow	Fast	—	8	16

Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
Port G										
G[0]	PCR[96]	ALT0 ALT1 ALT2 ALT3 —	GPIO[96] F[0] — — EIRQ[30]	SIUL FCCU — — SIUL	I/O O — — I	Slow	Medium	—	38	46
G[1]	PCR[97]	ALT0 ALT1 ALT2 ALT3 —	GPIO[97] F[1] — — EIRQ[31]	SIUL FCCU — — SIUL	I/O O — — I	Slow	Medium	—	141	173
G[2]	PCR[98]	ALT0 ALT1 ALT2 ALT3 —	GPIO[98] — — — SIN_4	SIUL — — — DSPI_4	I/O — — — I	Slow	Medium	—	102	126
G[3]	PCR[99]	ALT0 ALT1 ALT2 ALT3	GPIO[99] — SOUT_4 —	SIUL — DSPI_4 —	I/O — O —	Slow	Medium	—	104	128
G[4]	PCR[100]	ALT0 ALT1 ALT2 ALT3	GPIO[100] — SCK_4 —	SIUL — DSPI_4 —	I/O — I/O —	Slow	Medium	—	100	124
G[5]	PCR[101]	ALT0 ALT1 ALT2 ALT3	GPIO[101] — CS0_4 —	SIUL — DSPI_4 —	I/O — I/O —	Slow	Medium	—	85	103
G[6]	PCR[102]	ALT0 ALT1 ALT2 ALT3	GPIO[102] — CS1_4 —	SIUL — DSPI_4 —	I/O — O —	Slow	Medium	—	98	122
G[7]	PCR[103]	ALT0 ALT1 ALT2 ALT3	GPIO[103] — CS2_4 —	SIUL — DSPI_4 —	I/O — O —	Slow	Medium	—	83	101

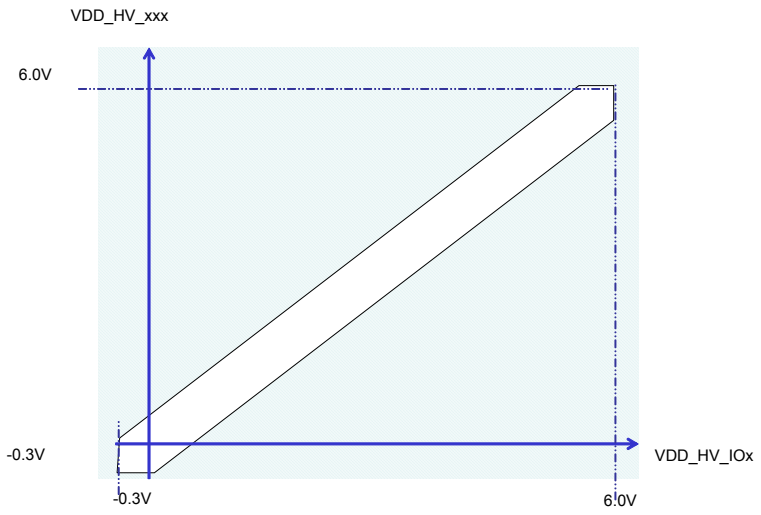
Table 9. Absolute maximum ratings(1) (continued)

Symbol		Parameter	Conditions	Min	Max(2)	Unit
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
I_{VDD_LV}	SR	Low voltage static current sink through V_{DD_LV}	—	—	155	mA
T_{STG}	SR	Storage temperature	—	–55	150	°C
T_J	SR	Junction temperature under bias	—	–40	150	°C

1. Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.
3. The difference between each couple of voltage supplies must be less than 300 mV, $|V_{DD\_HV\_IOy} - V_{DD\_HV\_IOx}| < 300$ mV.
4. Guaranteed by device validation.
5. Minimum value of TV_{DD} must be guaranteed until $V_{DD\_HV\_REG}$ reaches 2.6 V (maximum value of V_{PORH}).

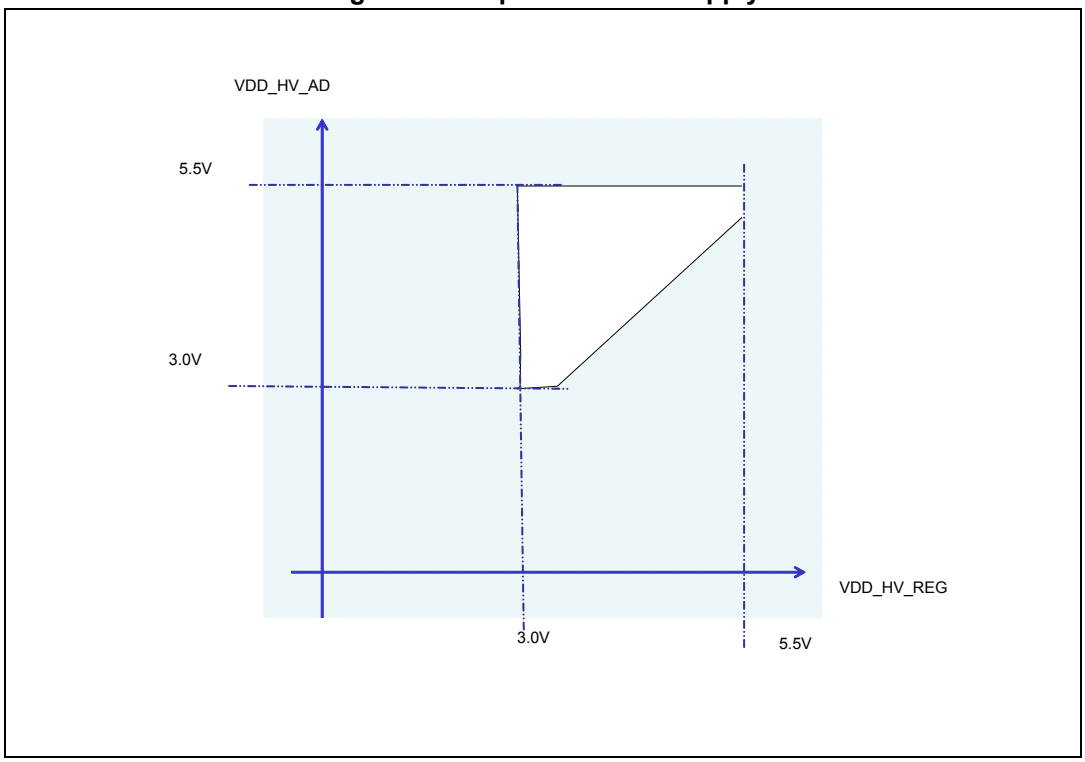
Figure 5 shows the constraints of the different power supplies.

Figure 5. Power supplies constraints



The SPC56xP54x/SPC56xP60x supply architecture provides an ADC supply that is managed independently of standard V_{DD_HV} supply. *Figure 6* shows the constraints of the ADC power supply.

Figure 8. Independent ADC supply



3.5 Thermal characteristics

Table 12. Thermal characteristics for 144-pin LQFP

Symbol		Parameter	Conditions	Typical value	Unit
$R_{\theta JA}$	D	Thermal resistance junction-to-ambient, natural convection(1)	Single layer board—1s	53.4	°C/W
	D		Four layer board—2s2p	43.9	°C/W
$R_{\theta JB}$	D	Thermal resistance junction-to-board(2)	Four layer board—2s2p	29.6	°C/W
$R_{\theta JCtop}$	D	Thermal resistance junction-to-case (top)(3)	Single layer board—1s	9.3	°C/W
Ψ_{JB}	D	Junction-to-board, natural convection(4)	Operating conditions	29.8	°C/W
Ψ_{JC}	D	Junction-to-case, natural convection(5)	Operating conditions	1.3	°C/W

1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-7. Thermal test board meets JEDEC specification for this package.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.
5. Thermal characterization parameter indicating the temperature difference between the case and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

Table 18. Low voltage monitor electrical characteristics

Symbol		Parameter	Conditions[1]	Value		Unit
				Min	Max	
V_{PORH}	T	Power-on reset threshold	—	1.5	2.7	V
V_{PORUP}	P	Supply for functional POR module	T_A = 25°C	1.0	—	V
$V_{REGLVDMOK\_H}$	P	Regulator low voltage detector high threshold	—	—	2.95	V
$V_{REGLVDMOK\_L}$	P	Regulator low voltage detector low threshold	—	2.6	—	V
$V_{FLLVDMOK\_H}$	P	Flash memory low voltage detector high threshold	—	—	2.95	V
$V_{FLLVDMOK\_L}$	P	Flash memory low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDMOK\_H}$	P	I/O low voltage detector high threshold	—	—	2.95	V
$V_{IOLVDMOK\_L}$	P	I/O low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDM5OK\_H}$	P	I/O 5V low voltage detector high threshold	—	—	4.4	V
$V_{IOLVDM5OK\_L}$	P	I/O 5V low voltage detector low threshold	—	3.8	—	V
$V_{MLVDDOK\_H}$	P	Digital supply low voltage detector high	—	—	1.15	V
$V_{MLVDDOK\_L}$	P	Digital supply low voltage detector low	—	1.08	—	V

1. V_{DD} = 3.3V ± 10% / 5.0V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified.

3.9 Power Up/Down sequencing

To prevent an overstress event or a malfunction within and outside the device, the SPC56xP54x/SPC56xP60x implements the following sequence to ensure each module is started only when all conditions for switching it ON are available:

1. A POWER_ON module working on voltage regulator supply controls the correct start-up of the regulator. This is a key module ensuring safe configuration for all voltage regulator functionality when supply is below 1.5V. Associated POWER_ON (or POR) signal is active low.
   - Several low voltage detectors, working on voltage regulator supply monitor the voltage of the critical modules (voltage regulator, I/Os, flash memory and low voltage domain). LVDs are gated low when POWER_ON is active.
   - A POWER_OK signal is generated when all critical supplies monitored by the LVD are available. This signal is active high and released to all modules including I/Os, flash memory and RC16 oscillator needed during power-up phase and reset phase. When POWER_OK is low the associated modules are set into a safe state.

Figure 10. Power-up typical sequence

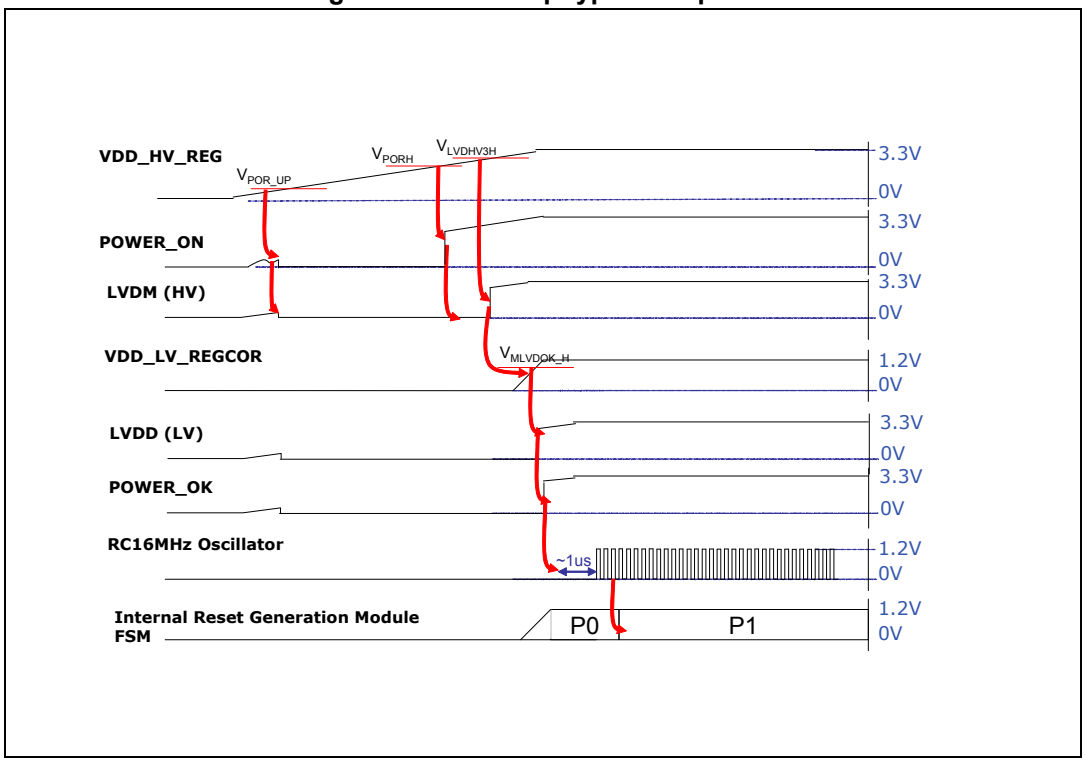


Figure 11. Power-down typical sequence

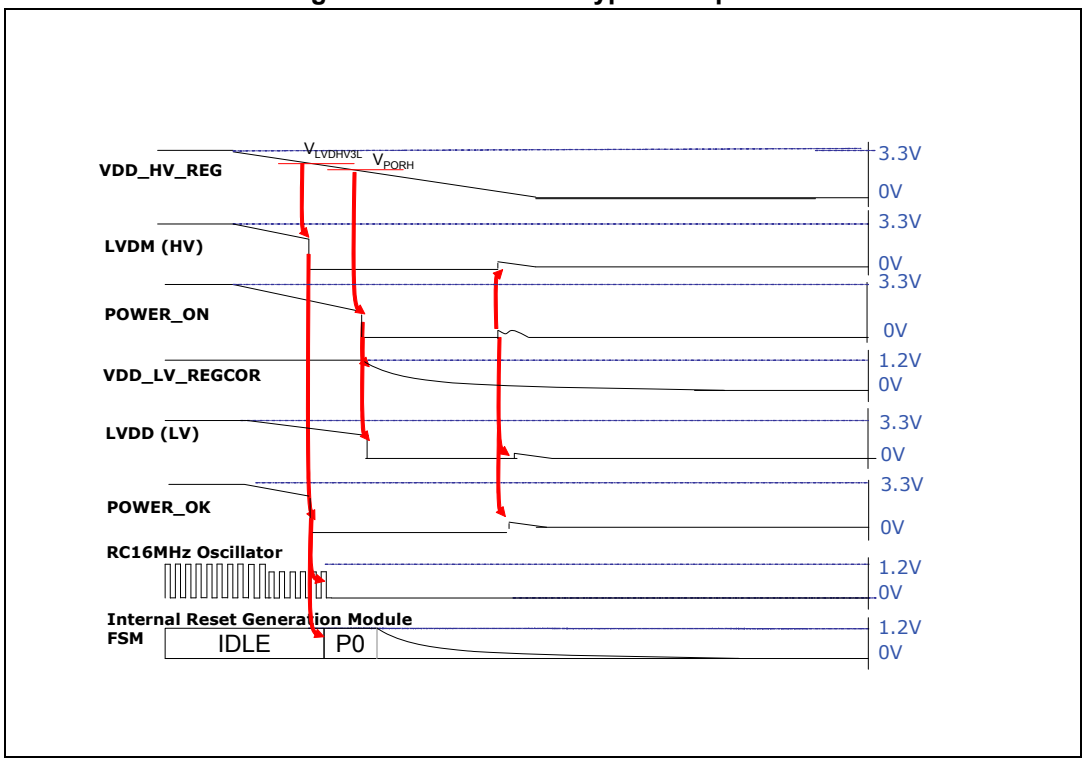


Figure 20. Start-up reset requirements(g)

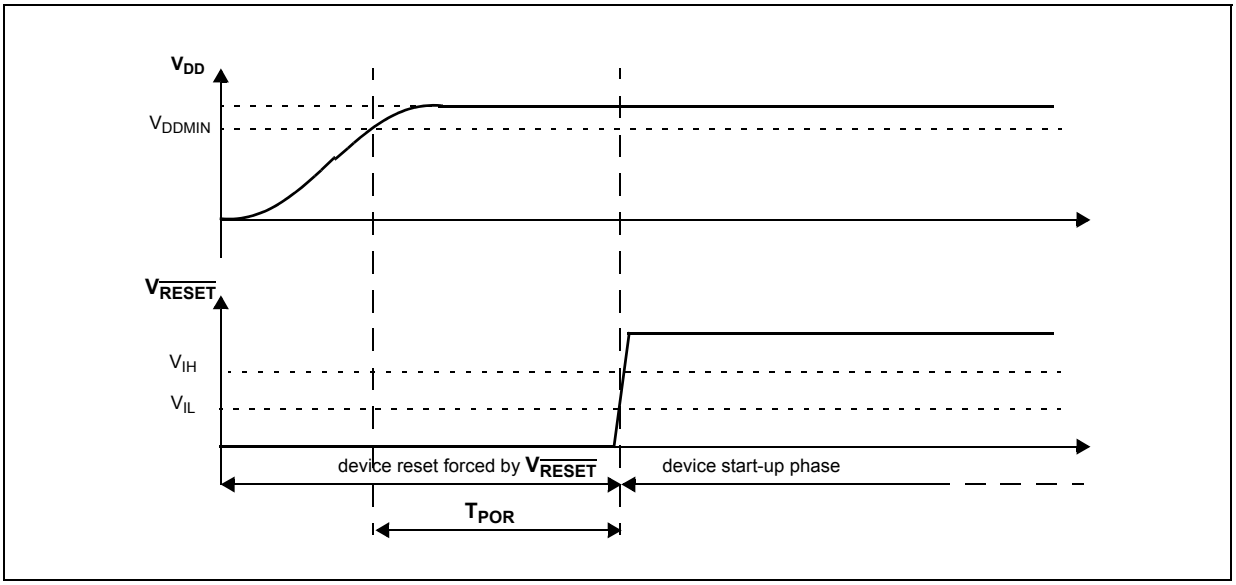
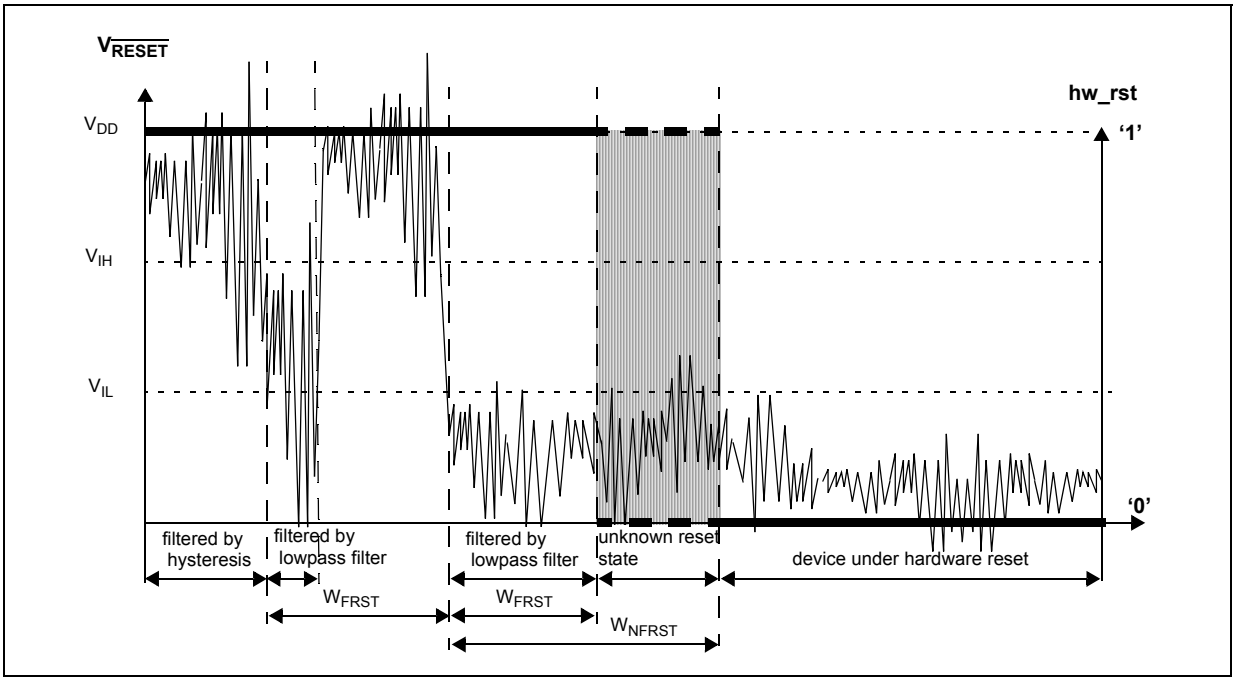


Figure 21. Noise filtering on reset signal



g. The output drive provided is open drain and hence must be terminated by an external resistor of value 1 kΩ.

Table 37. $\overline{\text{RESET}}$ electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input High Level CMOS (Schmitt Trigger)	—	$0.65V_{DD}$	—	$V_{DD}+0.4$	V
V_{IL}	SR	P	Input low Level CMOS (Schmitt Trigger)	—	–0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	$0.1V_{DD}$	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 2mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
				Push Pull, I_{OL} = 1mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
				Push Pull, I_{OL} = 1mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
T_{tr}	CC	D	Output transition time output pin[3] MEDIUM configuration	C_L = 25pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
				C_L = 50pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
				C_L = 100pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
				C_L = 25pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
				C_L = 50pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
				C_L = 100pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W_{FRST}	SR	P	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ input not filtered pulse	—	500	—	—	ns
T_{POR}	CC	D	maximum delay before internal reset is released after all VDD_HV reach nominal supply	Monotonic VDD_HV supply ramp	—	—	1	ms
$\lvert I_{WPU}\rvert$	CC	P	Weak pull-up current absolute value	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	10	—	150	µA
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	10	—	150	
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[4]	10	—	250	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified.
2. This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of device reference manual).
3. C_L includes device and package capacitance (C_{PKG} < 5 pF).
4. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Figure 30. DSPI classic SPI timing — master, CPHA = 1

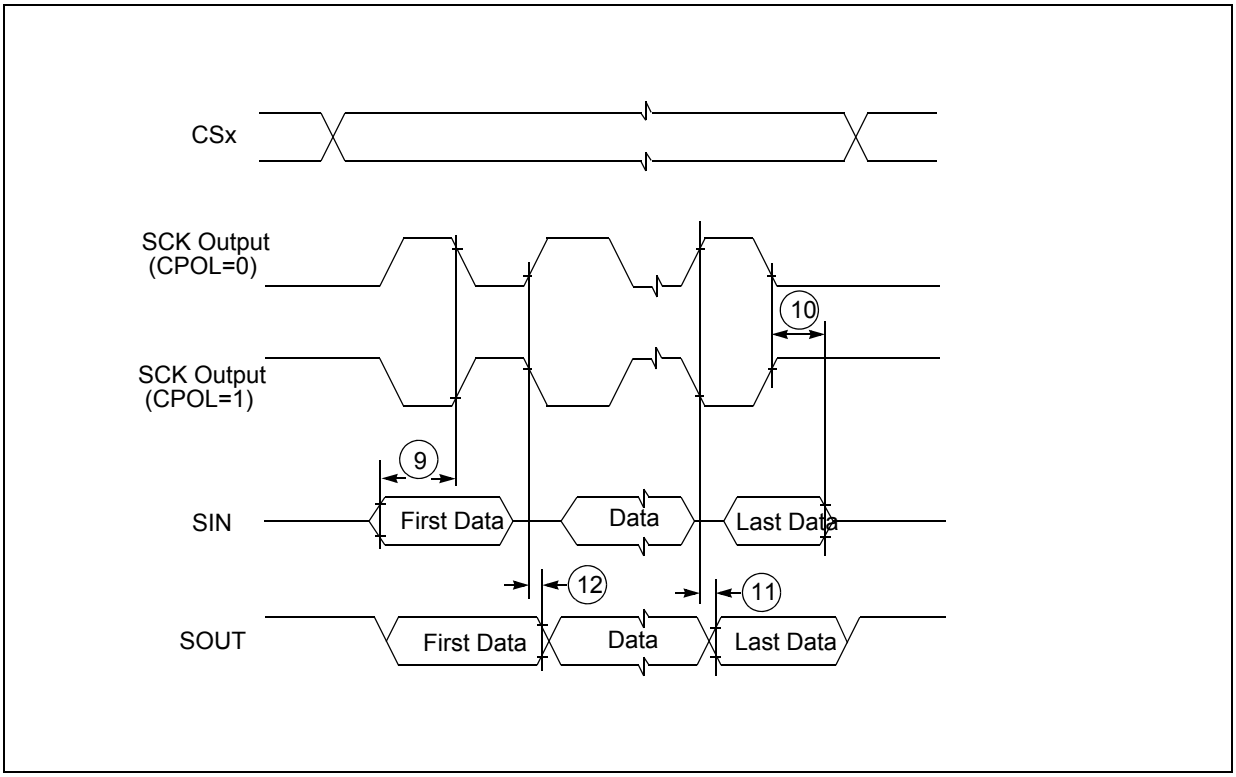
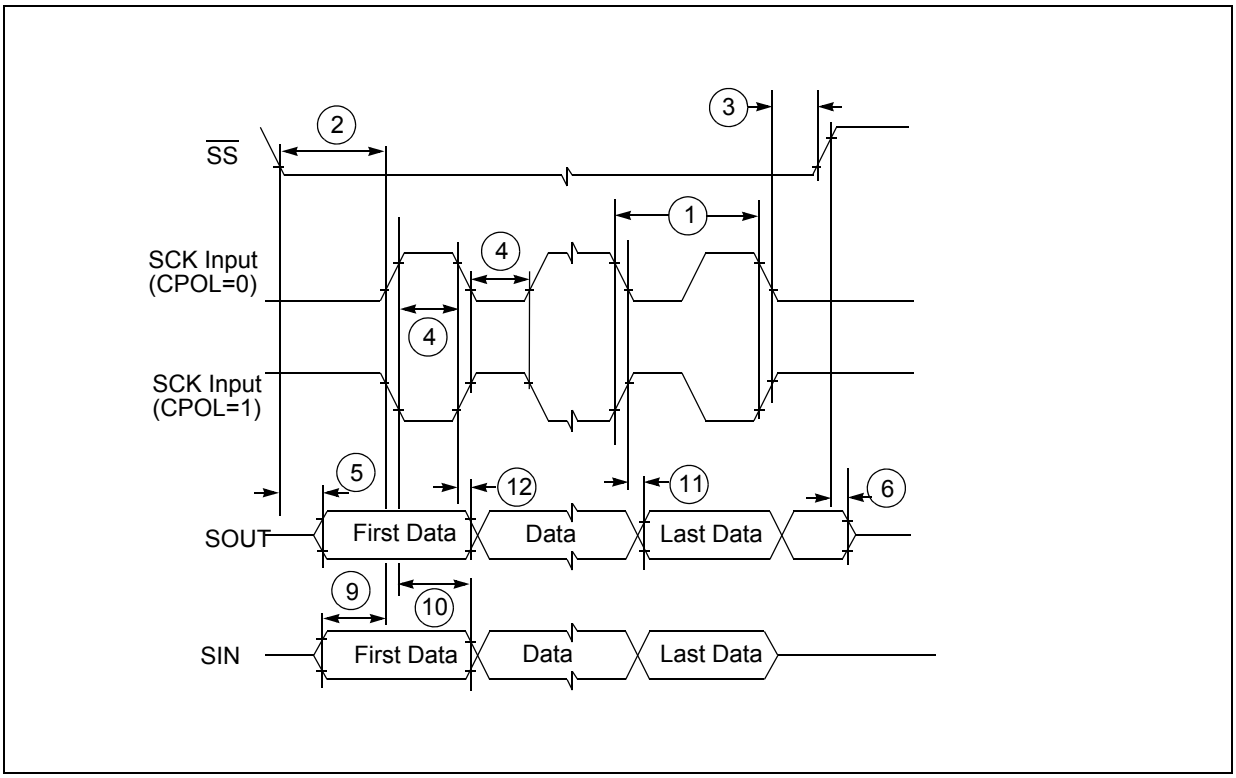


Figure 31. DSPI classic SPI timing — slave, CPHA = 0



4 Package characteristics

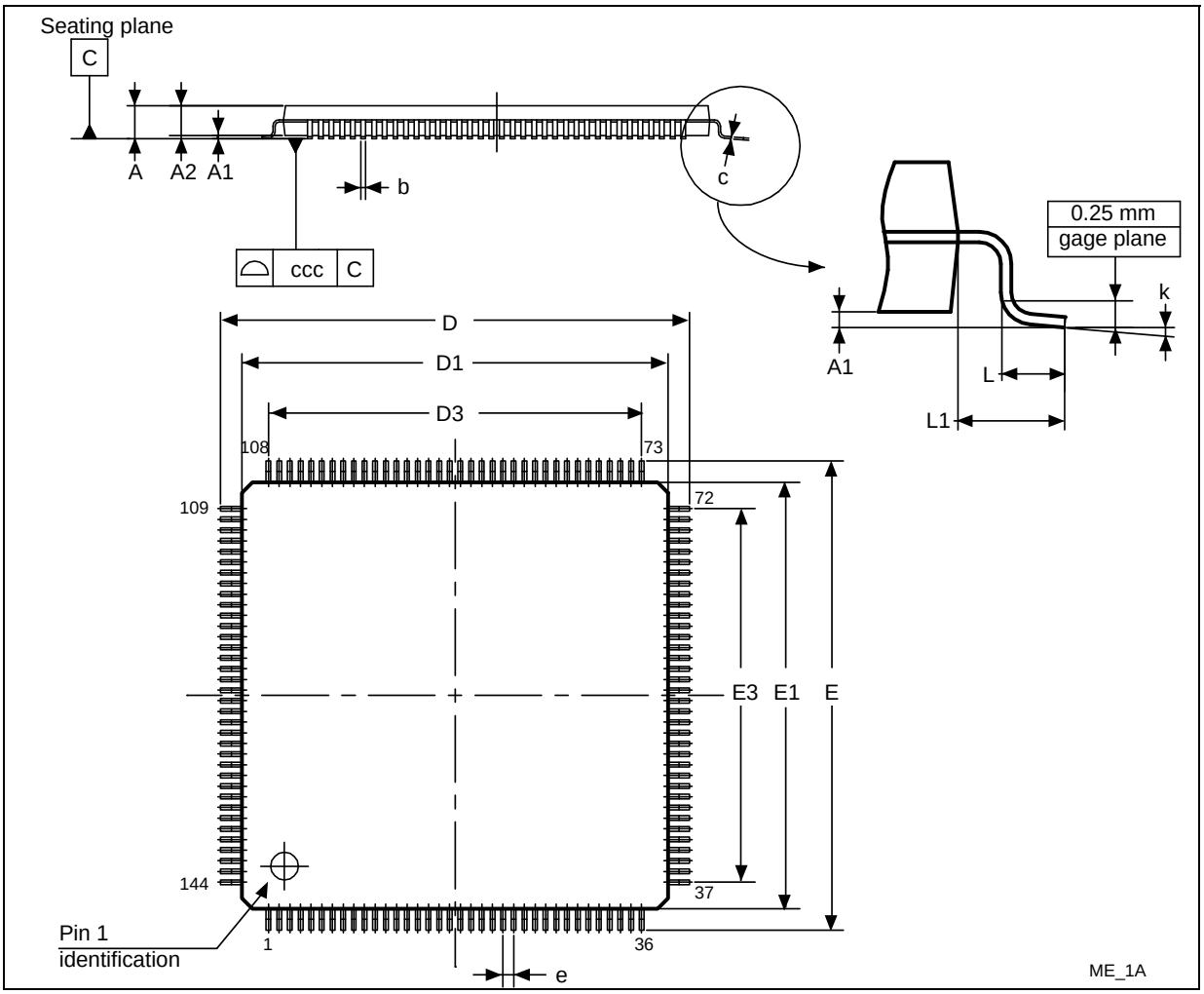
4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.2 Package mechanical data

4.2.1 LQFP144 mechanical outline drawing

Figure 38. LQFP144 package mechanical drawing



4.2.2 LQFP100 mechanical outline drawing

Figure 39. LQFP100 package mechanical drawing

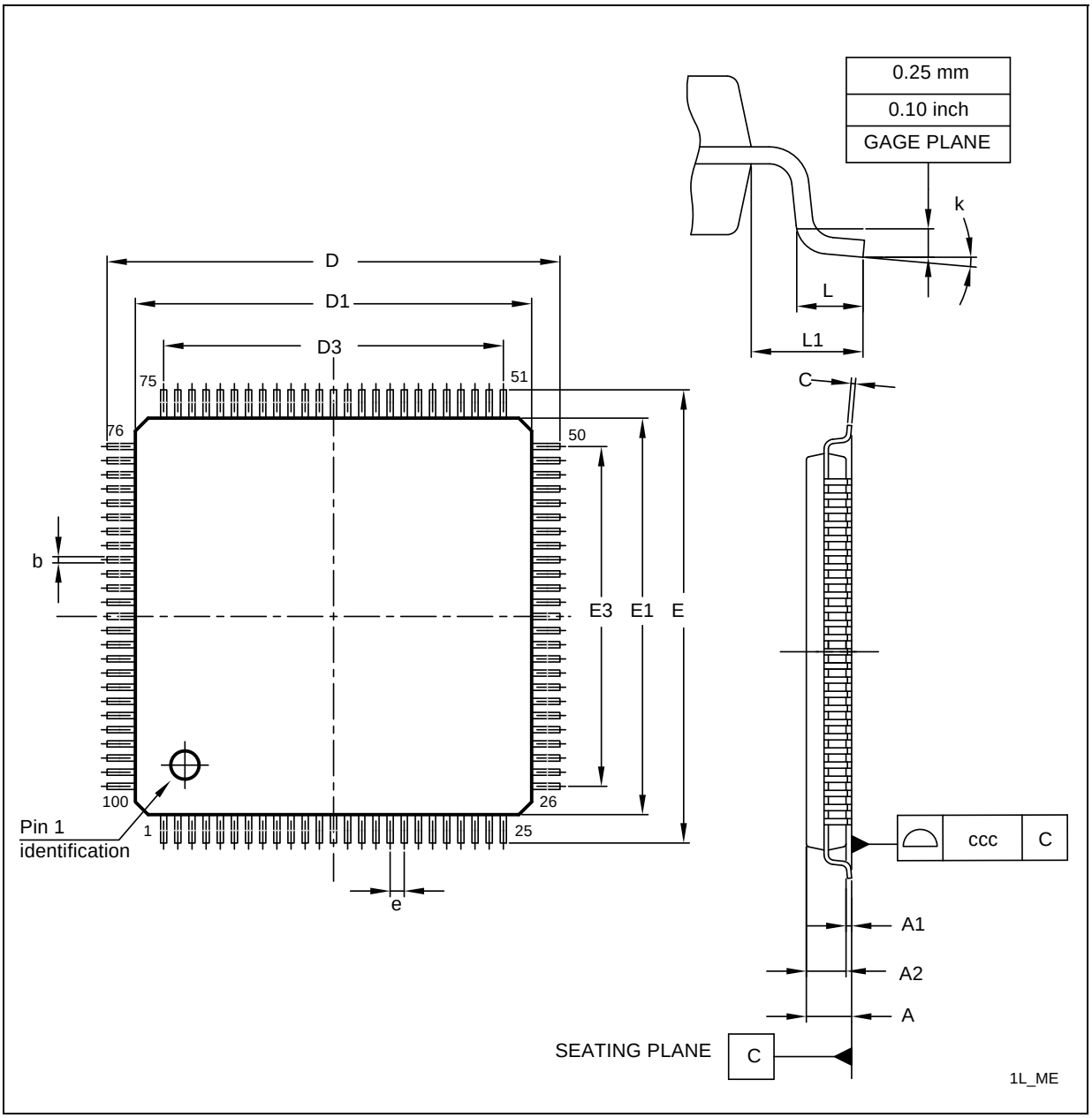


Table 43. LQFP100 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571

Table 43. LQFP100 mechanical data (continued)

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	—	12.000	—	—	0.4724	—
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	—	12.000	—	—	0.4724	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0 °	0.0 °	3.5 °	7.0 °
ccc[2]	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Tolerance.