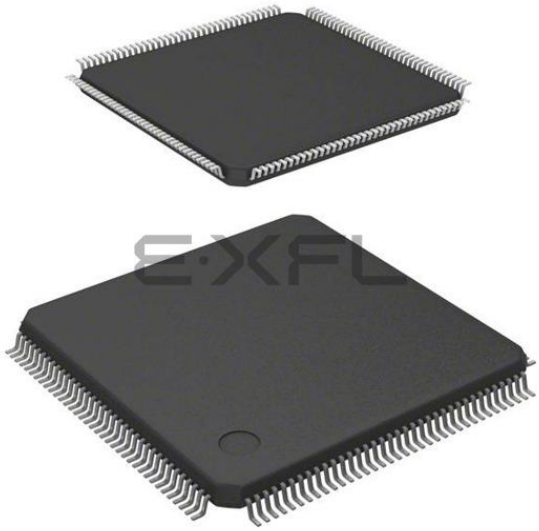

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 26x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc56ap60l5cefay

List of figures

allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

The INTC provides the following features:

- Unique 9-bit vector for each separate interrupt source
- 8 software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority.
  - Modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources.
- 2 external high priority interrupts directly accessing the main core and IOP critical interrupt mechanism

The INTC module is replicated for each processor.

1.5.7 System clocks and clock generation

The following list summarizes the system clock and clock generation on the SPC56xP54x/SPC56xP60x:

- Lock detect circuitry continuously monitors lock status
- Loss of clock (LOC) detection for PLL outputs
- Programmable output clock divider (÷1, ÷2, ÷4, ÷8)
- Programmable output clock divider (÷1, ÷2, ÷3 to ÷256)
- eTimer module running at the same frequency as the e200z0h core
- On-chip oscillator with automatic level control
- Internal 16 MHz RC oscillator for rapid start-up and safe mode
  - Supports frequency trimming by user application

1.5.8 Frequency modulated phase-locked loop (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 40 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The FMPLL multiplication factor, output clock divider ratio are all software configurable.

The FMPLL has the following major features:

- Input clock frequency from 4 MHz to 40 MHz
- Voltage controlled oscillator (VCO) range from 256 MHz to 512 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- Modulation enabled/disabled through software

1.5.21 Serial communication interface module (LINFlex)

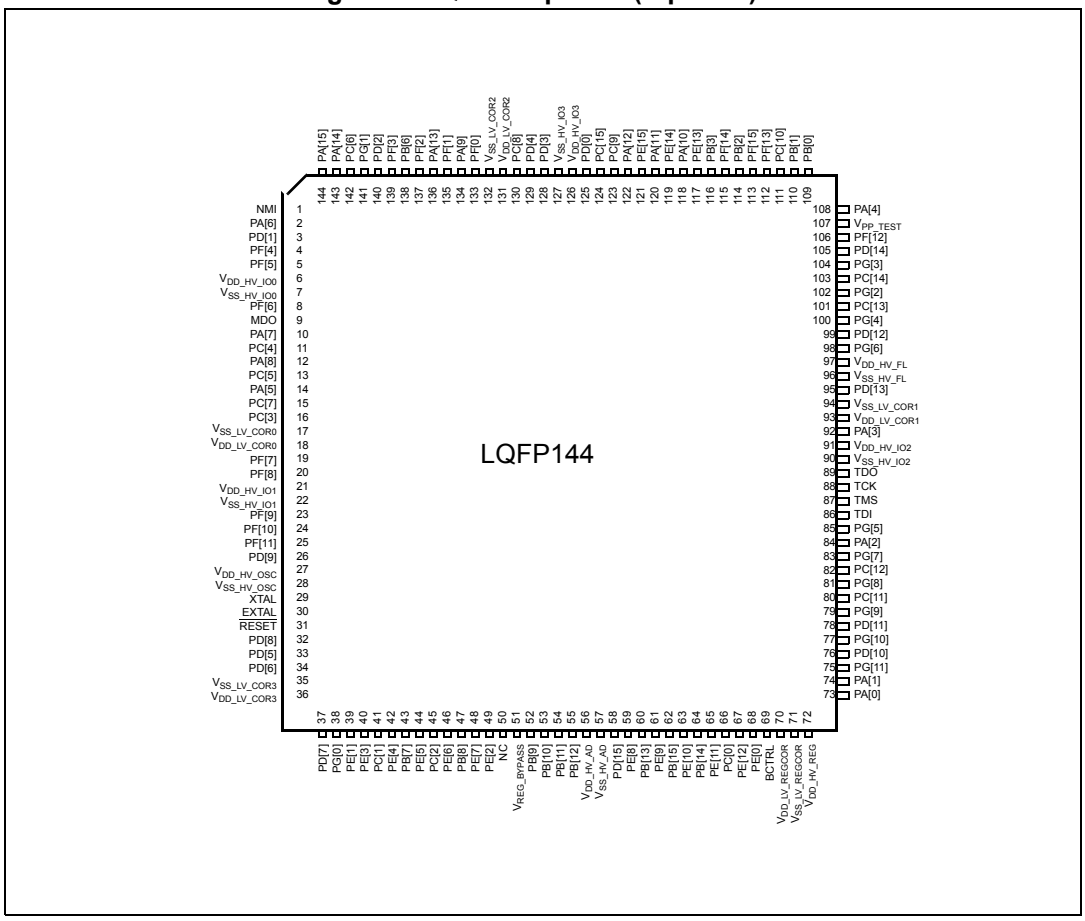
The LINFlex on the SPC56xP54x/SPC56xP60x features the following:

- Supports LIN Master mode (on both modules), LIN Slave mode (on one module) and UART mode
- LIN state machine compliant to LIN1.3, 2.0, and 2.1 Specifications
- Handles LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store Identifier and up to 8 data bytes
  - Supports message length as long as 64 bytes
  - Detection and flagging of LIN errors: Sync field; Delimiter; ID parity; Bit; Framing; Checksum and Time-out errors
  - Classic or extended checksum calculation
  - Configurable Break duration as long as 36-bit times
  - Programmable Baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features: Loop back; Self Test; LIN bus stuck dominant detection
  - Interrupt-driven operation with 16 interrupt sources
- LIN slave mode features
  - Autonomous LIN header handling
  - Autonomous LIN response handling
- UART mode
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit or 9-bit words)
  - Error detection and flagging
  - Parity, Noise and Framing errors
  - Interrupt-driven operation with four interrupt sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - 2 receiver wake-up methods

1.5.22 Deserial serial peripheral interface (DSPI)

The deserial serial peripheral interface (DSPI) module provides a synchronous serial interface for communication between the SPC56xP54x/SPC56xP60x MCU and external devices.

Figure 3. LQFP144 pinout (top view)(c)



c. Availability of port pin alternate functions depends on product selection.

Table 5. Supply pins (continued)

Supply		Pin		
Symbol	Description	LQFP 100	LQFP 144	LQFP 176[1]
$V_{SS\_LV\_COR0}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR0}$ pin.	11	17	25
$V_{DD\_LV\_COR1}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR1}$ pin.	65	93	117
$V_{SS\_LV\_COR1}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR1}$ pin.	66	94	118
$V_{DD\_LV\_COR2}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR2}$ pin.	92	131	155
$V_{SS\_LV\_COR2}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR\ 2}$ pin.	93	132	156
$V_{DD\_LV\_COR3}$	1.2 V Decoupling pins for core logic supply. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR3}$ pin.	25	36	44
$V_{SS\_LV\_COR3}$	1.2 V Decoupling pins for core logic GND. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR\ 3}$ pin.	24	35	43

1. LQFP176 available only as development package.
2. See datasheet Voltage Regulator Electrical Characteristics section for more details.

2.2.2 System pins

Table 6 and *Table 7* contain information on pin functions for the SPC56xP54x/SPC56xP60x devices. The pins listed in *Table 6* are single-function pins. The pins shown in *Table 7* are multi-function pins, programmable via their respective Pad Configuration Register (PCR) values.

Table 6. System pins

Symbol	Description	Direction	Pad Speed[1]		Pin		
			SRC=0	SRC=1	LQFP 100	LQFP 144	LQFP 176[2]
Dedicated pins							
MDO0	Nexus Message Data Output—line 0	Output Only	Fast		—	9	17
MDO4	Nexus Message Data Output—line 4	Output Only	Fast		—	—	7

Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
A[2] [8]	PCR[2]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[2] ETC[2] CS3_4 — SIN_2 ABS[0] EIRQ[2]	SIUL eTimer_0 DSPI_4 — DSPI_2 MC_RGM SIUL	I/O I/O O — I I I	Slow	Medium	57	84	102
A[3] [8]	PCR[3]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[3] ETC[3] CS0_2 — ABS[1] EIRQ[3]	SIUL eTimer_0 DSPI_2 — MC_RGM SIUL	I/O I/O I/O — I I	Slow	Medium	64	92	116
A[4] [8]	PCR[4]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[4] ETC[0] CS1_2 ETC[4] FAB EIRQ[4]	SIUL eTimer_1 DSPI_2 eTimer_0 MC_RGM SIUL	I/O I/O O I/O I I	Slow	Medium	75	108	132
A[5]	PCR[5]	ALT0 ALT1 ALT2 ALT3 —	GPIO[5] CS0_1 ETC[5] CS7_0 EIRQ[5]	SIUL DSPI_1 eTimer_1 DSPI_0 SIUL	I/O I/O I/O O I	Slow	Medium	8	14	22
A[6]	PCR[6]	ALT0 ALT1 ALT2 ALT3 —	GPIO[6] SCK_1 CS2_4 — EIRQ[6]	SIUL DSPI_1 DSPI_4 — SIUL	I/O I/O I/O — I	Slow	Medium	2	2	2
A[7]	PCR[7]	ALT0 ALT1 ALT2 ALT3 —	GPIO[7] SOUT_1 CS1_4 — EIRQ[7]	SIUL DSPI_1 DSPI_4 — SIUL	I/O O I/O — I	Slow	Medium	4	10	18
A[8]	PCR[8]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[8] — CS0_4 — SIN_1 EIRQ[8]	SIUL — DSPI_4 — DSPI_1 SIUL	I/O — I/O — I I	Slow	Medium	6	12	20

Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
E[15]	PCR[79]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[79] — — — SIN_3 EIRQ[27]	SIUL — — — DSPI_3 SIUL	I/O — — — I I	Slow	Medium	—	121	145
Port F										
F[0]	PCR[80]	ALT0 ALT1 ALT2 ALT3 —	GPIO[80] DBG_0 CS3_3 — EIRQ[28]	SIUL FlexRay_0 DSPI_3 — SIUL	I/O O O — I	Slow	Medium	—	133	157
F[1]	PCR[81]	ALT0 ALT1 ALT2 ALT3 —	GPIO[81] DBG_1 CS2_3 — EIRQ[29]	SIUL FlexRay_0 DSPI_3 — SIUL	I/O O O — I	Slow	Medium	—	135	159
F[2]	PCR[82]	ALT0 ALT1 ALT2 ALT3	GPIO[82] DBG_2 CS1_3 —	SIUL FlexRay_0 DSPI_3 —	I/O O O —	Slow	Medium	—	137	161
F[3]	PCR[83]	ALT0 ALT1 ALT2 ALT3	GPIO[83] DBG_3 CS0_3 —	SIUL FlexRay_0 DSPI_3 —	I/O O I/O —	Slow	Medium	—	139	167
F[4]	PCR[84]	ALT0 ALT1 ALT2 ALT3	— — MDO[3] —	— — nexus_0 —	— — O —	Slow	Fast	—	4	4
F[5]	PCR[85]	ALT0 ALT1 ALT2 ALT3	— — MDO[2] —	— — nexus_0 —	— — O —	Slow	Fast	—	5	13
F[6]	PCR[86]	ALT0 ALT1 ALT2 ALT3	GPIO[86] — MDO[1] —	SIUL — nexus_0 —	I/O — O —	Slow	Fast	—	8	16

Table 7. Pin muxing[1] (continued)

Port pin	PCR No.	Alternate function[2], [3]	Functions	Peripheral [4]	I/O direction [5]	Pad speed[6]		Pin		
						SRC = 0	SRC = 1	LQFP 100	LQFP 144	LQFP 176[7]
Port G										
G[0]	PCR[96]	ALT0 ALT1 ALT2 ALT3 —	GPIO[96] F[0] — — EIRQ[30]	SIUL FCCU — — SIUL	I/O O — — I	Slow	Medium	—	38	46
G[1]	PCR[97]	ALT0 ALT1 ALT2 ALT3 —	GPIO[97] F[1] — — EIRQ[31]	SIUL FCCU — — SIUL	I/O O — — I	Slow	Medium	—	141	173
G[2]	PCR[98]	ALT0 ALT1 ALT2 ALT3 —	GPIO[98] — — — SIN_4	SIUL — — — DSPI_4	I/O — — — I	Slow	Medium	—	102	126
G[3]	PCR[99]	ALT0 ALT1 ALT2 ALT3	GPIO[99] — SOUT_4 —	SIUL — DSPI_4 —	I/O — O —	Slow	Medium	—	104	128
G[4]	PCR[100]	ALT0 ALT1 ALT2 ALT3	GPIO[100] — SCK_4 —	SIUL — DSPI_4 —	I/O — I/O —	Slow	Medium	—	100	124
G[5]	PCR[101]	ALT0 ALT1 ALT2 ALT3	GPIO[101] — CS0_4 —	SIUL — DSPI_4 —	I/O — I/O —	Slow	Medium	—	85	103
G[6]	PCR[102]	ALT0 ALT1 ALT2 ALT3	GPIO[102] — CS1_4 —	SIUL — DSPI_4 —	I/O — O —	Slow	Medium	—	98	122
G[7]	PCR[103]	ALT0 ALT1 ALT2 ALT3	GPIO[103] — CS2_4 —	SIUL — DSPI_4 —	I/O — O —	Slow	Medium	—	83	101

3 Electrical characteristics

3.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This can be done by the internal pull-up or pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

Caution: All of the following parameter values can vary depending on the application and must be confirmed during silicon validation, silicon characterization or silicon reliability trial.

3.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 8* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 8. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

Table 26. I/O consumption (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{RMSFST}	CC	D	Root medium square I/O current for FAST configuration	C_L = 25 pF, 40 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	22	mA
				C_L = 25 pF, 64 MHz		—	—	33	
				C_L = 100 pF, 40 MHz		—	—	56	
				C_L = 25 pF, 40 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C_L = 25 pF, 64 MHz		—	—	20	
				C_L = 100 pF, 40 MHz		—	—	35	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

3.12 Main oscillator electrical characteristics

The SPC56xP54x/SPC56xP60x provides an oscillator/resonator driver.

Table 27. Main oscillator electrical characteristics (5.0 V, NVUSRO[PAD3V5V]=0)

Symbol		Parameter	Min	Max	Unit
f_{OSC}	SR	Oscillator frequency	4	40	MHz
g_m	P	Transconductance	6.5	25	mA/V
V_{OSC}	T	Oscillation amplitude on EXTAL pin	1	—	V
t_{OSCSU}	T	Start-up time[1],[2]	8	—	ms

1. The start-up time is dependent upon crystal characteristics, board leakage, etc., high ESR and excessive capacitive loads can cause long start-up time.
2. Value captured when amplitude reaches 90% of EXTAL.

Table 28. Main oscillator electrical characteristics (3.3 V, NVUSRO[PAD3V5V]=1)

Symbol		Parameter	Min	Max	Unit
f_{OSC}	SR	Oscillator frequency	4	40	MHz
g_m	P	Transconductance	4	20	mA/V
V_{OSC}	T	Oscillation amplitude on EXTAL pin	1	—	V
t_{OSCSU}	T	Start-up time[1],[2]	8	—	ms

1. The start-up time is dependent upon crystal characteristics, board leakage, etc., high ESR and excessive capacitive loads can cause long start-up time.
2. Value captured when amplitude reaches 90% of EXTAL.

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Equation 5

$$\tau_1 = (R_{SW} + R_{AD}) \times \frac{C_P \times C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Equation 6

$$\tau_1 < (R_{SW} + R_{AD}) \times C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to *Equation 7*:

Equation 7

$$V_{A1} \times (C_S + C_{P1} + C_{P2}) = V_A \times (C_{P1} + C_{P2})$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Equation 8

$$\tau_2 < R_L \times (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraint on R_L sizing is obtained:

Equation 9

$$8.5 \times \tau_2 = 8.5 \times R_L \times (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. *Equation 10* must be respected (charge balance assuming now C_S already charged at V_{A1}):

Equation 10

$$V_{A2} \times (C_S + C_{P1} + C_{P2} + C_F) = V_A \times C_F + V_{A1} \times (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on

Table 32. ADC conversion characteristics (continued)

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
TUE	T	Total unadjusted error with current injection	16 precision channels	–3	—	3	LSB
TUE	T	Total unadjusted error with current injection	10 standard channels	–4	—	4	LSB

1. V_{DD} = 3.3 V to 3.6 V / 4.5 V to 5.5 V, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified and analog input voltage from $V_{SS\_HV\_AD}$ to $V_{DD\_HV\_AD}$.
2. V_{INAN} may exceed V_{SS_ADC} and V_{DD_ADC} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.
3. AD_clk clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
4. When configured to allow 60 MHz ADC, the minimum ADC clock speed is 9 MHz, below which precision is lost.
5. During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC_S}. After the end of the sample time t_{ADC_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC_S} depend on programming.
6. This parameter includes the sample time t_{ADC_S}.
7. 20 MHz ADC clock. Specific prescaler is programmed on MC_PLL_CLK to provide 20 MHz clock to the ADC.
8. See *Figure 16*.

3.16 Flash memory electrical characteristics

Table 33. Program and erase specifications

Symbol		Parameter	Conditions	Value				Unit
				Min	Typ[1]	Initial max[2]	Max[3]	
$T_{wprogram}$	P	Word Program (32 bits) Time[4]	Data Flash	—	30	70	500	µs
$T_{dwprogram}$	P	Double Word (64 bits) Program Time[4]	Code Flash	—	18	50	500	µs
T_{BKPRG}	P	Bank Program (64 KB)[4, 5]	Data Flash	—	0.49	1.2	4.1	s
	P	Bank Program (1056 KB)[4, 5]	Code Flash	—	2.6	6.6	66	s
T_{MDPRG}	P	Module Program (512 KB)[4]	Code Flash	—	1.3	1.65	33	s
$T_{16kpperase}$	P	16 KB Block Pre-program and Erase Time	Code Flash	—	200	500	5000	ms
			Data Flash		700	800		
$T_{32kpperase}$	P	32 KB Block Pre-program and Erase Time	Code Flash	—	300	600	5000	ms
$T_{64kpperase}$	P	64 KB Block Pre-program and Erase Time	Code Flash	—	400	900	5000	ms
$T_{128kpperase}$	P	128 KB Block Pre-program and Erase Time	Code Flash	—	600	1300	5000	ms
t_{ESRT}	P	Erase Suspend Request Rate[6]	Code Flash	20	—	—	—	ms
			Data Flash	10				

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3.18.2 IEEE 1149.1 interface timing

Table 38. JTAG pin AC electrical characteristics

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	CC	D	TCK cycle time	—	100	—	ns
2	t_{JDC}	CC	D	TCK clock pulse width (measured at $V_{DD\_HV\_IOx}/2$)	—	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40% – 70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	—	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO data valid	—	—	40	ns
7	t_{TDOI}	CC	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	CC	D	TCK low to TDO high impedance	—	40	—	ns
9	t_{BSDV}	CC	D	TCK falling edge to output valid	—	—	50	ns
10	t_{BSDVZ}	CC	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
11	t_{BSDHZ}	CC	D	TCK falling edge to output high impedance	—	—	50	ns
12	t_{BSDST}	CC	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
13	t_{BSDHT}	CC	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

Figure 22. JTAG test clock input timing

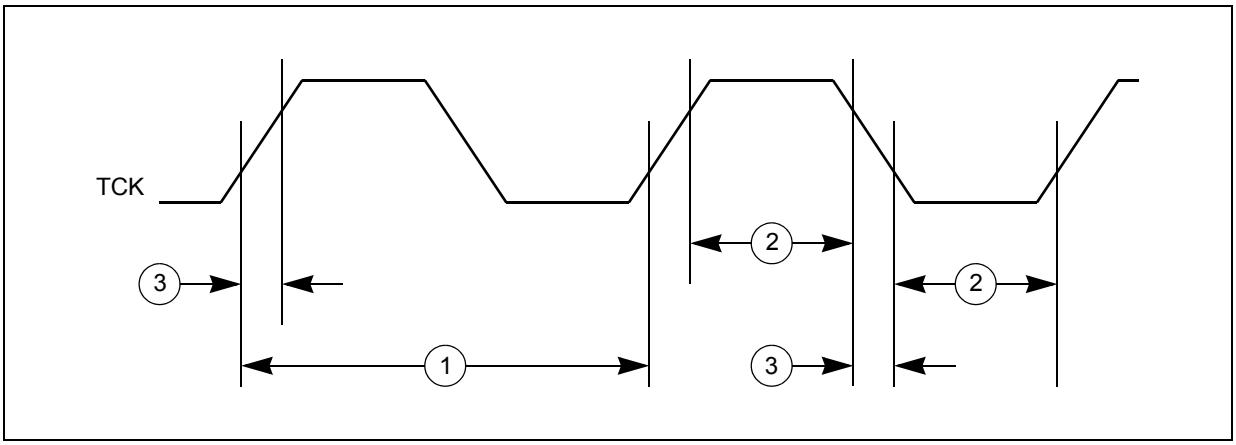
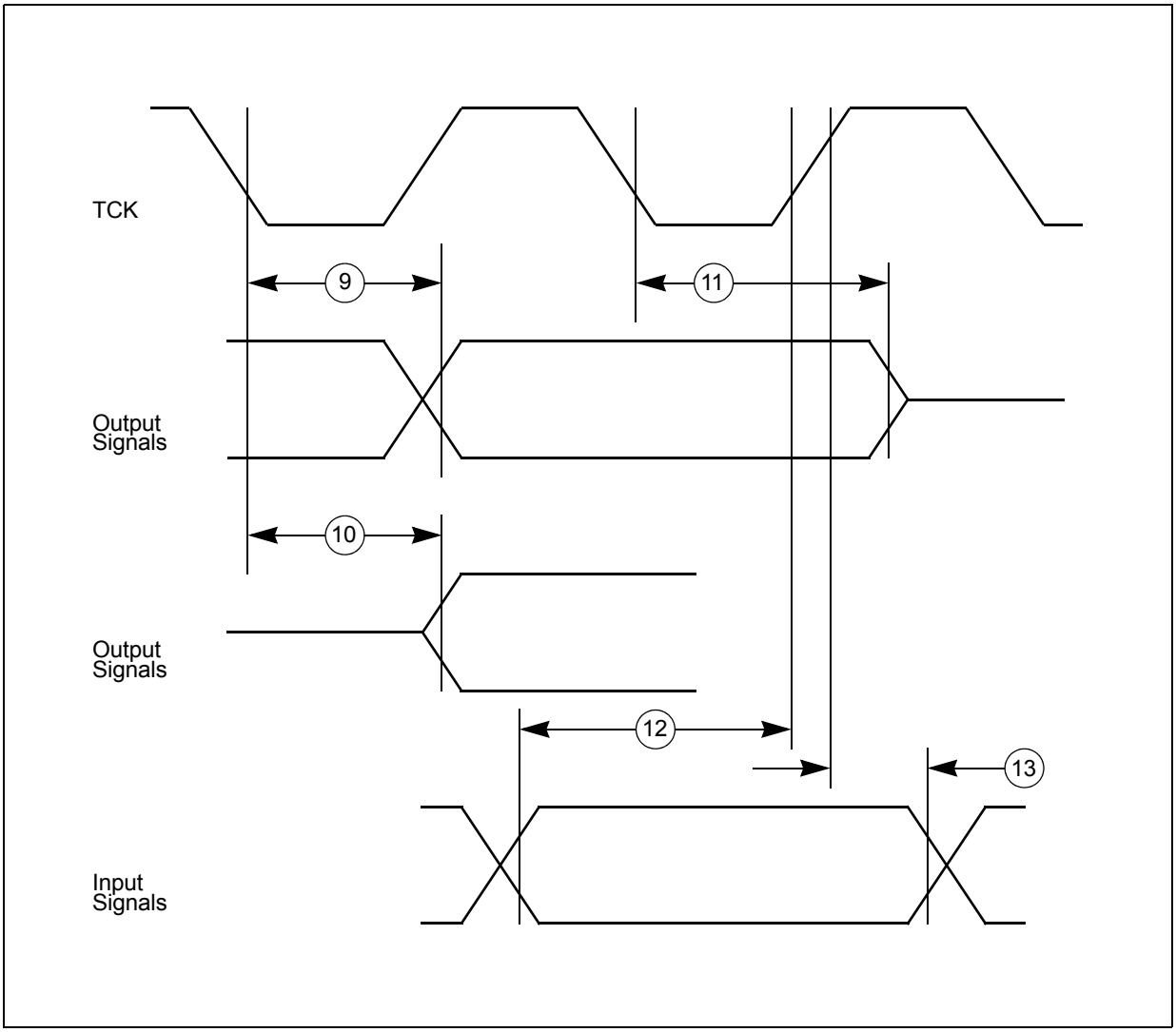


Figure 24. JTAG boundary scan timing



3.18.3 Nexus timing

Table 39. Nexus debug port timing(1)

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{MCYC}	CC	D	MCKO cycle time	32	—	—	ns
2	t_{MDOV}	CC	D	MCKO edge to MDO data valid	–0.1 × t_{MCYC}	—	0.25 × t_{MCYC}	ns
3	t_{MSEOV}	CC	D	MCKO edge to $\overline{\text{MSEO}}$ data valid	–0.1 × t_{MCYC}	—	0.25 × t_{MCYC}	ns
4	t_{EVTOV}	CC	D	MCKO edge to $\overline{\text{EVTO}}$ data valid	–0.1 × t_{MCYC}	—	0.25 × t_{MCYC}	ns
5	t_{TCYC}	CC	D	TCK cycle time	64(2)	—	—	ns

Figure 32. DSPI classic SPI timing — slave, CPHA = 1

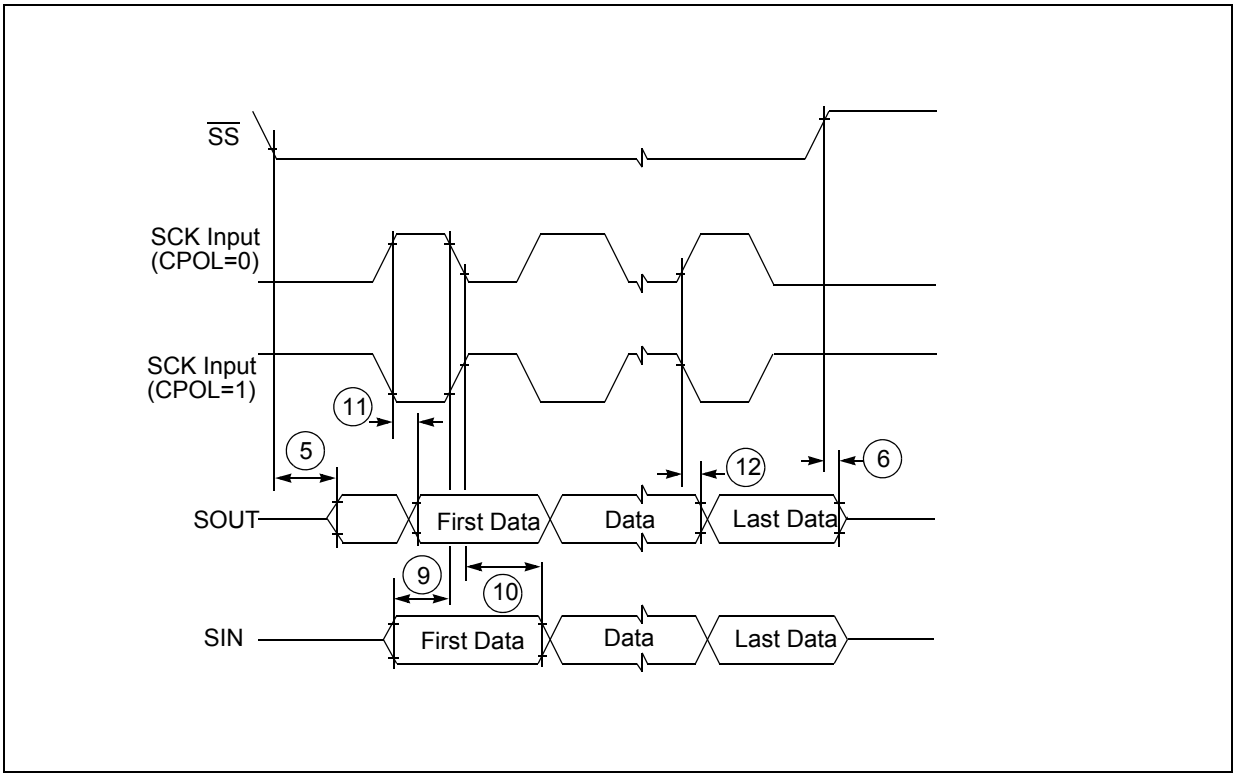


Figure 33. DSPI modified transfer format timing — master, CPHA = 0

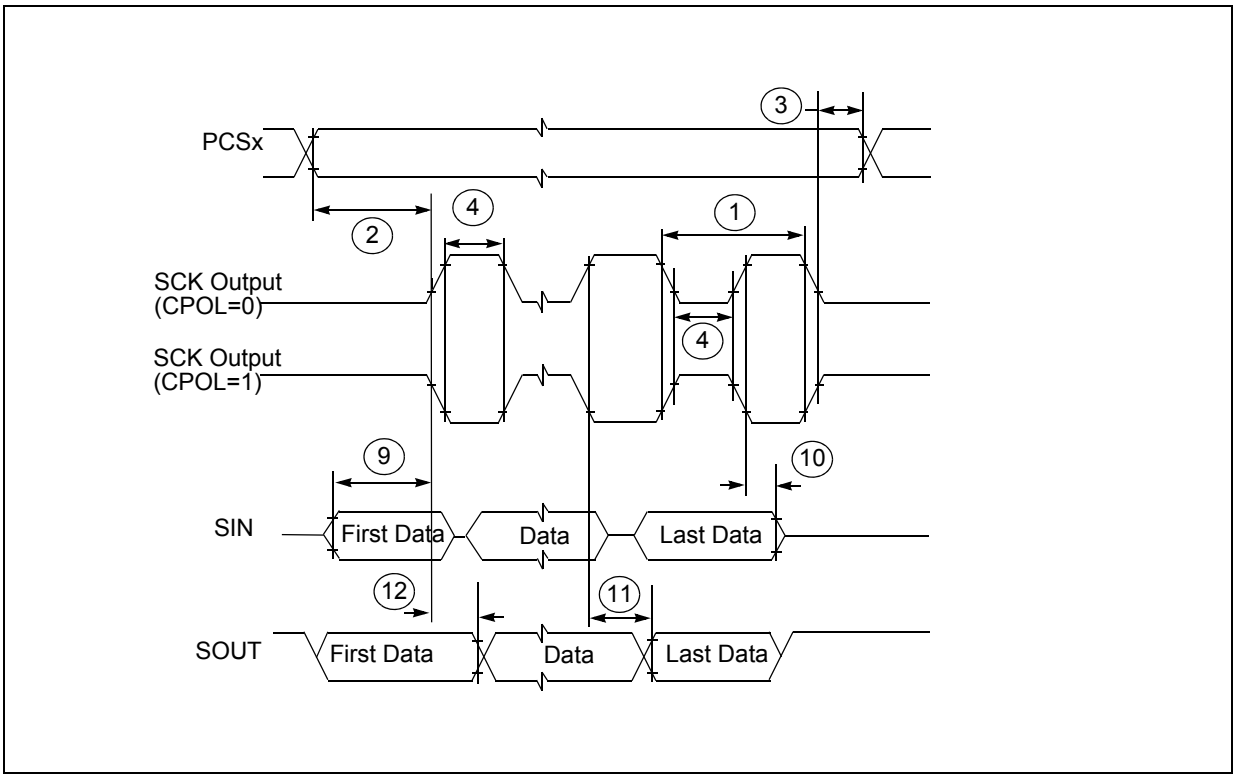


Table 42. LQFP144 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	—	17.500	—	—	0.6890	—
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	—	17.500	—	—	0.6890	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0°	3.5 °	0.0 °	7.0 °
ccc[2]	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Tolerance.

Table 43. LQFP100 mechanical data (continued)

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	—	12.000	—	—	0.4724	—
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	—	12.000	—	—	0.4724	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0 °	0.0 °	3.5 °	7.0 °
ccc[2]	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Tolerance.

Table 44. Document revision history (continued)

Date	Revision	Substantive changes
15-May-2012	3	Removed “Enhanced Full-featured” version. In the cover page, added “(1 × Master/Slave, 1 × Master Only)“ at the end of the bullet “2 LINFlex modules (LIN 2.1)” *Table 2: SPC56xP54x/SPC56xP60x device comparison*, updated the value of “LINFLEX module” to “2 (1 × Master/Slave, 1 × Master only)” *Section 1.5.4: On-chip flash memory with ECC* replaced two occurrences of “3 wait states” to “2 wait states” replaced 60 MHz to 64 MHz *Section 1.5.21: Serial communication interface module (LINFlex)*, updated first bullet to “Supports LIN Master mode (on both modules), LIN Slave mode (on one module) and UART mode” *Section 1.5.24: Analog-to-digital converter (ADC)*, removed bullet concerning the analog watchdogs from Normal mode features. *Table 5: Supply pins*, removed V_{REG_BYPASS} row. *Table 6: System pins*: added V_{REG_BYPASS} row added a footnote about $\overline{RESET}$ *Table 9: Absolute maximum ratings*: changed typical value of TV_{DD} to 0.25 and added a footnote added V_{INAN} entry Updated *Section 3.8.1: Voltage regulator electrical characteristics* Updated *Table 14: EMI testing specifications* *Table 18: Low voltage monitor electrical characteristics*, changed maximum value of $V_{MLVDDOK\_H}$ to 1.15 *Table 20: DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V]=0)*, added IPU and IPD rows for $\overline{RESET}$ pin. *Table 21: Supply current (5.0 V, NVUSRO[PAD3V5V]=0)*: added maximum values of $I_{DD\_LV\_CORE}$ for: RUN, HALT, and STOP mode updated values and parameter classification of I_{DD_FLASH} *Table 22: DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V]=1)*, added IPU and IPD rows for $\overline{RESET}$ pin. *Table 23: Supply current (3.3 V, NVUSRO[PAD3V5V]=1)*: added maximum values of $I_{DD\_LV\_CORE}$ for: RUN, HALT, and STOP mode updated values and parameter classification of I_{DD_FLASH} Added *Table 26: I/O consumption* *Table 31: 16 MHz RC oscillator electrical characteristics*, changed minimum and maximum values of Δ_{RCMVAR} respectively to -6 and 6. Renamed *Figure 16: Input equivalent circuit (precise channels)* (was “Input equivalent circuit”) Added *Figure 17: Input equivalent circuit (extended channels)* *Section 3.15.1: Input impedance and ADC accuracy*, updated *Equation 4* and *Equation 10* *Table 32: ADC conversion characteristics*, added V_{INAN}, C_{P3} and R_{SW2} rows