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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z380C
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	20MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	144-LQFP
Supplier Device Package	144-VQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8038220asc

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Table 1. Pin Numbers and Input/Output Classifications (Continued)

Pin	Input Class[1]	Output Class[1]	Pin Number(s)
$\overline{\text{INT0-3}}$	R		136 - 139
$\overline{\text{IORD}}$	I	3	125
$\overline{\text{IORQ}}$	I	3	115
$\overline{\text{IOWR}}$	I	3	123
$\overline{\text{M1}}$	I	3	116
$\overline{\text{MRD}}$	I	3	126
$\overline{\text{MSIZE}}$	I	D	117
$\overline{\text{MWR}}$	I	3	124
$\overline{\text{NMI}}$	R		135
$\overline{\text{RAMCSL}}$		O	43
$\overline{\text{RESET}}$	R	D	134
$\overline{\text{ROMCS}}$	O		42
$\overline{\text{RTS0}}$/HINT2/STSCHG		H	88
$\overline{\text{STNBY}}$		O	120
$\overline{\text{TXEN1-0}}$/$\overline{\text{RTS1-0}}$		O	94 -93
$\overline{\text{WAIT}}$	I	D	130
A23-0	I	3	141 - 144, 1 - 4, 6 - 13, 15 - 22
BUSCLK		H	127
CKA0/HDRQ1/PCRESET	I	H	92
CKA1/HA10	I	3	65
CKS/HA11	I	3	64
CLKI	R		128
CLKO		O	129
D15-0	I	3	24 - 31, 33 - 40
DCL/RXC2/BCL2	I		106
DD/TXD2	I	D (DD) O (TXD2)	107
DU/TXC2/FSC2	I	D (DU) O (TXC2, FSC2)	105
FSC/RXD2	I		108

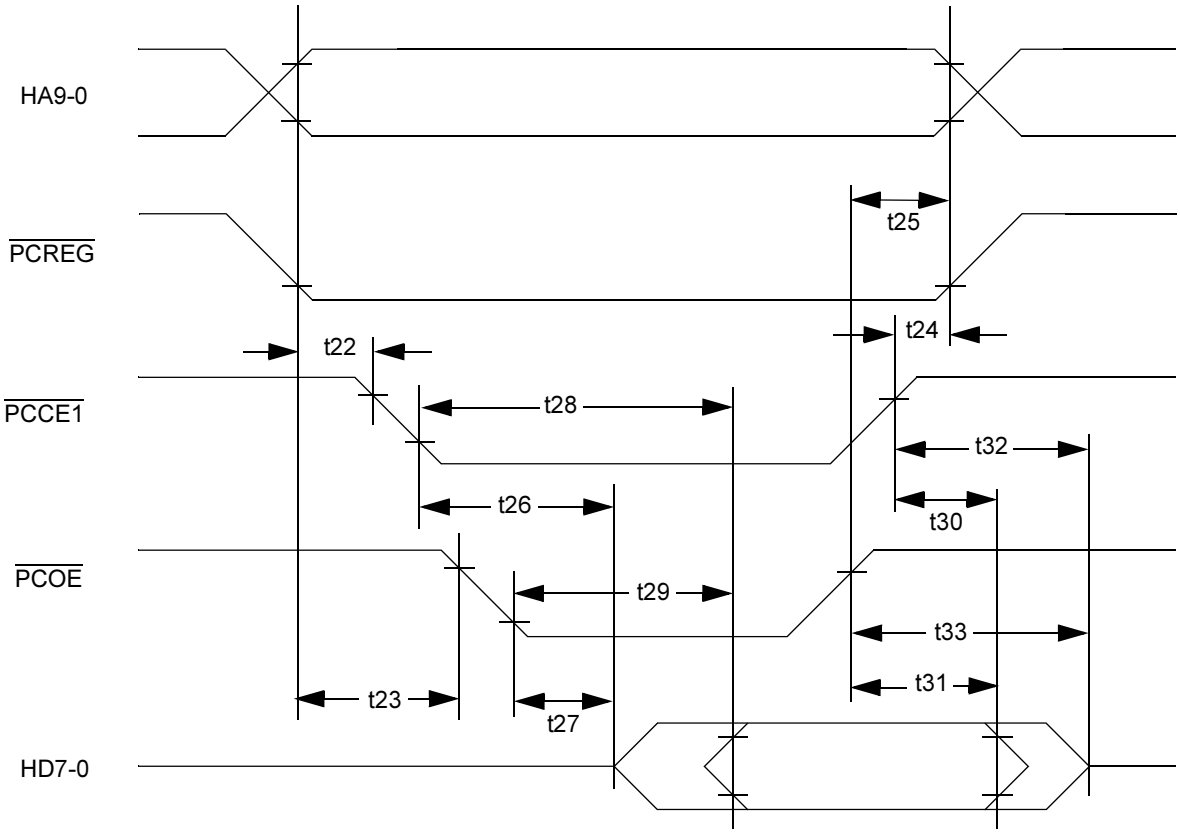

Figure 5. Host - PCMCIA Attribute Memory Read Timing Diagram

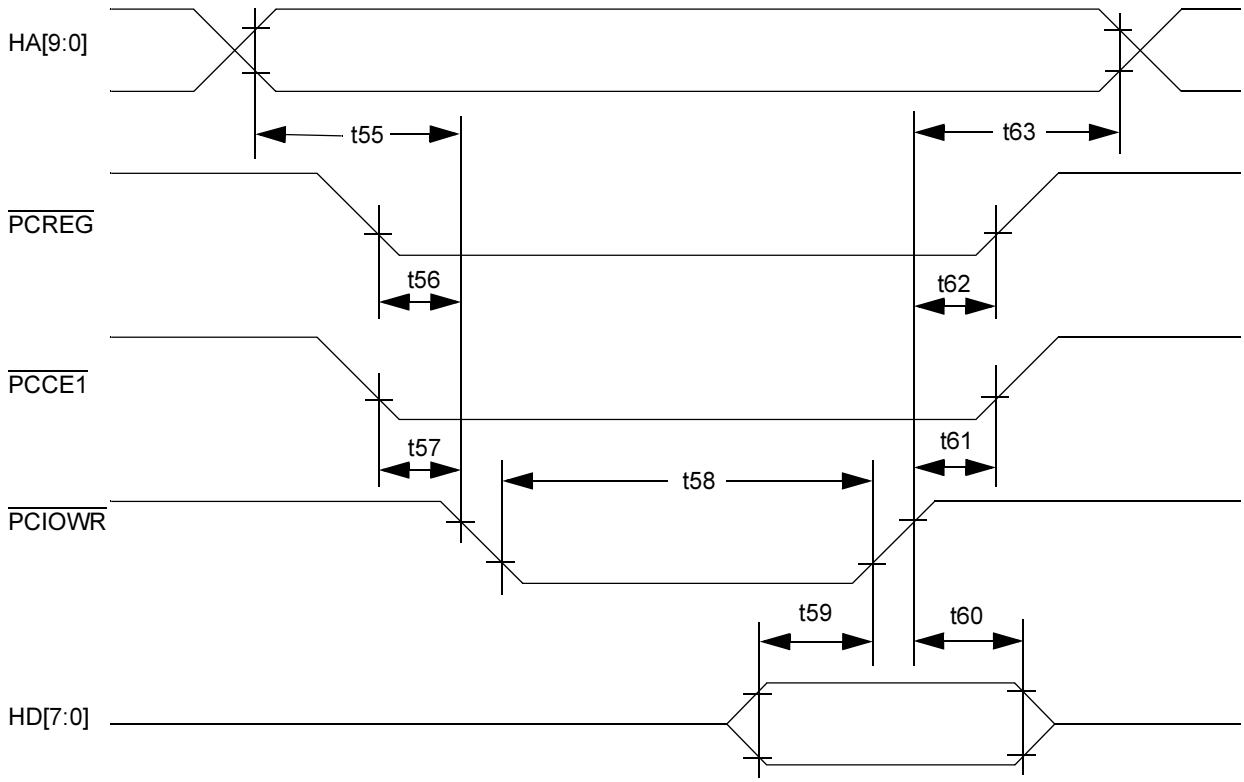

Figure 8. Host - PCMCIA I/O Write Timing Diagram

Timer Output Timing (See Figure 9)

Specifications apply over Standard Operating Conditions unless otherwise noted. C_L = 50 pF for outputs.

Table 10. Timer Output Timing

		Z80382		Z8L382		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t64	BUSCLK Low to TOUT Valid		20		20	ns

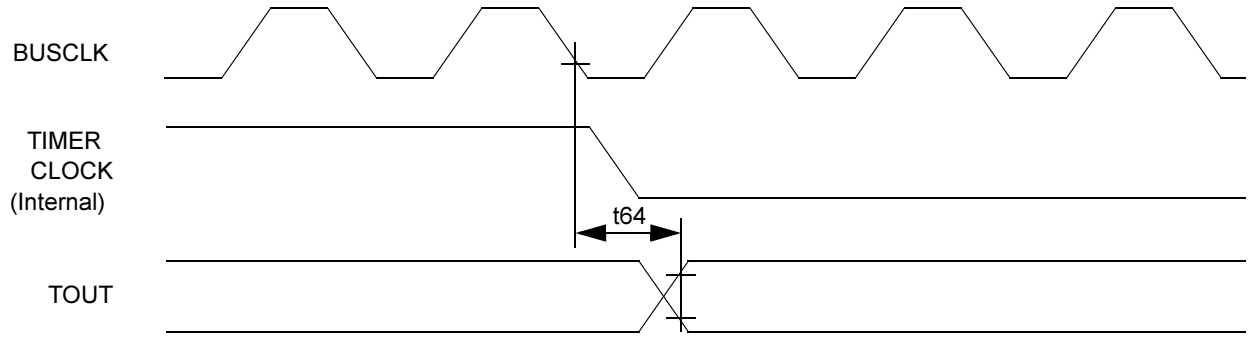

Figure 9. Timer Output Timing Diagram

HDLC Timing - Non-GCI TDM mode (See Figure 20)

Specifications apply over Standard Operating Conditions unless otherwise noted.
C_L = 50 pF for outputs

Table 18. HDLC Timing - Non-GCI TDM Mode

		Z80382		Z8L382		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t120	FSC Setup to BCL Fall	30		50		ns
t121	FSC Hold from BCL Low	20		30		ns
t122	BCL Period	50		50		ns
t123	BCL High Time	15		15		ns
t124	BCL Low Time	15		15		ns
t125	BCL High to $\overline{\text{TxEN}}$ Low		15		20	ns
t126	BCL High to $\overline{\text{TxEN}}$ High		15		20	ns
t127	BCL High to TxD Valid		15		20	ns
t128	BCL High to TxD Invalid	15		20		ns
t129	RxD Setup to BCL Fall (Rise)[1]	15		20		ns
t130	RxD Hold from BCL Low (High)[1]	5		5		ns

Note: 1. Receive clock sampling edge is configurable by means of RIRn[6]. See Z80382 User Manual.

Table 19. GCI/SCIT Timing - Slave Characteristics (Continued)

Symbol	Parameter	Z80382		Z8L382		Units
		Min.	Max.	Min.	Max.	
t137	FSC High to DU/DD Transmit Data Valid		15		20	ns
t138	DU/DD Receive Data Setup to DCL Fall	15		20		ns
t139	DU/DD Receive Data Hold from DCL Low	0		0		ns

GCI/SCIT Timing - Master Characteristics (See Figure 21)

Specifications apply over Standard Operating Conditions unless otherwise noted. C_L = 50 pF for outputs.

Table 20. GCI/SCIT Timing - Master Characteristics

Symbol	Parameter	Z80382		Z8L382		Units
		Min.	Max.	Min.	Max.	
t131	DCL Data Clock Rise/Fall Time		5		10	ns
t132	DCL Clock Period	50		50		ns
t133	DCL Pulse Width High	15		15		ns
t134	FSC Setup to DCL Fall	30		30		ns
t135	FSC Hold from DCL Low	5		10		ns
t136	DCL High to DU/DD Transmit Data Valid		15		20	ns
t137	FSC High to DU/DD Transmit Data Valid		15		20	ns
t138	DU/DD Receive Data Setup to DCL Fall	15		20		ns
t139	DU/DD Receive Data Hold from DCL Low	0		0		ns
t140	FSC High from DCL High	0		0		ns

Table 21. Multiprocessor Unit (MPU) Signals

Pin Name	Pin Number(s)	Description
A23 - 0	141 - 144, 1 - 4, 6 - 13, 15 - 22	**Address Bus** (outputs, active High, 3-state): These non-multiplexed address signals provide a linear memory address space of 16 MB. The address signals are also used to access I/O devices.
$\overline{\text{BUSACK}}$	132	**Bus Acknowledge** (output, active Low, 3-state): This signal, when asserted, indicates that the 380C has accepted an external bus request and has 3-stated its output drivers for the address bus, databus and the bus control signals TREFR, TREFA, TREFC, BHEN, BLEN, MRD, MWR, IORQ, IORD, and IOWR. The 380C cannot provide any DRAM refresh transactions while it is in the bus acknowledge state.
$\overline{\text{BHEN}}$	118	**Byte High Enable** (output, active Low, 3-state): This signal is asserted at the beginning of a memory or refresh transaction, to request an operation on D15-8. If software initiates a 16-bit memory operation, but MSIZE is asserted indicating a byte-wide memory, only the data on D7-0 is transferred in the current transaction, and another transaction is performed to transfer the other data byte, also on D7-0. See note in the next paragraph under BLEN pin description.
$\overline{\text{BLEN}}$	119	**Byte Low Enable** (output, active Low, 3-state): This signal is asserted at the beginning of a memory or refresh transaction, to request an operation on D7-0. If software initiates a 16-bit memory transaction, but MSIZE is asserted indicating a byte-wide memory, only the data on D7-0 is transferred in the current transaction, and another transaction is performed to transfer the other data byte, also on D7-0. Note: To align Z382 documentation and terminology with historical Z80 and industry practice, the names of the BHEN and BLEN pins, as well as the D15-8 and D7-0 pins, have been swapped on the Z382 compared to the Z380. This fact should be significant only for those using a Z380 Emulator in a Z382-based project.
$\overline{\text{BUSREQ}}$	133	**Bus Request** (input, active Low): When this signal is asserted, an external bus master is requesting control of the bus. BREQ has higher priority than all nonmaskable and maskable interrupt requests.
BUSCLK	127	**Bus Clock** (output, active High, 3-state): This signal is the reference edge for the majority of other signals generated by the 380C. Its frequency may be that of the CLKI pin, or CLKI divided by two or times two.

Table 21. Multiprocessor Unit (MPU) Signals (Continued)

Pin Name	Pin Number(s)	Description
D15-0	24 - 31 33 - 40	**D15-0 Data Bus** (input/output, active High, 3-state): This bidirectional 16-bit data bus is used for data transfer between the 380C and memory or I/O devices. In a memory word transfer, the even-addressed (A0=0) byte is transferred on D7-0, and the odd-addressed (A0=1) byte on D15-8. 8-bit memories should be connected to D7-0, while 8-bit I/O devices should be attached to D15-8 (this difference tends to equalize electrical loading). (See note under BLEN pin description on page 38.)
HALT STNBY	121 120	**HALT, STANDBY Status** (outputs, active Low): These two outputs indicate the status of the Z382 as follows: STNBY / HALT / Mode H / H / Normal instruction execution H / L / HALT instruction L / H / SLEEP Mode: clock runs but is blocked from most of the chip L / L / STANDBY Mode: oscillator is stopped
INT3 INT2 INT1	139 138 137	**Interrupt Requests** (inputs, active Low): Asynchronous maskable interrupt inputs. Can be selected as low- or high-level sensitive, or as falling- or rising-edge triggered.
INT0	136	**Interrupt Request** (input, active Low): INT0 is logically ORed (positive-logic ANDed) with the interrupt requests from the on-chip MIMIC, DMAs, and HDLC controllers, to create the processor's INT0 input.
IOCLK	114	**Input/Output Clock** (output, active High, 3-state): This signal is a program controlled divided-down version of BUSCLK. The division factor can be two, four, six or eight with I/O transactions and interrupt-acknowledge transactions occurring relative to IOCLK. IOCLK can be disabled, in which case BUSCLK is the timing reference for I/O transactions. Note: The INTACK output of the Z380 has been omitted on the Z382 for pinning reasons. A similar signal can be easily obtained by low-active-ANDing (positive-logic ORing) the M1 and IORQ outputs.
IORQ	115	**Input/Output Request** (output, active Low, 3-state): This signal is active during all I/O read and write transactions and interrupt acknowledge transactions.
IORD	125	**Input/Output Read Strobe** (output, active Low, 3-state): This signal is used to strobe data from the peripherals during I/O read transactions.
IOWR	123	**Input/Output Write Strobe** (output, active Low, 3-state): This signal is used to strobe data into the peripherals during I/O write transactions.
IOCS1 IOCS2	45 46	**Input/Output Chip Select** (output, active Low): These outputs may be used to access external I/O devices. The base I/O address and range are programmable.

Table 21. Multiprocessor Unit (MPU) Signals (Continued)

Pin Name	Pin Number(s)	Description
$\overline{M1}$	116	**Machine Cycle One** (output, active Low, 3-state): This signal is active during instruction fetch and interrupt acknowledge transactions. The Z382 does not support RETI decoding by Z80 peripherals (PIO, SIO, and CTC). It does support Z80-type interrupt daisy-chaining by devices that include explicit clearing of IUS (for example, SCC).
$\overline{MRD}$	126	**Memory Read** (output, active Low, 3-state): This signal indicates that the addressed memory location places its data on the data bus. $\overline{MRD}$ is active from the end of T1 until the end of T4 during memory read transactions.
$\overline{MSIZE}$	117	**Memory Size** (input/open-drain output, active Low): In 16-bit memory operations, this signal indicates whether the addressed memory location is word size (logic High) or byte size (logic Low). In the latter case, the 8-bit memory is connected to the D7-0 lines, and an additional memory transaction on D7-0 automatically is generated to transfer the other byte of the word. (See the note on pin name swapping after the $\overline{BLEN}$ pin description on page 38) $\overline{MSIZE}$ is driven as an open-drain output by the memory decoding modules, when they are enabled in 8-bit mode and the address falls within their range.
$\overline{MWR}$	124	**Memory Write** (output, active Low, 3-state): This signal indicates that the addressed memory location stores the data on the databus, as qualified by $\overline{BHEN}$ and $\overline{BLEN}$. $\overline{MWR}$ is active from the end of T2 until the end of T4 during memory write transactions.
$\overline{NMI}$	135	**Nonmaskable Interrupt** (input, falling edge-triggered): This input has higher priority than the maskable interrupt inputs INT3-INT0.
$\overline{RESET}$	134	**Reset** (input, active Low): This input must be active for a minimum of five BUSCLK periods to initialize the Z382. The effect of $\overline{RESET}$ is described in detail in the Reset section.
$\overline{ROMCS}$	42	**ROM Chip Select** (output, active Low): After Reset, the Z382 drives this output and $\overline{MSIZE}$ Low for all memory accesses with A23=0. Software can program the chip select logic to assert $\overline{ROMCS}$ for a different range of memory addresses. If ROM is 16 bits wide and composed of two 8-bit devices, connect the Chip Select inputs of both devices to $\overline{ROMCS}$, and program the hardware not to force $\overline{MSIZE}$ Low in the first two instructions of the ROM code.

On the Host side, attribute memory is accessible only on even byte addresses. On the 380C side attribute memory can be accessed as bytes or words.

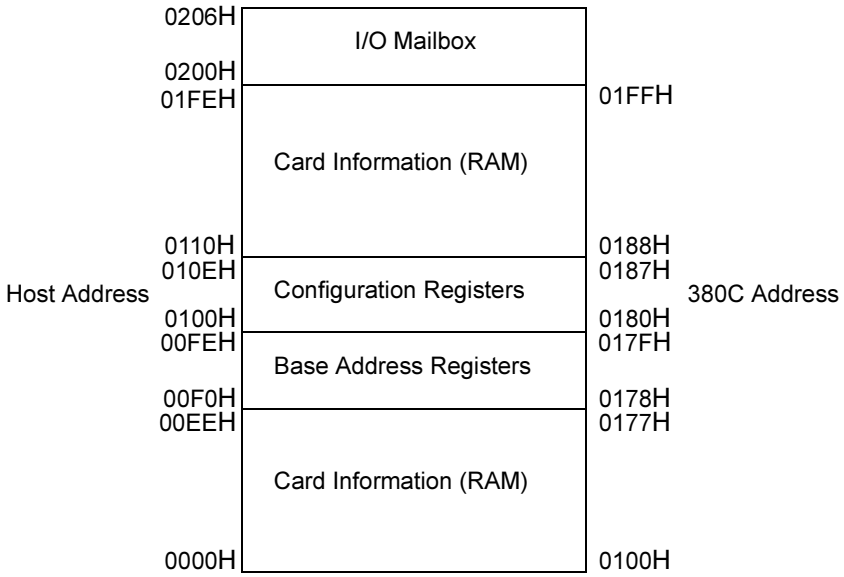

Figure 28. PCMCIA Attribute Memory Organization

Base Address Registers

These seven registers are written by the 380C with the base addresses of 8-byte windows in the host's I/O address space which the host can use to communicate with the host-accessible registers in the MIMIC.

Configuration Registers

There are five configuration registers of the PCMCIA 3.0 standard and in addition a version number register, two image base address registers, and the seven base address registers described in the previous paragraph. The Host accesses these registers to configure the interface and to retrieve status.

Configuration Option Register. This register is used on one side to configure the PCMCIA interface, controlling items such as type of interrupt, DMA enable, and selection of the Base Address Register. On the other side, a reset can be triggered by setting a certain bit.

Card Configuration and Status Register. This register contains information about the status of the interface, including whether certain signals have changed, interrupts, and power down.

Monitor Channel Operation

The monitor channels are full duplex and operate on a pseudo-asynchronous basis, in other words, data transfers take place synchronized to frame sync but the flow is controlled by a handshake procedure using the MX and MR bits. Figure 32 illustrates the handshake procedure (flow of events).

Idle. The MX and MR pair being held inactive (High) for two or more frames constitutes the channel being idle in that direction. The data received in the monitor channel is invalid and should be 11111111.

Start of Transmission. The first byte of data is placed on the bus and MX is activated (Low). MX remains active, and the data is repeated until an inactive-to-active transition of MR is received, indicating that the data has been captured by the receiver.

Subsequent Transmissions. The second and subsequent bytes are placed on the bus after the inactive to active transition of MR. At the time that the second byte is transmitted, MX is returned inactive for one frame time only; the data is valid in the same frame. In the following frame, MX returns active again and the same byte is transmitted. Data is repeated in subsequent frames and MX remains active until acknowledgment is detected (MR transition from inactive to active).

Maximum Speed Case. The transmitter is capable of minimizing the delay between bytes to achieve higher data throughput than is provided by the general case described previously. The first and second bytes are transmitted normally, However, starting with the third byte, the transmitter deactivates MX and transmits new data one frame time after MR is deactivated. In this way, the transmitter anticipates that MR is reactivated, which it accomplishes one frame time after it is deactivated, unless an abort is signalled by the receiver.

End of Message (EOM). The transmitter sends an EOM, normally after the last byte of data has been transmitted, by not reactivating MX after deactivating it in response to MR going inactive.

Reception. At the time the receiver detects the first byte, indicated by the inactive-to-active transition of MX, MR is inactive. In response to the activation of MX, the data is read off the bus and MR is activated. MR remains active until the next byte is received or an end of message is detected. Subsequent data is received from the bus on each falling edge of MX, and a monitor channel receive data available interrupt is generated. The data may be valid at the time that MX went inactive, one frame time prior to going active. MR is deactivated after the data is read and reactivated one frame time later. The transmitter detects MR going inactive and anticipates its reactivation one frame later. The reception of data is terminated by the reception of an end of message indication.

Abort. The abort is a signal from the receiver to the transmitter indicating that the data has been missed. It is not an abort in the classical sense, which is an indica-

Table 42. HDLC Registers (Continued)

Register Name	I/O Address	Access
HDLC1 Receive Interrupt Register	006DH	R/W
HDLC1 Counter Access Port	006EH	R/W
HDLC1 DMA Select Register	006FH	R/W
HDLC2 Transmit Mode Register	0070H	R/W
HDLC2 Transmit Interrupt Register	0071H	R/W
HDLC2 Transmit Control/Status Register	0072H	R/W
HDLC2 Transmit Fill Register	0073H	R/W
HDLC2 Receive Mode Register	0074H	R/W
HDLC2 Receive Interrupt Register	0075H	R/W
HDLC2 Counter Access Port	0076H	R/W
HDLC2 DMA Select Register	0077H	R/W

Table 43. GCI/SCIT Registers

Register Name	I/O Address	Access
GCI Control Register	00C0H	R/W
GCI Status Register 1	00C1H	RO
GCI Status Register 2	00C2H	R/W
GCI Interrupt Enable Register	00C3H	R/W
MON0 Transmit Data Register	00C4H	WO
MON0 Receive Data Register	00C4H	RO
MON1 Transmit Data Register	00C5H	WO
MON1 Receive Data Register	00C5H	RO
C/I0 Transmit Data Register	00C6H	WO
C/I0 Receive Data Register	00C6H	RO
C/I1 Transmit Data Register	00C7H	WO
C/I1 Receive Data Register	00C7H	RO

D

E

F

G

Q

R

U

V

W

Z