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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z380C
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	20MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	144-LQFP
Supplier Device Package	144-VQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8038220asg

Host-PCMCIA I/O Write Timing (See Figure 8)

Specifications apply over Standard Operating Conditions unless otherwise noted. C_L = 50 pF for outputs.

Table 9. Host-PCMCIA I/O Write Timing

		Z80382		Z8L382		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t55	Address Setup to $\overline{\text{PCIOWR}}$ Fall	50		50		ns
t56	$\overline{\text{PCREG}}$ Setup to $\overline{\text{PCIOWR}}$ Fall	5		5		ns
t57	$\overline{\text{PCCE1}}$ Setup to $\overline{\text{PCIOWR}}$ Fall	5		5		ns
t58	$\overline{\text{PCIOWR}}$ Low Width	125		125		ns
t59	Data Setup to $\overline{\text{PCIOWR}}$ Rise	35		35		ns
t60	Data Hold from $\overline{\text{PCIOWR}}$ High	20		20		ns
t61	$\overline{\text{PCCE1}}$ Hold from $\overline{\text{PCIOWR}}$ High	10		10		ns
t62	$\overline{\text{PCREG}}$ Hold from $\overline{\text{PCIOWR}}$ High	10		10		ns
t63	Address Hold from $\overline{\text{PCIOWR}}$ High	10		10		ns

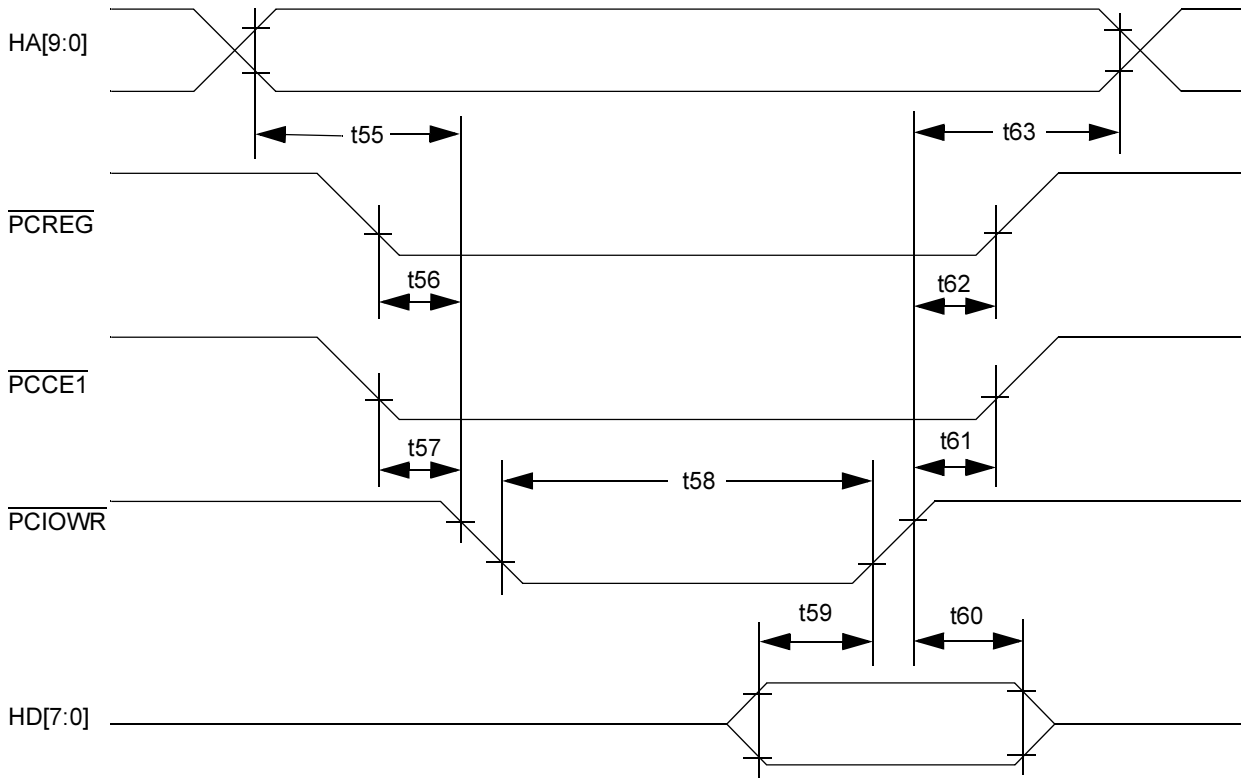

Figure 8. Host - PCMCIA I/O Write Timing Diagram

General-Purpose I/O Port Timing. (See Figure 16)

Specifications apply over Standard Operating Conditions unless otherwise noted. C_L = 50 pF for outputs.

Table 15. General-Purpose I/O Port Timing

		Z80382		Z8L382		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t100	I/O Port Data Setup to $\overline{\text{IORD}}$ Fall	10		10		ns
t101	I/O Port Data Hold from $\overline{\text{IORD}}$ High	5		5		ns
t102	I/O Port Data Valid from $\overline{\text{IOWR}}$ High		20		20	ns

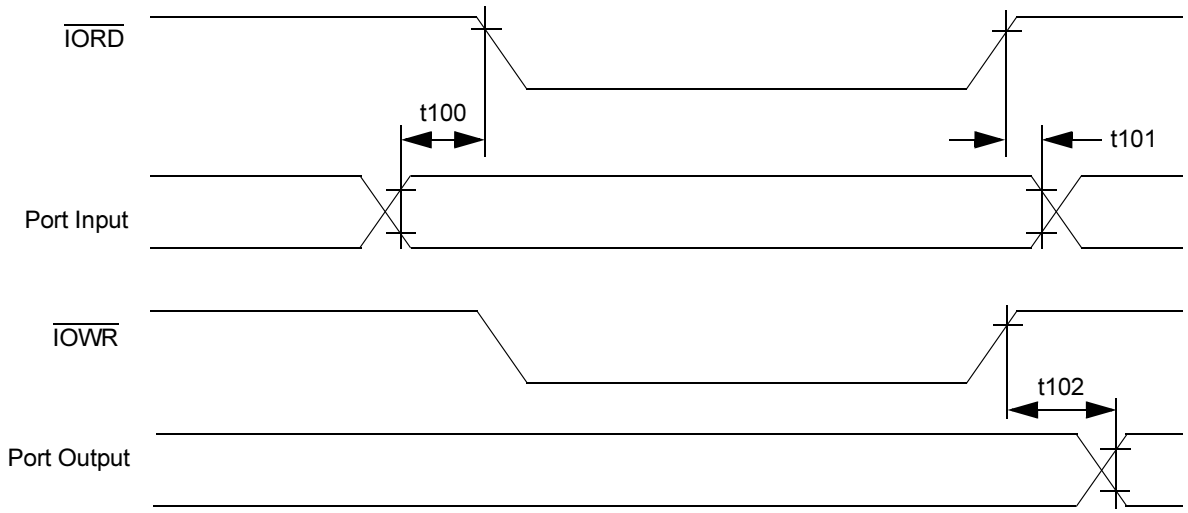

Figure 16. General-Purpose I/O Port Timing Diagram

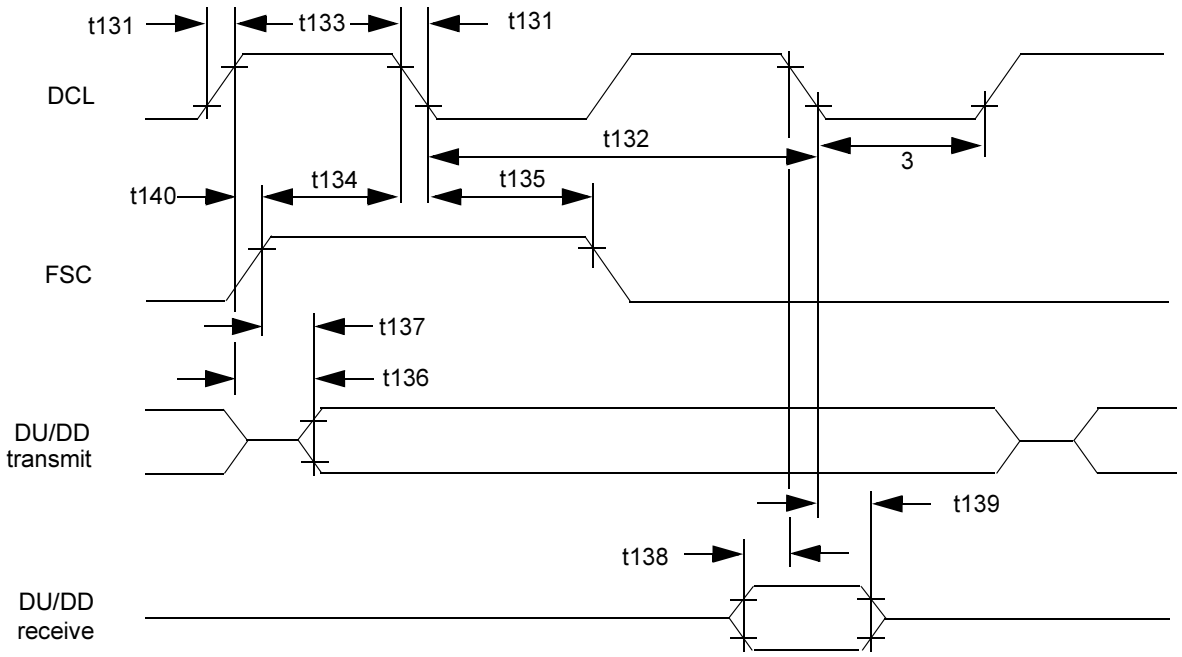

Figure 21. GCI/SCIT Slave and Master Timing Diagram

Pin Functions

Tables 21 through 11 describe the input and output signals of the Z382. Signals are normally asserted in the High state and negated in the Low state. An overline ( ) above the signal name indicates that the signal is asserted in the Low state and negated in the High state.

Many pins have multiple functions, and thus may appear more than once in the pin description tables. In each table, such pins are described using their function in that mode. Likewise, some signals may be output on alternate pins depending on the mode under which the Z382 is operating. The notation xx/yy in the Pin Number column indicates that the signal may be assigned to pin xx or pin yy.

Table 21. Multiprocessor Unit (MPU) Signals

Pin Name	Pin Number(s)	Description
A23 - 0	141 - 144, 1 - 4, 6 - 13, 15 - 22	**Address Bus** (outputs, active High, 3-state): These non-multiplexed address signals provide a linear memory address space of 16 MB. The address signals are also used to access I/O devices.
$\overline{\text{BUSACK}}$	132	**Bus Acknowledge** (output, active Low, 3-state): This signal, when asserted, indicates that the 380C has accepted an external bus request and has 3-stated its output drivers for the address bus, databus and the bus control signals TREFR, TREFA, TREFC, BHEN, BLEN, MRD, MWR, IORQ, IORD, and IOWR. The 380C cannot provide any DRAM refresh transactions while it is in the bus acknowledge state.
$\overline{\text{BHEN}}$	118	**Byte High Enable** (output, active Low, 3-state): This signal is asserted at the beginning of a memory or refresh transaction, to request an operation on D15-8. If software initiates a 16-bit memory operation, but MSIZE is asserted indicating a byte-wide memory, only the data on D7-0 is transferred in the current transaction, and another transaction is performed to transfer the other data byte, also on D7-0. See note in the next paragraph under BLEN pin description.
$\overline{\text{BLEN}}$	119	**Byte Low Enable** (output, active Low, 3-state): This signal is asserted at the beginning of a memory or refresh transaction, to request an operation on D7-0. If software initiates a 16-bit memory transaction, but MSIZE is asserted indicating a byte-wide memory, only the data on D7-0 is transferred in the current transaction, and another transaction is performed to transfer the other data byte, also on D7-0. Note: To align Z382 documentation and terminology with historical Z80 and industry practice, the names of the BHEN and BLEN pins, as well as the D15-8 and D7-0 pins, have been swapped on the Z382 compared to the Z380. This fact should be significant only for those using a Z380 Emulator in a Z382-based project.
$\overline{\text{BUSREQ}}$	133	**Bus Request** (input, active Low): When this signal is asserted, an external bus master is requesting control of the bus. BREQ has higher priority than all nonmaskable and maskable interrupt requests.
BUSCLK	127	**Bus Clock** (output, active High, 3-state): This signal is the reference edge for the majority of other signals generated by the 380C. Its frequency may be that of the CLKI pin, or CLKI divided by two or times two.

Table 21. Multiprocessor Unit (MPU) Signals (Continued)

Pin Name	Pin Number(s)	Description
$\overline{M1}$	116	**Machine Cycle One** (output, active Low, 3-state): This signal is active during instruction fetch and interrupt acknowledge transactions. The Z382 does not support RETI decoding by Z80 peripherals (PIO, SIO, and CTC). It does support Z80-type interrupt daisy-chaining by devices that include explicit clearing of IUS (for example, SCC).
$\overline{MRD}$	126	**Memory Read** (output, active Low, 3-state): This signal indicates that the addressed memory location places its data on the data bus. $\overline{MRD}$ is active from the end of T1 until the end of T4 during memory read transactions.
$\overline{MSIZE}$	117	**Memory Size** (input/open-drain output, active Low): In 16-bit memory operations, this signal indicates whether the addressed memory location is word size (logic High) or byte size (logic Low). In the latter case, the 8-bit memory is connected to the D7-0 lines, and an additional memory transaction on D7-0 automatically is generated to transfer the other byte of the word. (See the note on pin name swapping after the $\overline{BLEN}$ pin description on page 38) $\overline{MSIZE}$ is driven as an open-drain output by the memory decoding modules, when they are enabled in 8-bit mode and the address falls within their range.
$\overline{MWR}$	124	**Memory Write** (output, active Low, 3-state): This signal indicates that the addressed memory location stores the data on the databus, as qualified by $\overline{BHEN}$ and $\overline{BLEN}$. $\overline{MWR}$ is active from the end of T2 until the end of T4 during memory write transactions.
$\overline{NMI}$	135	**Nonmaskable Interrupt** (input, falling edge-triggered): This input has higher priority than the maskable interrupt inputs INT3-INT0.
$\overline{RESET}$	134	**Reset** (input, active Low): This input must be active for a minimum of five BUSCLK periods to initialize the Z382. The effect of $\overline{RESET}$ is described in detail in the Reset section.
$\overline{ROMCS}$	42	**ROM Chip Select** (output, active Low): After Reset, the Z382 drives this output and $\overline{MSIZE}$ Low for all memory accesses with A23=0. Software can program the chip select logic to assert $\overline{ROMCS}$ for a different range of memory addresses. If ROM is 16 bits wide and composed of two 8-bit devices, connect the Chip Select inputs of both devices to $\overline{ROMCS}$, and program the hardware not to force $\overline{MSIZE}$ Low in the first two instructions of the ROM code.

Table 23. ISA Bus Signals

Pin Name	Pin Number(s)	Description
HD7-0	78 - 85	**Host Data Bus** (Input/Output, 3-state): ISA or PCMCIA data bus.
$\overline{\text{HDOEN}}$	62	**Host Data Output Enable** (Output, active Low): This signal goes Low when the Host reads data from the MIMIC, the I/O Mailbox, or the Plug and Play interface, and during Host DMA read cycles.
HA11-0	64 - 67 69 - 76	**Host Address** (Input): Part of the ISA or PCMCIA address bus. The MS bits can be decoded by the built-in address decoder; bits 2-0 determine which MIMIC register the Host accesses. Bits 11-10 are decoded only by the Plug and Play ISA module.
HAEN	63	**Host Address Enable** (Input): HAEN must be Low to qualify COM Port decoding, I/O Mailbox decoding, and Plug and Play decoding. To support 16-bit decoding of Host I/O addresses, provide an external decoder for HA15-12 and HAEN all Low and connect its Low-active output to this pin.
$\overline{\text{HWR}}$	60	**Host Write** (Input, active Low): The Host drives this input Low to signal the MIMIC that a write operation is taking place.
$\overline{\text{HRD}}$	61	**Host Read** (Input, active Low): This input is used by the Host to signal the MIMIC interface that a read operation is taking place.
HINT1 HINT2	87 88	**Host Interrupt** (Outputs, active High): One of these outputs is driven High by the Plug and Play module when the MIMIC requests an interrupt from the Host. The unused signal is 3-stated.
$\overline{\text{HDAK0}}$ HDAK1	89 90	**Host DMA Acknowledge** (Inputs, active Low): These inputs indicate that the Host DMA controller has acknowledged the request and is transferring data.
HDRQ0 HDRQ1	91 92	**Host DMA Request** (Outputs, active High, 3-state): These outputs request a DMA transfer operation from the Host.

Table 26. PCMCIA Interface Signals

Pin Name	Pin Number(s)	Description
HA9-0	66 - 67 69 - 76	**PCMCIA Address Bus** (inputs): Provide Host PC addressing of attribute memory, configuration registers, and MIMIC. Decoded by the I/O address decoder.
HD7-0	78 - 85	**PCMCIA Data Bus** (input/outputs): Used for data transfers between the Host PC and the MIMIC, the attribute memory, and the configuration registers.
$\overline{\text{PCIORD}}$	61	**PCMCIA I/O Read** (input, active Low): Used to generate the $\overline{\text{INPACK}}$ signal when an I/O read cycle is within the configured range, and reads from the MIMIC.
$\overline{\text{PCIOWR}}$	60	**PCMCIA I/O Write** (input, active Low): This signal is used to write to the MIMIC.
$\overline{\text{PCWE}}$	89	**PCMCIA Write Enable** (input, active Low): Used to write to the attribute memory or to the configuration register which is addressed by means of HA9-1. Such an operation is recognized when $\overline{\text{PCWE}}$, $\overline{\text{PCCE1}}$, and $\overline{\text{PCREG}}$ are all Low, and either the interface is configured for I/O and memory operation, or $\overline{\text{PCIRQ}}$ is High, signifying ready, when configured as a memory only interface. The data applied while $\overline{\text{PCWE}}$ is Low are written to the attribute memory range on the positive edge of the $\overline{\text{PCWE}}$ or Card-enable ($\overline{\text{PCCE1}}$) signal.
$\overline{\text{PCOE}}$	90	**PCMCIA Output Enable** (input, active Low): $\overline{\text{PCOE}}$, $\overline{\text{PCCE1}}$, and $\overline{\text{PCREG}}$ all Low signify a read from attribute memory or a configuration register as selected by HA9-1.
$\overline{\text{PCCE1}}$	91	**PCMCIA Chip Enable 1** (input, active Low): $\overline{\text{PCCE1}}$ Low indicates a read or write access to: an even addressed byte in attribute memory, a configuration register, or the MIMIC.
$\overline{\text{PCREG}}$	63	**PCMCIA Register Select** (input, active Low): $\overline{\text{PCREG}}$ Low indicates a read or write access to the attribute memory range or to the I/O address range.
$\overline{\text{INPACK}}$	62	**PCMCIA Input Acknowledge** (Output, active Low): $\overline{\text{INPACK}}$ goes Low while an I/O read access is performed within the configured I/O address range. If the PCMCIA interface is configured such that it reacts independent of the address to all I/O read cycles, then $\overline{\text{INPACK}}$ is activated with $\overline{\text{PCIORD}}$.

Table 26. PCMCIA Interface Signals (Continued)

PCIRQ	87	**PCMCIA Interrupt Request** (Output, active Low): After the PCMCIA interface is reset it is in a MEMORY-ONLY mode, and this signal is driven Low to signify a Busy state until the 380C writes a register bit to indicate it is ready. After the card is then configured by the Host, PCIRQ goes Low to request a Host PC interrupt when the internal INT0 signal is asserted by the MIMIC. PCIRQ is monitored by the PCMCIA Host adapter and, dependent on the configuration, connected to one of the Host interrupts (for example, COM1 or COM2 interrupt). PCIRQ can be programmed to be a pulsed interrupt with a minimal pulse length of one microsecond, or a level-interrupt that is reset when the interrupt is processed by the Host. This choice is made by means of bit 6 of the Configuration Option Register.
PCRESET	92	**PCMCIA Reset** (input, active High): Setting PCRESET High resets the PCMCIA interface. The card configuration register is cleared and the PCMCIA interface operates in the MEMORY-ONLY mode until it is configured again. The attribute memory has to be initialized by the controller, and the Ready/Busy (PCIRQ) signal has to be deactivated.
STSCHG	88	**PCMCIA Status Change** (output): This output is controlled by a bit in the PCMCIA module's 380C Control Register.

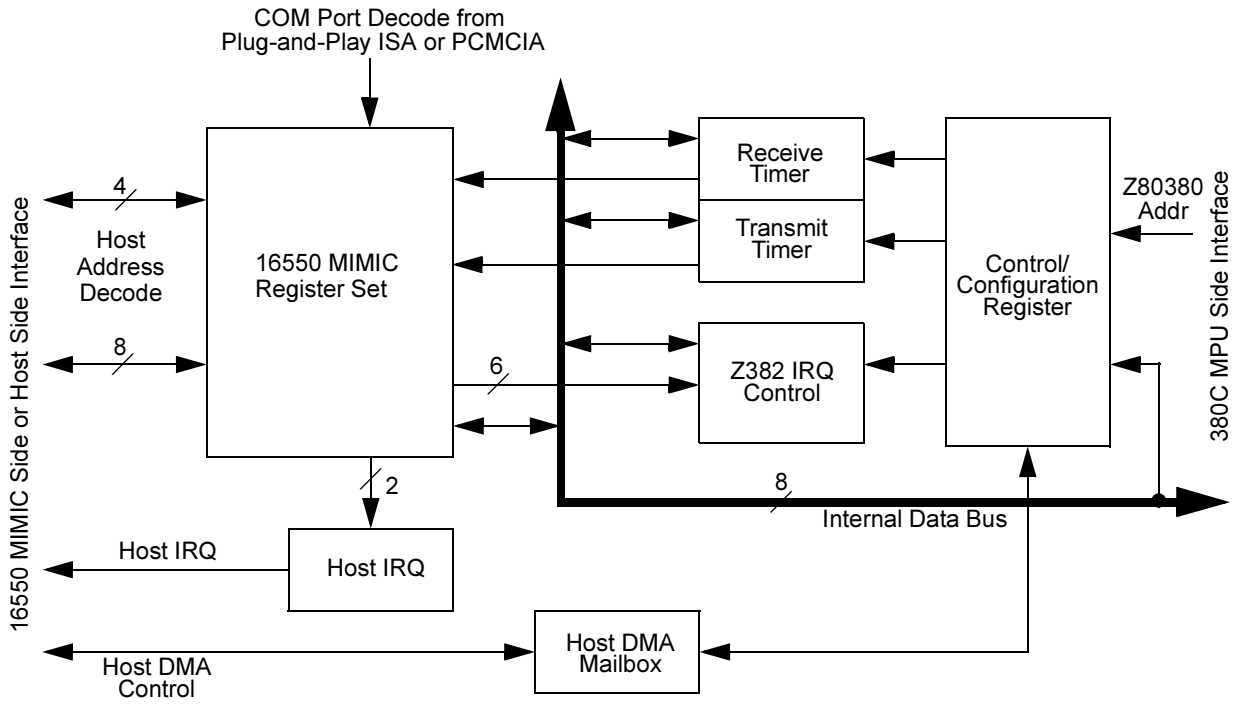

Figure 23. 16550 MIMIC Block Diagram

MIMIC Receiver FIFO

The receiver FIFO is 16-words deep and stores eight data bits and three error bits (Parity error, Framing error and Break detect) for each character received. The data and error bits move together in the FIFO. The error bits become available to the Host side of the interface when that particular location becomes the next address to read (top of FIFO). At that time these bits may either be read by the Host or they may cause an interrupt to the Host interface if so enabled. The error bits are set by the error status of the byte at the top of the FIFO but may only be cleared by reading the Line Status Register (LSR). If successive reads of the receiver FIFO are performed without reading the LSR, the status bits are set if any of the bytes read have the respective error bit set.

The Host interface may be interrupted when 1, 4, 8 or 14 bytes are available in the receiver FIFO. If the FIFO is not empty, but below the programmed trigger value, a timeout interrupt is available if the receiver FIFO is not written by the 380C or read by the Host by an interval determined by the Character Timeout Timer. This timer is an additional timer with 380C access-only which is used to emulate the 16550 four-character timeout delay. The timer receives the BRG as its input clock. Software determines the correct values to program into the Receiver Timeout Register

Table 28. MIMIC Programming Registers (Continued)

Interrupt Vector Register	00FCH
FIFO Status and Control Register	00ECH
Rx Timeout Time Constant Register	00EAH
Tx Timeout Time Constant Register	00EBH
Transmitter Time Constant Register	00FAH
Receiver Time Constant Register	00FBH

MIMIC-Host Interface Registers

In addition to the MIMIC programming registers, the Z382 contains a register set for interfacing with the Host by means of the MIMIC. These registers are used to emulate the 16550 UART so that the Host can access these registers in a manner similar to interfacing with the UART. This feature provides software compatibility with existing Host communication software. The registers are:

Configuration Registers

The following Configuration registers are implemented in the Z382 to provide for the resources required by the host to interface to the host-accessible functions within the chip:

- I/O Mailbox I/O Address
- MIMIC I/O Address
- Interrupt Request Level– This register can be selected to be output on either of the two available interrupt output lines. A unique Z382 feature allows these two pins to be configured to be any two of the ISA-bus interrupt lines.
- DMA Channel 0, DMA Channel 1– A unique Z382 feature allows the two DMA pin pairs to be configured to be any two of the seven ISA-bus DMA channels.

Host writes to the Configuration registers are effective immediately, in hardware, so there is no urgent need for the 380C processor to translate them into other register values. But the 380C processor can use the interrupt that occurs when the Host terminates Configuration state to examine what the Host has done to the Configuration registers, and operate accordingly in the future.

PCMCIA Interface

The PCMCIA Interface block integrates all the functions necessary for the operation of I/O interface cards in a PCMCIA 2.0 and 3.0 socket. These functions are:

- PCMCIA Interface Control
- Attribute Memory
- Configuration Registers
- I/O Interface
- Configurable Address Decoder
- Configurable Interrupt Logic
- Z380 Interface

Figure 27 illustrates the PCMCIA Interface block diagram

1. It puts the address of the Type/Status byte (from the LAR) on the address bus, and writes the code for Completed Buffer (no Status) into that byte.
2. If the DMA channel's Buffer IE field indicates `Interrupt for all buffers`, or `Interrupt for` Notify buffers and this was a Notify buffer, it sets its IP bit to request an interrupt.
3. It increments the LAR to the address following this list entry, and goes back to fetch a new list entry from that address, as described above.

Terminate

The HDLC receiver asserts this signal for an End of Frame, Abort, or Overrun condition. The HDLC Transmitter does so for an Underrun condition. After the DMA channel transfers a byte, if the device signals Data Request and Terminate, or if the device signals Terminate without Data Request, the DMA channel proceeds as follows:

Note: If the device encounters an error from which an operation can not continue without processor attention, after signalling, the device must refrain from asserting Data Request until software has done so. The HDLC Transmitter performs this function for Underrun.

1. The device places the address of the Length field on the address bus, and writes the current (16-bit) value in its BLR to memory at that address and the next higher address. This value enables software to determine how much data was actually written into, or read out of, this buffer.
2. The device places the address of the Type/Status byte on the address bus, sets the control signals for a memory write, signals Completed Buffer (with Status), and asserts the Store Status signal to the device.
3. The device, in response to Store Status, can place up to 6 bits of status on D5-0. For the HDLC receiver, this status includes Overrun, End of Frame, Abort, CRC Error, and the residual bit count. For the HDLC Transmitter, only Underrun will prompt a Terminate indication, so the specific status bits are unimportant.
4. After the Type/Status byte has been written, the DMA channel advances the LAR over this list entry, in other words, to the address of the next entry.
5. If the DMA channel's Buffer IE field indicates anything other than No Buffer Interrupts, it requests an interrupt.
6. The DMA channel then fetches another list entry from the address in the LAR, as described above.

Centralized DMA Registers

Two registers listed below provide overall DMA subsystem control and status:

DMA Control Register	(DMACR)
DMA Vector Register	(DMAVR)

DMA Control Register (DMACR)

This register controls when bus control is returned to the 380C processor after a DMA channel has operated. It also provides modes whereby the Buffer Address and Buffer Length per-channel registers can be read and written.

DMA Vector Register (DMAVR)

This register contains the base interrupt vector for the DMA channels. It also identifies, during an interrupt acknowledge cycle, the interrupting DMA Channel.

Serial Communication Channels

The Z382 provides several means of serial data communications. These are the Asynchronous Serial Communication Interface (ASCI), the HDLC controllers, the GCI/SCIT interface and the Clocked Serial I/O Channel.

Asynchronous Serial Communications Interface (ASCI)

The Z382 provides two independently programmable ASCIs, each including a flexible baud rate generator. Key ASCI features include:

- Full-duplex operation
- Programmable data format
  - 7- or 8- data bits with optional ninth bit for multiprocessor communication
  - One or two stop bits
  - Odd, even or no parity
- Programmable baud rate generator
  - Divide-by-one, divide-by-16 and divide-by-64 modes
  - Up to three modem control signals per channel, depending on operating mode of the Z382
- Programmable interrupt conditions
- Four level data/status FIFOs for the receivers

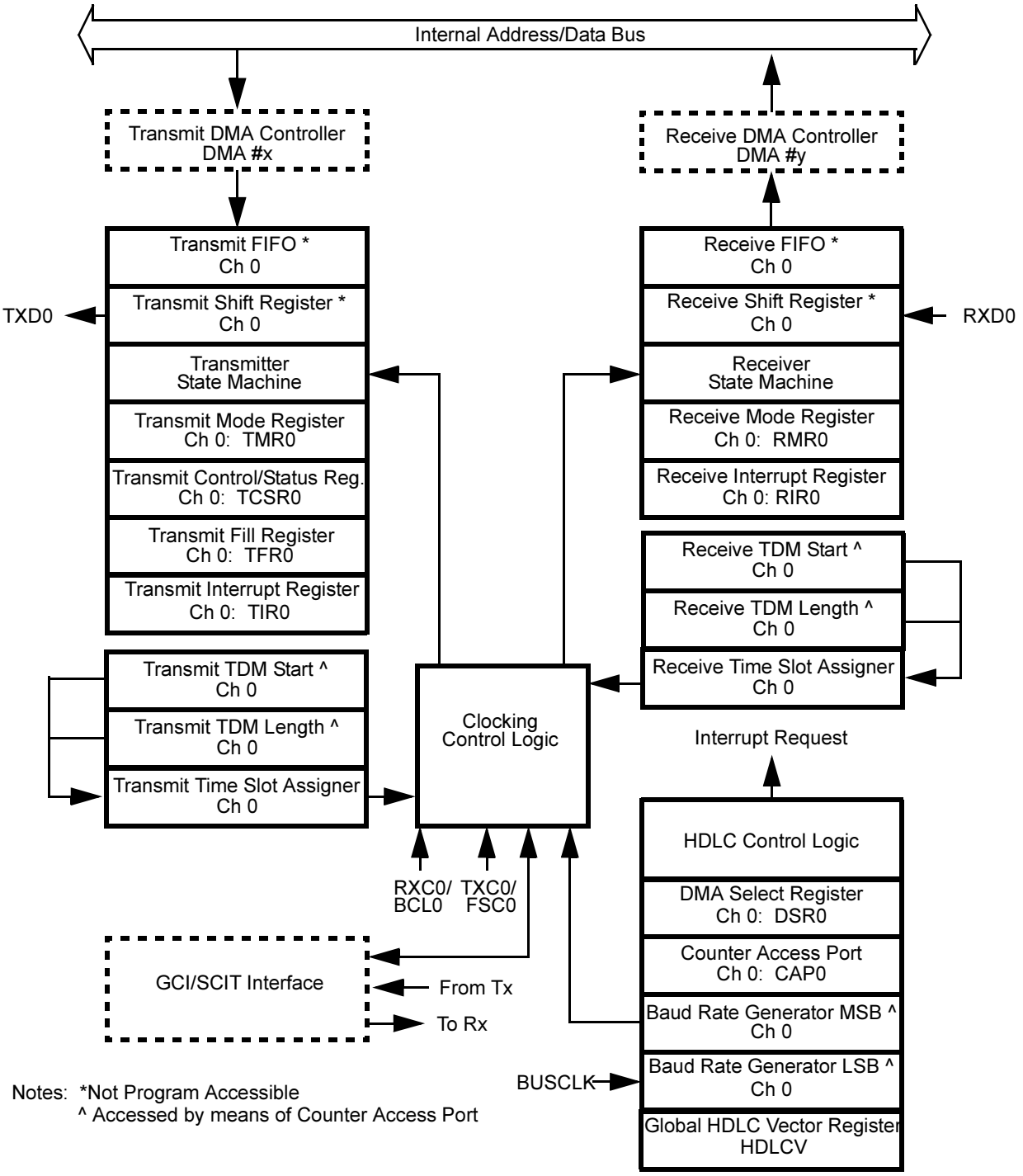

Figure 31. HDLC Channel Block Diagram (One of Three Channels Illustrated)

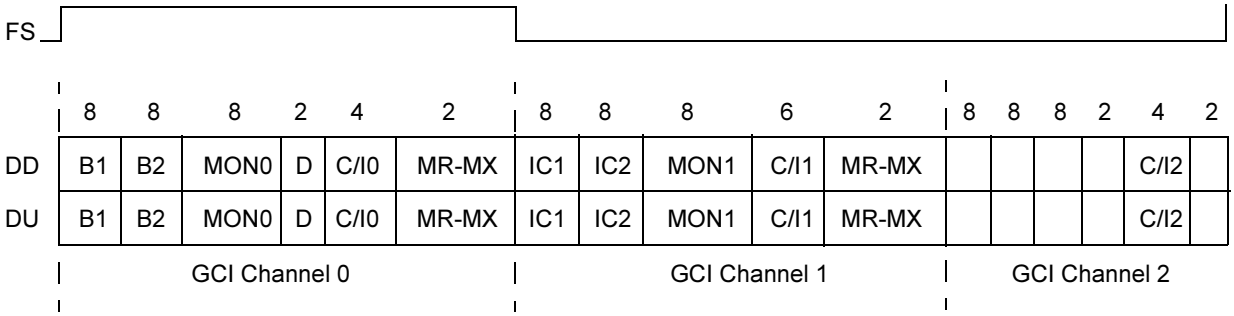

Figure 32. GCI/SCIT Frame Structure

B Channels. B1 and B2 are the first two 8-bit time slots after the frame sync pulse. Each B channel provides 64 Kbps of user data to/from the network.

Monitor Channels. There are two channels, monitor 0 and monitor 1. Each channel consists of eight bits of data and two associated handshake bits, MR and MX, that control data flow.

D Channel. The 16 Kbps D channel (2 bits per frame) provides a connection between the layer two and layer one components.

Command/Indicate Channels. Three command/indicate channels, C/I0, C/I1 and C/I2 are provided. Each sub-frame has one. (C/I2 is the same as TIC, as indicated below.) These channels provide real-time status between devices connected by means of the GCI/SCIT bus.

Intercommunication Channels. Two intercommunication subchannels are provided in GCI channel 1. These subchannels provide 64 Kbps data paths between user devices.

TIC Bus. The TIC bus is the same as C/I2 and is used for D channel access with some GCI/SCIT devices. It allows multiple layer-2 devices to individually gain access to the D and C/I channels located in the first sub-frame.

The data signals on the GCI/SCIT bus are called Data Upstream (DU) and Data Downstream (DD). Each of these is a bus that can be sensed as well as driven in an open-drain (open-collector) fashion by the Z382 and other devices. GCI practice defines certain fields on each line to flow in certain directions.

The Z382 always receives from DD and (when enabled) drives DU in the B2, MON0, D, C/I0, and MX0 fields. The Z382 always receives from DU and (when enabled) drives DD in the MR0 bit. Which line is driven and which is received is selected by software for the IC1, IC2, MON1, and C/I1 fields and the MX1 and MR1 bits, with MR1 always being in the opposite direction from MON1 and MX1.

Monitor Channel Operation

The monitor channels are full duplex and operate on a pseudo-asynchronous basis, in other words, data transfers take place synchronized to frame sync but the flow is controlled by a handshake procedure using the MX and MR bits. Figure 32 illustrates the handshake procedure (flow of events).

Idle. The MX and MR pair being held inactive (High) for two or more frames constitutes the channel being idle in that direction. The data received in the monitor channel is invalid and should be 11111111.

Start of Transmission. The first byte of data is placed on the bus and MX is activated (Low). MX remains active, and the data is repeated until an inactive-to-active transition of MR is received, indicating that the data has been captured by the receiver.

Subsequent Transmissions. The second and subsequent bytes are placed on the bus after the inactive to active transition of MR. At the time that the second byte is transmitted, MX is returned inactive for one frame time only; the data is valid in the same frame. In the following frame, MX returns active again and the same byte is transmitted. Data is repeated in subsequent frames and MX remains active until acknowledgment is detected (MR transition from inactive to active).

Maximum Speed Case. The transmitter is capable of minimizing the delay between bytes to achieve higher data throughput than is provided by the general case described previously. The first and second bytes are transmitted normally, However, starting with the third byte, the transmitter deactivates MX and transmits new data one frame time after MR is deactivated. In this way, the transmitter anticipates that MR is reactivated, which it accomplishes one frame time after it is deactivated, unless an abort is signalled by the receiver.

End of Message (EOM). The transmitter sends an EOM, normally after the last byte of data has been transmitted, by not reactivating MX after deactivating it in response to MR going inactive.

Reception. At the time the receiver detects the first byte, indicated by the inactive-to-active transition of MX, MR is inactive. In response to the activation of MX, the data is read off the bus and MR is activated. MR remains active until the next byte is received or an end of message is detected. Subsequent data is received from the bus on each falling edge of MX, and a monitor channel receive data available interrupt is generated. The data may be valid at the time that MX went inactive, one frame time prior to going active. MR is deactivated after the data is read and reactivated one frame time later. The transmitter detects MR going inactive and anticipates its reactivation one frame later. The reception of data is terminated by the reception of an end of message indication.

Abort. The abort is a signal from the receiver to the transmitter indicating that the data has been missed. It is not an abort in the classical sense, which is an indica-

- I/OCS1 High and Low Address Registers
- I/OCS2 High and Low Address Registers

I/O Chip Select 1/2 High and Low Address Registers. Specify the base address and the I/O block size for I/O Chip Selects 1 and 2.

RAM and ROM Chip Selects

Three memory chip select outputs are provided: $\overline{\text{ROMCS}}$, $\overline{\text{RAMCSL}}$, and $\overline{\text{RAMCSH}}$. These outputs support both 8- and 16-bit memories, and are asserted for a selected address range (4 KB to 8 MB) during both memory and I/O cycles. Unlike Chip Select and $\overline{\text{MSIZE}}$ signalling, Wait State generation can be specified which occurs only during memory cycles.

For the selected ROM and/or RAM range, the $\overline{\text{MSIZE}}$ pin can be programmed to be forced Low in an open-drain fashion when the address is in the programmed range, forcing 8-bit accesses in one or both ranges. When $\overline{\text{MSIZE}}$ is forced for 8-bit RAM in this way, $\overline{\text{RAMCSL}}$ is asserted for all cycles in the selected address range, and the $\overline{\text{RAMCSH}}$ pin assumes its alternate use as port pin PC7. When $\overline{\text{MSIZE}}$ is not forced for 8-bit RAM, $\overline{\text{RAMCSL}}$ is qualified by $\overline{\text{BLEN}}$, and $\overline{\text{RAMCSH}}$ acts as a chip select output pin and is qualified by $\overline{\text{BHEN}}$.

RAM and ROM Chip Select Registers

The following I/O-mapped registers are associated with the RAM and ROM chip selects and can be read and written by the 380C processor:

- RAM Address High and Low Registers
- ROM Address High and Low Registers
- Memory Mode Register 1
- Memory Mode Register 2

RAM Address High and Low Registers. These registers specify which bits of the address bus are used in the address comparison and thus, the memory block size. The block size can range from 4 KB to 8 MB.

ROM Address High and Low Registers. These registers specify which bits of the address bus are used in the address comparison and thus, the memory block size. The block size can range from 4 KB to 8 MB.

Memory Mode Register 1. This register enables the ROM chip select, specifies the number of wait states for the ROM chip select, and specifies the number of T1 Wait states for the RAM chip select.

Memory Mode Register 2. This register enables the RAM chip select, specifies 8- or 16-bit memory accesses for the RAM and ROM chip selects independently, and specifies the number of T2 and T3 Wait states for the RAM chip select.

Table 46. Plug-and-Play ISA Registers (Continued)

Register Name	I/O Address	Access	Host
Wake Register	None		PnP 03H, WO
PnP Master Register	0102H	R/W	None
Resource Data Register	0104H	WO	PnP 04H, RO
PnP Status Register	0105H	RO	PnP 05H, RO
Card Select Number (CSN) Register	0106H	RO	PnP 06H, R/W
Logical Device Number Register	None		PnP 07H, RO
Activate Register	0130H	R/W	PnP 30H, R/W
I/O Range Check Register	None		PnP 31H, R/W
I/O Mailbox Base Address Registers	0160,1H	R/W	PnP 60,1H, R/W
MIMIC Base Address Registers	0162,3H	R/W	PnP 62,3H, R/W
Interrupt Request Level Register	0170H	R/W	PnP 70H, R/W
DMA Channel 0,1 Registers	0174,5H	R/W	PnP 74,5H, R/W