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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z380C
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	20MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	144-QFP
Supplier Device Package	144-QFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8038220fsc

- Up to 32 General-Purpose I/O Pins
- DC to 20 MHz Operating Frequency @ 5.0V
- DC to 10 MHz Operating Frequency @ 3.3V
- 144-Pin QFP and VQFP Style Packages

General Description

The Z80382 (Z382) is designed to address high-end data communication applications such as digital modems (ISDN, GSM, Mobitex & Modacom), xDSL and analog modems (V.34 and beyond). The Z382 provides a performance upgrade to existing Z80- and Z18x-based designs by utilizing the increased bandwidth of the 380C processor. The Z8L382 is a low voltage version of the device.

Notes: In this document the notation 380C denotes the Z380-compatible CPU core which is embedded in the Z382.

An overline ($\overline{\ }$) above a signal name indicates that the signal is asserted in the Low state and negated in the High state.

The 380C microprocessor is a high-performance processor with fast and efficient throughput and increased memory addressing capabilities. The 380C offers a continuing growth path for present Z80- or Z18x-based designs, while maintaining Z80 and Z180 object code compatibility. Its enhancements include added instructions, expanded 16 MB address space and flexible bus interface timing.

In the 380C, the basic addressing modes of the Z80 microprocessor have been augmented to include Stack Pointer Relative loads and stores, 16-bit and 24-bit indexed offsets, and more flexible Indirect Register addressing. Internally, all of the addressing modes allow up to 32-bit linear addressing; however, the Z382 has 24 address pins, therefore it can address a maximum of 16 MB of memory.

Other additions to the instruction set include a full complement of 16-bit arithmetic and logical operations, 16-bit I/O operations, multiply and divide, and a complete set of register-to-register loads and exchanges.

The 380C register file includes alternate versions of the IX and IY registers. There are four banks of registers in the 380C, along with instructions for switching among them. All of the 16-bit register pairs and index registers in the basic Z80 microprocessor register file are expanded to 32 bits.

The Z382 includes dynamic bus sizing to allow any mix of 8- and 16-bit memory, and I/O devices in a system. One application for this capability would be to copy code from a low-cost, slow 8-bit ROM to 16-bit RAM, from which it can be exe-

cuted at much higher speeds. Memory bus sizes can be configured internally by software to eliminate the need for external logic to drive MSIZE.

Some features that have traditionally been handled by external peripherals have been incorporated in the Z382. These on-chip peripherals reduce system chip count and interconnections on the external bus. These peripherals, illustrated in the Z382 Block Diagram in Figure 1, are summarized below.

HDLC Synchronous Channels. Three HDLC channels operate at serial data rates of up to 10 Mbps and feature 8-byte receive and transmit FIFOs. These can be used for modems, general data communications, and ISDN. The ISDN can be handled separately or through the GCI/SCIT bus interface. HDLC Channels always transfer data through the DMA channels. A transparent mode is selectable. Two of the HDLC cells can be pin multiplexed with the ASCIs (UARTs) to provide dynamically switchable (async-sync) DTE interfaces.

DMA Channels. The eight DMA channels provide 24-bit memory addressing and can transfer memory block sizes of up to 64 KB (16-bits) word. These DMA channels can be dynamically assigned to serve the HDLC ports, MIMIC COM port, Host DMA Mailbox, or ASCIs in any mixture. Linked list operation allows all HDLC transmitters and receivers to operate at or above T1/E1 rates simultaneously without loading the bus bandwidth.

16550 MIMIC. Provides connection to a PC ISA bus and emulation of the 16550 UART register set. Improvements include 16 mA output drivers and internal COM port address decoding to reduce external PC interface components.

ASCI. Two flexible asynchronous serial channels with baud rate generators, modem control and status.

CSIO. A clocked serial I/O channel which can be used for serial memory interface.

Timers. Two 16-bit counter/timers with flexible prescalers for wide-range timing applications.

GCI/SCIT Bus Interface. A common interface to ISDN interface devices. Internal signals from this module can be connected to the HDLC channels to provide two B-channels and one D-channel for ISDN.

Plug-and-Play ISA Interface. Provides auto-configuration in ISA (AT bus) applications.

PCMCIA Interface. Provides connectivity to a PCMCIA bus.

32-Bit General-Purpose I/O. For non-PC add-in applications, four 8-bit ports are provided for general- purpose I/O. In ISA or PCMCIA applications, the pins from two of the ports are reallocated to host bus signals and are not available. Pins from the other two ports are selectively multiplexed with on-chip peripheral functions (ASCIs, CSIO, PRT). These pins are individually programmable for input/output mode.

Table 3. Input Class Characteristics

Input Class[1]	V_{IL} Max. (Z80382)	V_{IL} Max. (Z8L382)	V_{IH} Min. (Z80382)	V_{IH} Min. (Z8L382)	Minimum Hysteresis
I	0.8V	0.6V	2.0V	2.0V	0.4V
	I_I = ±10 µA max, V_I = 0 to 5V (includes leakage if I/O) C_{IN} = 5 pF max (if input only, see output type if I/O)				
	Note: Inputs of this type include a weak-latch circuit, except that a register bit can disable those for pins PB7-0.				
R	0.4V	0.4V	V_{DD} - 0.6V	V_{DD} - 0.3V	0.4V
	I_I = ±10 µA max, V_I = 0 to 5V C_{IN} = 5 pF max				
	Note: Inputs of this type except CLKI include a weak-latch circuit.				

Note: The Pin Numbers and Input/Output Classifications described in Table 1 identifies the specific input pins in each class.

Host-PCMCIA Attribute Memory Read Timing (See Figure 5)

Specifications apply over Standard Operating Conditions unless otherwise noted. C_L = 50 pF for outputs.

Table 6. Host-PCMCIA Attribute Memory Read Timing

		Z80382		Z8L382		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
t22	Address Setup to $\overline{\text{PCCE1}}$ Fall	15		20		ns
t23	Address Setup to $\overline{\text{PCOE}}$ Fall	15		20		ns
t24	Address Hold from $\overline{\text{PCCE1}}$ High	5		5		ns
t25	Address Hold from $\overline{\text{PCOE}}$ High	5		5		ns
t26	$\overline{\text{PCCE1}}$ Low to Data Active	0		0		ns
t27	$\overline{\text{PCOE}}$ Low to Data Active	0		0		ns
t28	$\overline{\text{PCCE1}}$ Low to Data Valid		60		60	ns
t29	$\overline{\text{PCOE}}$ Low to Data Valid		60		60	ns
t30	Data Invalid from $\overline{\text{PCCE1}}$ High	5		5		ns
t31	Data Invalid from $\overline{\text{PCOE}}$ High	5		5		ns
t32	Data 3-state from $\overline{\text{PCCE1}}$ High		20		20	ns
t33	Data 3-state from $\overline{\text{PCOE}}$ High		20		20	ns
Note: Timings also apply for reads from registers located in the attribute memory space.						

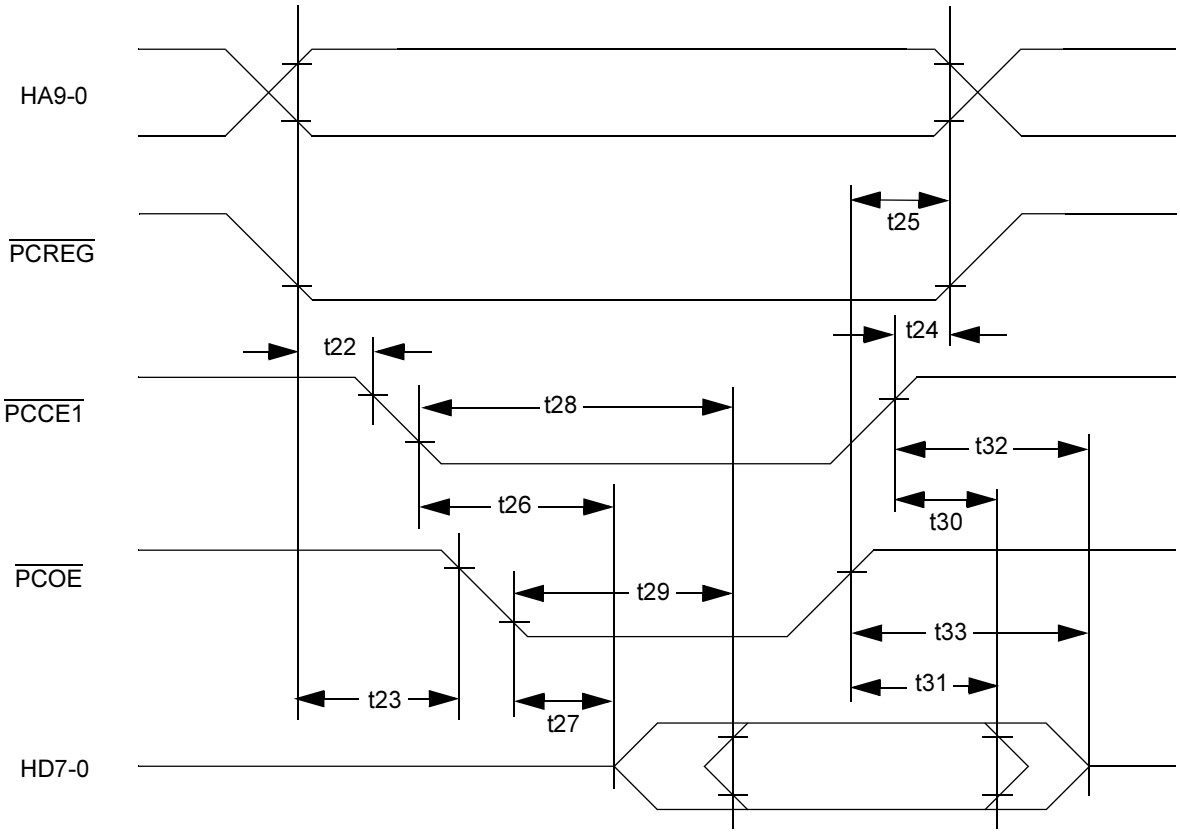

Figure 5. Host - PCMCIA Attribute Memory Read Timing Diagram

CSIO Receive/Transmit Timing (See Figure 10)

Specifications apply over Standard Operating Conditions unless otherwise noted. C_L = 50 pF for outputs.

Table 11. CSIO Receive/Transmit Timing

		Z80382		Z8L382		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t66	CKS Low to TXS Valid		40		40	ns
t67	RXS Setup to CKS Rise	20		20		ns
t68	RXS Hold from CKS High	5		5		ns
t71	CKS External Clock Period	50		50		ns

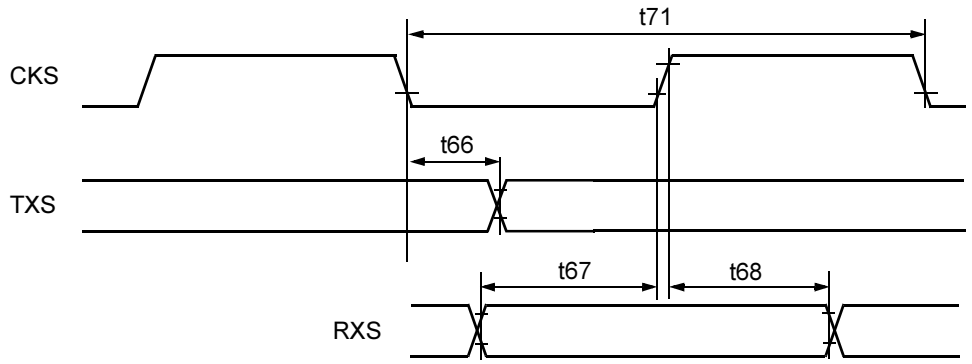

Figure 10. CSIO Receive/Transmit Timing Diagram

ASCI Transmitter Timing (See Figure 11)

Specifications apply over Standard Operating Conditions unless otherwise noted. C_L = 50 pF for outputs.

Table 12. ASCI Transmitter Timing

		Z80382		Z8L382		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t72	External Transmit Clock Period	50		50		ns
t73	External Transmit Clock Low Width	30		30		ns
t74	External Transmit Clock High Width	30		30		ns
t75	External Transmit Clock Fall Time		5		10	ns
t76	External Transmit Clock Rise Time		5		10	ns
t77	CKA Low to TXA Data Valid		20		30	ns

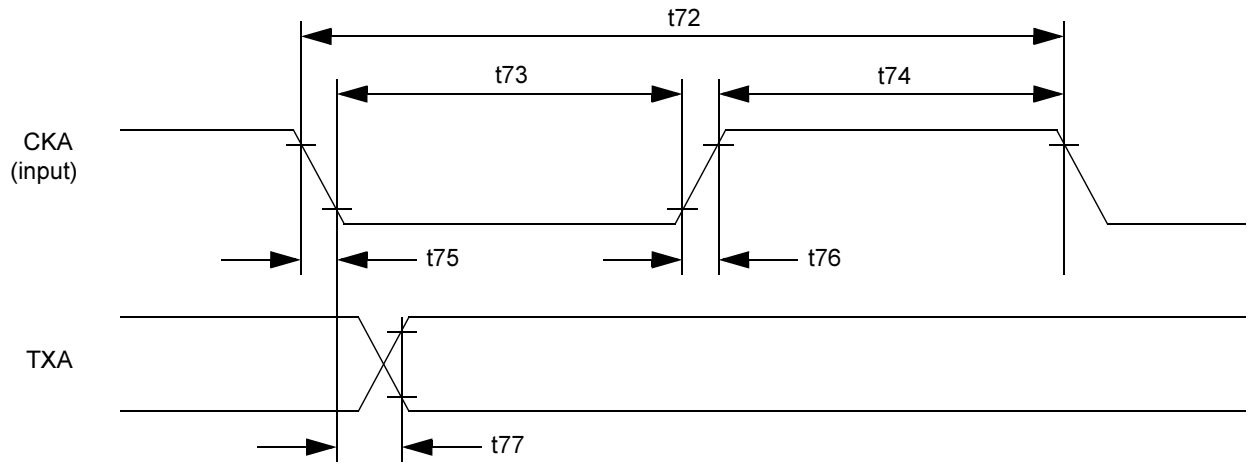

Figure 11. ASCI Transmitter Timing Diagram

HDLC Transmit Timing- Full Time HDLC Mode (See Figure 19)

Table 17. HDLC Transmit Timing

		Z80382		Z8L382		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t113	External Transmit Clock Period[1]	50		50		ns
t114	External Transmit Clock High Time	15		15		ns
t115	External Transmit Clock Low Time	15		15		ns
t116	External Transmit Clock Fall Time		5		10	ns
t117	External Transmit Clock Rise Time		5		10	ns
t118	TxC Low to TxD Data Valid		20		25	ns

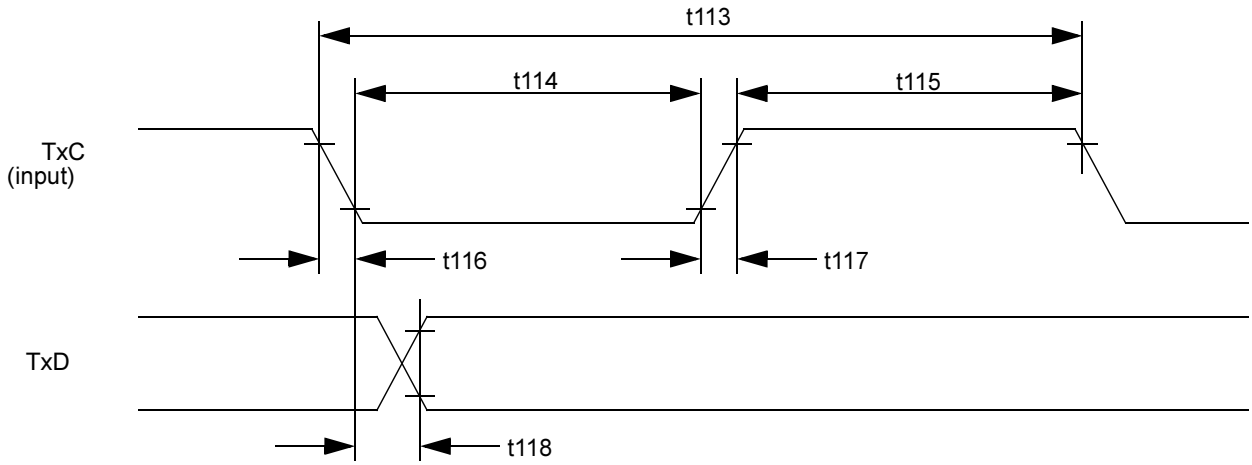

Figure 19. HDLC Transmit Timing Diagram (Full Time HDLC)

HDLC Timing - Non-GCI TDM mode (See Figure 20)

Specifications apply over Standard Operating Conditions unless otherwise noted.
C_L = 50 pF for outputs

Table 18. HDLC Timing - Non-GCI TDM Mode

		Z80382		Z8L382		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t120	FSC Setup to BCL Fall	30		50		ns
t121	FSC Hold from BCL Low	20		30		ns
t122	BCL Period	50		50		ns
t123	BCL High Time	15		15		ns
t124	BCL Low Time	15		15		ns
t125	BCL High to $\overline{\text{TxEN}}$ Low		15		20	ns
t126	BCL High to $\overline{\text{TxEN}}$ High		15		20	ns
t127	BCL High to TxD Valid		15		20	ns
t128	BCL High to TxD Invalid	15		20		ns
t129	RxD Setup to BCL Fall (Rise)[1]	15		20		ns
t130	RxD Hold from BCL Low (High)[1]	5		5		ns

Note: 1. Receive clock sampling edge is configurable by means of RIRn[6]. See Z80382 User Manual.

Table 22. UART, Timer and CSIO Signals

Pin Name	Pin Number(s)	Description
CKA0 CKA1	53/92/96 49/65/100	**Asynchronous Clock 0, 1** (Bidirectional): Clock signals to or from the asynchronous channels (ASCIs).
$\overline{\text{CTS0}}$ $\overline{\text{CTS1}}$	61/111 60/110	**Clear to Send 0, 1** (Inputs, active Low): Transmit control signals for the ASCI channels.
$\overline{\text{DCD0}}$ $\overline{\text{DCD1}}$	89/112 66	**Data Carrier Detect 0, 1** (Inputs, active Low): Receive control signals for the ASCI channels. $\overline{\text{DCD1}}$ is not available in ISA applications.
$\overline{\text{RTS0}}$ $\overline{\text{RTS1}}$	88/93 94	**Request to Send 0, 1** (Outputs, active Low, 3-state): Software-controlled output from the ASCI channels.
RXA0 RXA1	52/90/99 55/67/103	**Receive Data 0, 1** (Inputs): ASCI Receive data.
TXA0 TXA1	51/91/98 54/87/102	**Transmit Data 0, 1** (Outputs): ASCI Transmit data.
CKS	58/64	**Serial Clock** (Bidirectional): The clock for the CSIO channel.
RXS	57/63	**Clocked Serial Receive Data** (Input): Receive data for the CSIO channel.
TXS	56/62	**Clocked Serial Transmit Data** (Output): Transmit data from the CSIO channel.
TOUT	46/109	**Timer Out** (Output, active High): Pulse output from PRT1.

Table 26. PCMCIA Interface Signals (Continued)

PCIRQ	87	**PCMCIA Interrupt Request** (Output, active Low): After the PCMCIA interface is reset it is in a MEMORY-ONLY mode, and this signal is driven Low to signify a Busy state until the 380C writes a register bit to indicate it is ready. After the card is then configured by the Host, PCIRQ goes Low to request a Host PC interrupt when the internal INT0 signal is asserted by the MIMIC. PCIRQ is monitored by the PCMCIA Host adapter and, dependent on the configuration, connected to one of the Host interrupts (for example, COM1 or COM2 interrupt). PCIRQ can be programmed to be a pulsed interrupt with a minimal pulse length of one microsecond, or a level-interrupt that is reset when the interrupt is processed by the Host. This choice is made by means of bit 6 of the Configuration Option Register.
PCRESET	92	**PCMCIA Reset** (input, active High): Setting PCRESET High resets the PCMCIA interface. The card configuration register is cleared and the PCMCIA interface operates in the MEMORY-ONLY mode until it is configured again. The attribute memory has to be initialized by the controller, and the Ready/Busy (PCIRQ) signal has to be deactivated.
STSCHG	88	**PCMCIA Status Change** (output): This output is controlled by a bit in the PCMCIA module's 380C Control Register.

Table 27. Other Signals

Pin Name	Pin Number(s)	Description
CLKI	128	**Clock/Crystal** (input, active High): An externally generated clock can be input at this pin. Alternatively, a crystal can be connected between CLKI and CLKO. In either case, the frequency at this pin can be used directly as the processor clock (BUSCLK), or divided by two or multiplied by two, under software control.
CLKO	129	**CLKO Crystal** (output, active High): Crystal oscillator connection.This pin must be left open if an externally generated clock is input at the CLKI pin. Feedback on this pin can be disabled by software to save power and noise when an external clock is used.
IEI	47	**Interrupt Enable In** (input, active High): If external devices are connected to INT0, and have higher interrupt priority than the on-chip MIMIC, DMAs, and HDLC controllers, this signal must be connected to the IEO output of the lowest-priority among such devices.
IEO	48	**Interrupt Enable Out** (output, active High): If external devices are connected to INT0, and have lower interrupt priority than the on-chip MIMIC, DMAs, and HDLC controllers, this signal must be connected to the IEI input of the highest-priority device.
V_{DD}	5, 23, 41, 59, 77, 95, 113, 131	**Power Supply**: These eight pins carry power to the device. They must be tied to the same voltage externally.
V_{SS}	14, 32, 50, 68, 86, 104, 122, 140	**Ground**: These eight pins are the ground references for the device. They must be tied to the same voltage externally.

Functional Description

The functional blocks within the Z382 can be broadly identified as central processing unit, host interface, serial communication channels, DMA control, timers and counters, and system interface logic. Each of these blocks are further described in the sections which follow.

For additional information, please refer to the Z382 User's Manual, available from your ZiLOG representative or distributor.

Central Processing Unit

The Central Processing Unit (CPU) core of the Z382 is the 380C (Z380), which is a binary-compatible extension of the Z80® and Z180™ CPU architectures. High

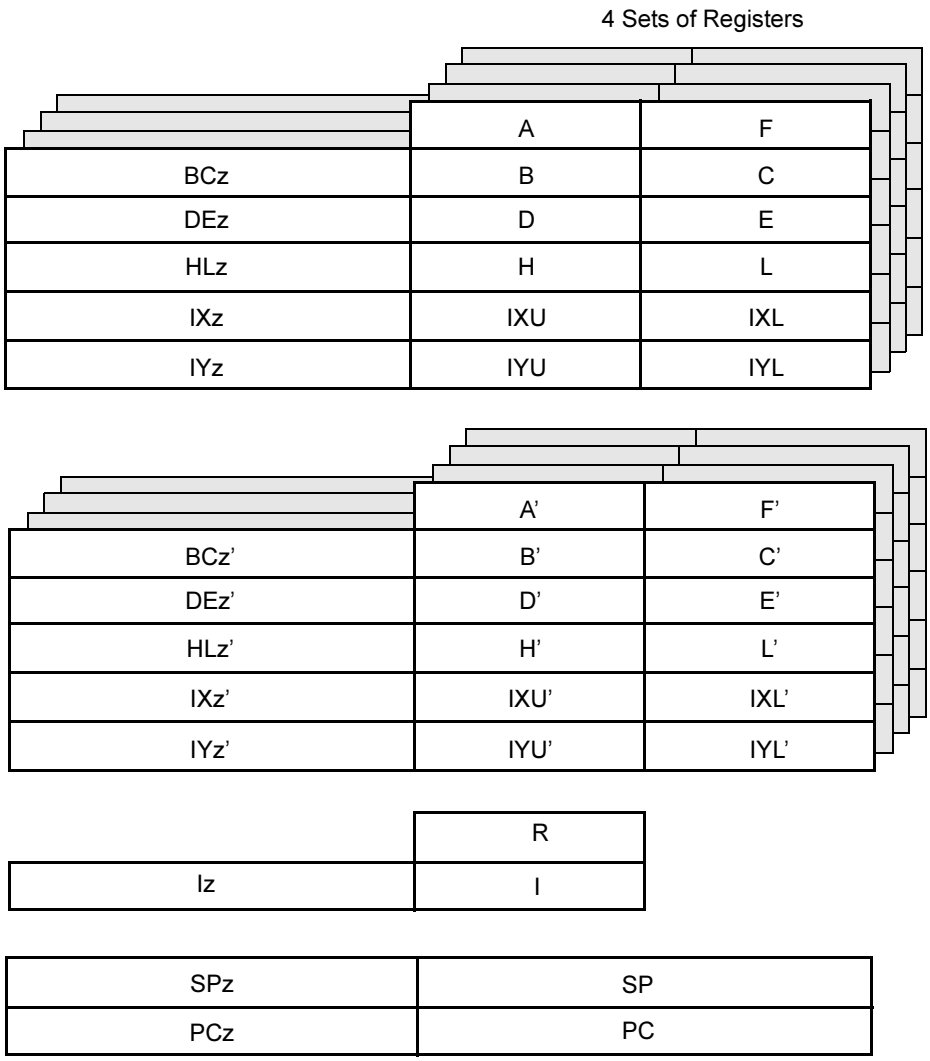

Figure 22. 380C Processor Core Register Set

Primary and Working Registers. The working register set is divided into the two register files; the primary file and the alternate file (designated by '). Each file contains an 8-bit Accumulator (A), a Flag register (F), and six general-purpose registers (B, C, D, E, H, and L). Only one file can be active at any given time, although data in the inactive file can still be accessed. Exchange instructions allow the programmer to exchange the active file with the inactive file.

The accumulator is the destination register for 8-bit arithmetic and logical operations. The six general-purpose registers can be paired (BC, DE, and HL), and are

Table 29. MIMIC-Host Registers

Register	Host Address[1]	380C I/O Address
Receiver Buffer Register	00H[2]	00F0H
Transmit Holding Register	00H[2]	00F0H
Interrupt Enable Register	01H[2]	00F1H
Interrupt ID Register	02H	—
Line Control Register	03H	00F3H
Modem Control Register	04H	00F4H
Line Status Register	05H	00F5H
Modem Status Register	06H	00F6H
Scratch Register	07H	00F7H
Divisor Latch MS Byte	01H[3]	00F9H
Divisor Latch LS Byte	00H[3]	00F8H
FIFO Control Register	02H	00E9H
MIMIC Modification Register	—	00E9H

Note:
1. The host address is relative to the MIMIC base address decoded by the PnP ISA or PCMCIA modules in the Z382.
2. DLAB (LCR[7]) = 0.
3. DLAB (LCR[7]) = 1.

Baud Rate Generator

The Baud Rate Generator (BRG) provides emulation timing for the MIMIC. The BRG output clocks the MIMIC emulation counter, while the BRG itself is clocked by the BUSCLK output of the 380C. Two 8-bit registers are provided to program the BRG time constant. On-the-fly modification of the registers does not cause irregular BRG output.

Host DMA Mailbox

The Host DMA Mailbox facility provides a path for Host DMA data transfers separate from the MIMIC COM port. Commands and data flow over the COM port, while the DMA path can be used for other purposes. The Host DMA Mailbox feature includes control registers that allow Host DMA data transfer between Host memory and, for example, a modem speaker/microphone codec. Transfers are driven by the Host's DMA on one side; Z382 DMA channel(s) or programmed I/O

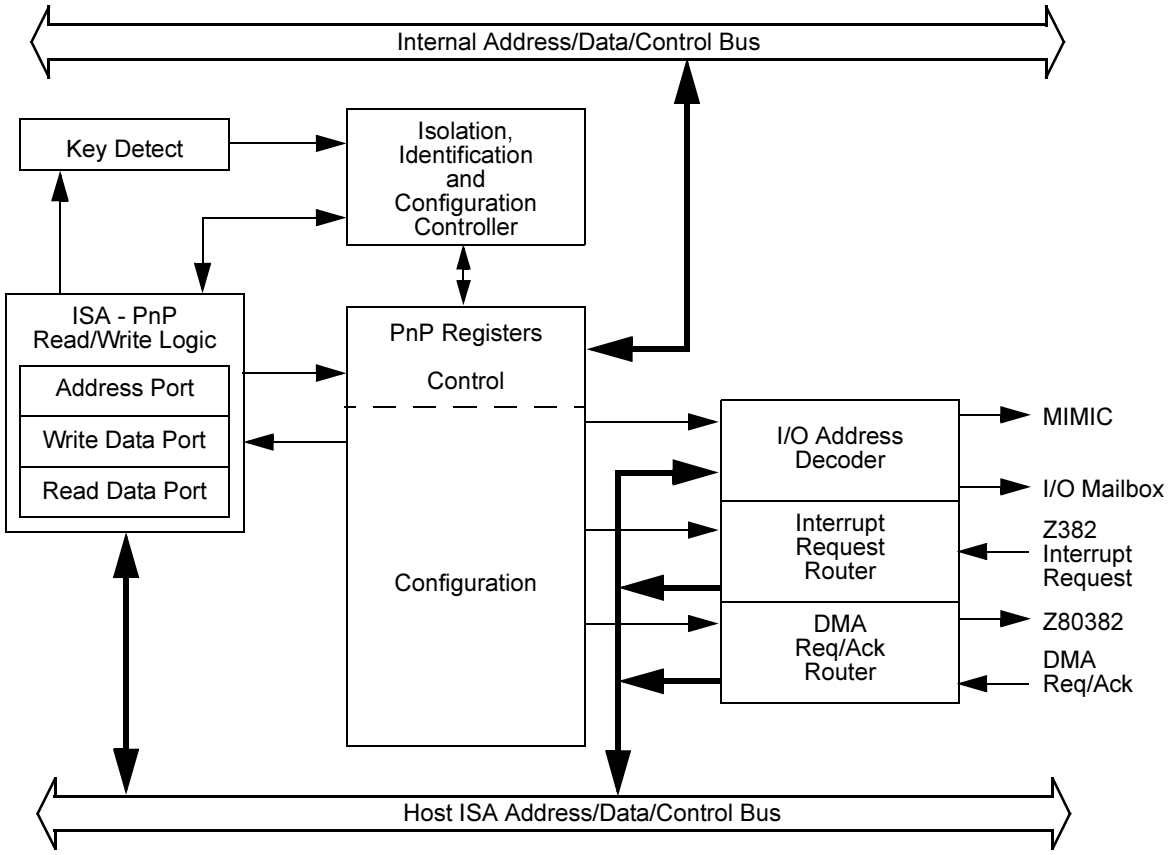

Figure 26. Plug-and-Play Interface Block Diagram

ISA Port

The PnP interface implements three 8-bit ports on the ISA bus. The Address port is a write-only port at the fixed address 0279H. The Write Data port is a write-only port at the fixed address 0A79H. The Read Data port is a read-only port at a programmable address among 0203H, 0207H, 020BH, ..., 03FFH.

The Host may write to the Address port for three reasons:

1. As part of sending an *Initiation key* to all the PnP cards in the system.
2. To select a register on one or all PnP cards as the destination of a subsequent write to the Write Data port.
3. To select a register on one card, or the *Isolation* facility on multiple cards, as the source of data in a subsequent read from the Read Data port.

Configuration Registers

The following Configuration registers are implemented in the Z382 to provide for the resources required by the host to interface to the host-accessible functions within the chip:

- I/O Mailbox I/O Address
- MIMIC I/O Address
- Interrupt Request Level– This register can be selected to be output on either of the two available interrupt output lines. A unique Z382 feature allows these two pins to be configured to be any two of the ISA-bus interrupt lines.
- DMA Channel 0, DMA Channel 1– A unique Z382 feature allows the two DMA pin pairs to be configured to be any two of the seven ISA-bus DMA channels.

Host writes to the Configuration registers are effective immediately, in hardware, so there is no urgent need for the 380C processor to translate them into other register values. But the 380C processor can use the interrupt that occurs when the Host terminates Configuration state to examine what the Host has done to the Configuration registers, and operate accordingly in the future.

PCMCIA Interface

The PCMCIA Interface block integrates all the functions necessary for the operation of I/O interface cards in a PCMCIA 2.0 and 3.0 socket. These functions are:

- PCMCIA Interface Control
- Attribute Memory
- Configuration Registers
- I/O Interface
- Configurable Address Decoder
- Configurable Interrupt Logic
- Z380 Interface

Figure 27 illustrates the PCMCIA Interface block diagram

Interface with a Common TDM Module (for example, GCI/SCIT)

The interface between an HDLC channel and the GCI/SCIT module includes:

Table 34. HDLC Channel/GCI/SCIT Interface

TxD	A bussed line onto which HDLC Transmitters place data in their time slots, as directed by software programming.
RxD	A bussed line from which HDLC Receivers take data in their time slots, as directed by software programming.
BCL	A common bit clock for HDLC Transmitters and Receivers. Transmitters change data on TxD on falling edges of BCL, and Receivers sample data from RxD on rising edges of BCL.
FSC	Frame Sync, synchronous to BCL. Transmitters and Receivers measure their time slots independently from the rising edge of this signal. The duration of FSC can be one or more BCL cycles.
$\overline{\text{TxEN}}$	An output from each Transmitter to the common TDM module, indicating its time slot, that is, when it is placing data on TxD.

TDM Processing

When the Transmit (Receive) TDM Length register is non-zero, the Transmitter (Receiver) activates its Time Slot Assigner to clock Tx (Rx) data only within the time slot. If a TDM Start register is non-zero, after each pulse on Frame Sync, the Time Slot Assigner blocks clocking for the number of bits specified by the TDM Start register. Then, or immediately at Frame Sync if the Start value is zero, clocking is enabled for the number of bits specified by the TDM Length register. Thereafter, clocking is blocked until the next Frame Sync pulse. For example, the Start and Length values for the GCI subchannels are:

Table 35. GCI Subchannel Start and Length Values

Channel	Start	Length
B1 (64K bps)	0	8
B1 (56K)	0	7
B2 (64K)	8	8
B2 (56K)	8	7
D	24	2
IC1	32	8
IC2	40	8

stream (clock slave) units. When this indication is received, a deactivation confirmation is issued, followed by stopping the clocks (forcing them Low) and placing the data pin in a high impedance state. After the clocks are stopped, the input pin is monitored for the presence of a timing request from the downstream unit (the pin being pulled Low).

Deactivation Request, Downstream to Upstream. Deactivation is normally initiated by the upstream device as described previously. When the downstream device receives the deactivation request over the C/I0 channel, it responds by sending the deactivation indication.

Activation Request, Downstream to Upstream. The downstream device can request that the clocks be started by pulling its data output line low. Once the clocks are started, the downstream unit requests activation by sending an activation request over the C/I0 channel.

Activation, Upstream to Downstream. The upstream unit activates the bus by starting the clocks and following the C/I0 channel-based activation procedure.

B1, B2, D, IC1, IC2 Channel Data. Rx data and the bit clock are supplied to the HDLC cells, and Tx data is taken from the HDLC cells. Each HDLC Transmitter and Receiver includes a Time Slot Assigner which can be programmed for any of the subchannels shown above.

Note: The HDLC Transmitters signal when they are sending data. These signals should not conflict with transmission by the GCI/SCIT module, but if they do, the HDLC modules have priority.

GCI/SCIT Registers

The GCI/SCIT interface includes the following I/O-mapped registers that can be read and written by the 380C processor:

- GCI Control Register
- Monitor 0 Transmit Data Register
- Monitor 0 Receive Data Register
- Monitor 1 Transmit Data Register
- Monitor 1 Receive Data Register
- C/I0–C/I2 Transmit Data Register
- C/I0–C/I2 Receive Data Register
- C/I1 Transmit Data Register
- C/I1 Receive Data Register
- GCI Status Register 1

Figure 34. CSIO Block Diagram

Note: The three pins associated with the CSIO are multiplexed with other signals and must be configured for CSIO operation in order to use the CSIO as described in this section.

CSIO Registers

The CSIO channel includes the following I/O-mapped registers that can be read and written by the 380C processor:

- Transmit/Receive Data Register
- CSIO Control Register

CSIO Control Register. CNTR is used to monitor CSIO status, enable and disable the CSIO, enable and disable interrupt generation, and select the data clock speed and source.

CSIO Tx/Rx Data Register. TRDR is used for both CSIO transmission and reception in a half-duplex protocol. Thus, the system design must ensure that transmit and receive operations do not occur simultaneously. For example, if a CSIO transmission is attempted while the CSIO is receiving data, a CSIO does not work. Also, the TRDR is not buffered. Thus, attempting to perform a CSIO transmit while the previous transmit data is still being shifted out causes the shift data to be immediately updated, corrupting the transmit operation in progress. Similarly, reading TRDR while a transmit or receive is in progress must be avoided.

Counters, Timers and Other Miscellaneous Logic

Programmable Reload Timer

Figure 35 illustrates the Programmable Reload Timer block diagram.

device to perform its interrupt functions. Finally, a DRAM refresh function is incorporated, with programmable refresh transaction burst size.

I/O Bus Control

The Z382 is designed to interface easily with external I/O devices that can be of the Z80 product family by supplying four I/O bus control signals: M1, IORQ, IORD, and IOWR. In addition, the Z382 supplies an IOCLK that is a divided down version of its BUSCLK. Programmable wait states can be inserted in the various I/O transactions.

DRAM Refresh

The Z382 is capable of providing refresh transactions to dynamic memories that have internal refresh address counters. A user can select how often refresh requests should be made to the Z80's External Interface Logic, as well as the burst size (number of refresh transactions) for each request iteration. The External Interface Logic grants these requests by performing refresh transactions with CAS-before-RAS timing on the TREFR, TREFA and TREFC bus control signals. In these transactions, BHEN, BLEN and the user specified chip select signal(s) are driven active to facilitate refreshing all the DRAM modules at the same time. A user can also specify the T1, T2 and T3 waits to be inserted.

Note: The Z382 cannot provide refresh transactions when it relinquishes the system bus, with its BREQ input active. In that situation, the number of missed refresh requests are accumulated in a counter, and when the Z382 regains the system bus, the missed refresh transactions are performed.

Low Power STANDBY Mode

The Z382 provides an optional STANDBY mode to minimize power consumption during system idle time. If this option is enabled, executing the Sleep instruction stops the Z382's oscillator if it is in use, and in any case stops clocking internal to the Z382 (except to PRT0 if it is enabled) and at the BUSCLK and IOCLK outputs. The STNBY and HALT signals go Low to indicate that the Z382 is entering the standby mode. All Z382 operations are suspended, the bus control signals are driven inactive and the address bus is driven High. STANDBY mode can be exited by asserting any of the RESET, NMI, INT3-INT0 (if enabled), or optionally, BREQ inputs.

If STANDBY mode is not enabled, the Sleep instruction does not stop the Z382's oscillator if it is in use, but blocks clocking from internal modules, except PRT0 if it is enabled. In this case, STNBY (but not HALT) goes Low to indicate the Z382's status.