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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z380C
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	144-LQFP
Supplier Device Package	144-VQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8l38210asc

Z80382, Z8L382 Data Communications Processor

Features

- Embedded Z380™ Microprocessor
  - Maintains Object Code Compatibility with Z80® and Z180™ Microprocessors
  - Enhanced Instruction Set for 16-Bit Operation
  - 16 MB Linear Addressing
  - Two Clock Cycle Instruction Execution Minimum
  - Four On-Chip Register Banks
  - BC/DE/HL/IX/IY Augmented to 32 Bits
  - Clock Divide-by-Two and Multiply-by-Two Options
  - Fully Static CMOS Design with Low-Power STANDBY Mode
  - 16-Bit Internal Bus
  - Dynamic Bus Sizing (8/16-Bit Inter-Operability)
- 16550 MIMIC with I/O Mailbox, DMA Mailbox, and 16 mA Bus Drive
- Three HDLC Synchronous Serial Channels
  - Serial Data Rate of up to 10 Mbps
- GCI/SCIT Bus Interface
- Eight Advanced DMA Channels with 24-Bit Addressing
- Plug-and-Play ISA Interface
- PCMCIA Interface
- Two Enhanced ASCIs (UARTs) with 16-Bit Baud Rate Generators (BRG)
- Clocked Serial I/O Channel (CSIO) for Use with Serial Memory
- Two 16-Bit Timers with Flexible Prescalers
- Three Memory Chip Selects with Wait-State Generators
- Watch-Dog Timer (WDT)

cuted at much higher speeds. Memory bus sizes can be configured internally by software to eliminate the need for external logic to drive MSIZE.

Some features that have traditionally been handled by external peripherals have been incorporated in the Z382. These on-chip peripherals reduce system chip count and interconnections on the external bus. These peripherals, illustrated in the Z382 Block Diagram in Figure 1, are summarized below.

HDLC Synchronous Channels. Three HDLC channels operate at serial data rates of up to 10 Mbps and feature 8-byte receive and transmit FIFOs. These can be used for modems, general data communications, and ISDN. The ISDN can be handled separately or through the GCI/SCIT bus interface. HDLC Channels always transfer data through the DMA channels. A transparent mode is selectable. Two of the HDLC cells can be pin multiplexed with the ASCIs (UARTs) to provide dynamically switchable (async-sync) DTE interfaces.

DMA Channels. The eight DMA channels provide 24-bit memory addressing and can transfer memory block sizes of up to 64 KB (16-bits) word. These DMA channels can be dynamically assigned to serve the HDLC ports, MIMIC COM port, Host DMA Mailbox, or ASCIs in any mixture. Linked list operation allows all HDLC transmitters and receivers to operate at or above T1/E1 rates simultaneously without loading the bus bandwidth.

16550 MIMIC. Provides connection to a PC ISA bus and emulation of the 16550 UART register set. Improvements include 16 mA output drivers and internal COM port address decoding to reduce external PC interface components.

ASCI. Two flexible asynchronous serial channels with baud rate generators, modem control and status.

CSIO. A clocked serial I/O channel which can be used for serial memory interface.

Timers. Two 16-bit counter/timers with flexible prescalers for wide-range timing applications.

GCI/SCIT Bus Interface. A common interface to ISDN interface devices. Internal signals from this module can be connected to the HDLC channels to provide two B-channels and one D-channel for ISDN.

Plug-and-Play ISA Interface. Provides auto-configuration in ISA (AT bus) applications.

PCMCIA Interface. Provides connectivity to a PCMCIA bus.

32-Bit General-Purpose I/O. For non-PC add-in applications, four 8-bit ports are provided for general- purpose I/O. In ISA or PCMCIA applications, the pins from two of the ports are reallocated to host bus signals and are not available. Pins from the other two ports are selectively multiplexed with on-chip peripheral functions (ASCIs, CSIO, PRT). These pins are individually programmable for input/output mode.

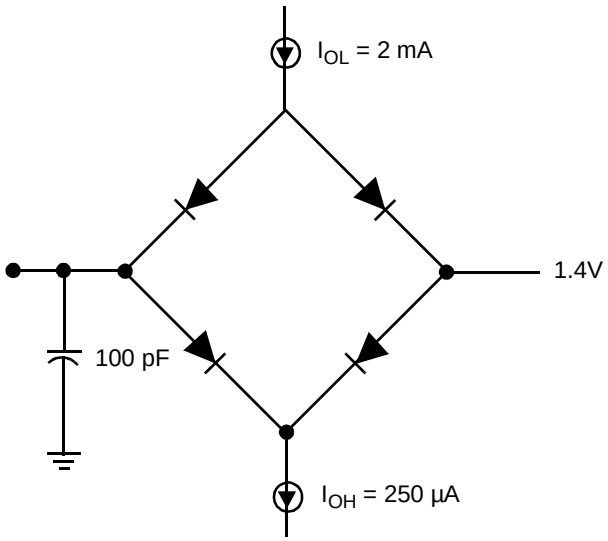

Figure 3. Test Load Diagram

DC Characteristics

Pin Numbers and Input/Output Classifications

Table 1. Pin Numbers and Input/Output Classifications

Pin	Input Class[1]	Output Class[1]	Pin Number(s)
$\overline{\text{BHEN}}$		O	118
$\overline{\text{BLEN}}$		O	119
$\overline{\text{BUSACK}}$		O	132
$\overline{\text{BUSREQ}}$	I		133
$\overline{\text{CTS0}}$/$\overline{\text{HRD}}$/$\overline{\text{PCIORD}}$	I		61
$\overline{\text{CTS0}}$/$\overline{\text{TREFA}}$	I	O	111
$\overline{\text{CTS1}}$/$\overline{\text{HWR}}$/$\overline{\text{PCIOWR}}$	I		60
$\overline{\text{CTS1}}$/$\overline{\text{TREFC}}$	I	O	110
$\overline{\text{DCD0}}$/$\overline{\text{HDAK0}}$/$\overline{\text{PCWE}}$	I		89
$\overline{\text{DCD0}}$/$\overline{\text{TREFR}}$	I	O	112
$\overline{\text{DCD1}}$/HA9	I		66
$\overline{\text{HALT}}$		O	121

Table 1. Pin Numbers and Input/Output Classifications (Continued)

Pin	Input Class[1]	Output Class[1]	Pin Number(s)
V_{DD}			5, 23, 41, 59, 77, 95, 113, 131
V_{SS}			14, 32, 50, 68, 86, 104, 122, 140

Note: 1. Characteristics of each pin are listed in terms of the classifications in the DC Characteristics Table 2 and Table 3 which follow.

Specifications apply over Standard Operating Conditions unless otherwise noted.

Table 2. Output Class Characteristics

Output Class(1)	Type	V_{OL} Max.	V_{OH} Min.	C_{OUT} Max.(2)
O	Totem Pole	0.4V @ I_{OL} = 2.0 mA	V_{DD} - 1.2V @ I_{OH} = 200 µA	15 pF
		Slew Rate = 0.33 V/ns min @ C_{LOAD} = 50 pF		
3	3-State	0.4V @ I_{OL} = 2.0 ma	V_{DD} - 1.2V @ I_{OH} = 200 µA	
		Slew Rate = 0.33 V/ns min @ C_{LOAD} = 50 pF		
H	High Drive 3-State	0.4V max @ I_{OL} = 16 mA, V_{DD} = 5V	2.4V min @ I_{OH} = 5mA, V_{DD} = 5V	15 pF
		Slew Rate = 0.33 V/ns min @ C_{LOAD} = 50 pF		
D	Open-Drain	0.4V max @ I_{OL} = 16 mA	--	15 pF

Notes:
1. The Pin Numbers and Input/Output Classifications described in Table 1 identifies the specific output pins in each class.
2. Applies to Output only or I/O.

Table 3. Input Class Characteristics

Input Class[1]	V_{IL} Max. (Z80382)	V_{IL} Max. (Z8L382)	V_{IH} Min. (Z80382)	V_{IH} Min. (Z8L382)	Minimum Hysteresis
I	0.8V	0.6V	2.0V	2.0V	0.4V
	I_I = ±10 µA max, V_I = 0 to 5V (includes leakage if I/O) C_{IN} = 5 pF max (if input only, see output type if I/O)				
	Note: Inputs of this type include a weak-latch circuit, except that a register bit can disable those for pins PB7-0.				
R	0.4V	0.4V	V_{DD} - 0.6V	V_{DD} - 0.3V	0.4V
	I_I = ±10 µA max, V_I = 0 to 5V C_{IN} = 5 pF max				
	Note: Inputs of this type except CLKI include a weak-latch circuit.				

Note: The Pin Numbers and Input/Output Classifications described in Table 1 identifies the specific input pins in each class.

Host-PCMCIA Attribute Memory Read Timing (See Figure 5)

Specifications apply over Standard Operating Conditions unless otherwise noted. C_L = 50 pF for outputs.

Table 6. Host-PCMCIA Attribute Memory Read Timing

		Z80382		Z8L382		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
t22	Address Setup to $\overline{\text{PCCE1}}$ Fall	15		20		ns
t23	Address Setup to $\overline{\text{PCOE}}$ Fall	15		20		ns
t24	Address Hold from $\overline{\text{PCCE1}}$ High	5		5		ns
t25	Address Hold from $\overline{\text{PCOE}}$ High	5		5		ns
t26	$\overline{\text{PCCE1}}$ Low to Data Active	0		0		ns
t27	$\overline{\text{PCOE}}$ Low to Data Active	0		0		ns
t28	$\overline{\text{PCCE1}}$ Low to Data Valid		60		60	ns
t29	$\overline{\text{PCOE}}$ Low to Data Valid		60		60	ns
t30	Data Invalid from $\overline{\text{PCCE1}}$ High	5		5		ns
t31	Data Invalid from $\overline{\text{PCOE}}$ High	5		5		ns
t32	Data 3-state from $\overline{\text{PCCE1}}$ High		20		20	ns
t33	Data 3-state from $\overline{\text{PCOE}}$ High		20		20	ns
Note: Timings also apply for reads from registers located in the attribute memory space.						

Host-PCMCIA I/O Write Timing (See Figure 8)

Specifications apply over Standard Operating Conditions unless otherwise noted. C_L = 50 pF for outputs.

Table 9. Host-PCMCIA I/O Write Timing

		Z80382		Z8L382		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t55	Address Setup to $\overline{\text{PCIOWR}}$ Fall	50		50		ns
t56	$\overline{\text{PCREG}}$ Setup to $\overline{\text{PCIOWR}}$ Fall	5		5		ns
t57	$\overline{\text{PCCE1}}$ Setup to $\overline{\text{PCIOWR}}$ Fall	5		5		ns
t58	$\overline{\text{PCIOWR}}$ Low Width	125		125		ns
t59	Data Setup to $\overline{\text{PCIOWR}}$ Rise	35		35		ns
t60	Data Hold from $\overline{\text{PCIOWR}}$ High	20		20		ns
t61	$\overline{\text{PCCE1}}$ Hold from $\overline{\text{PCIOWR}}$ High	10		10		ns
t62	$\overline{\text{PCREG}}$ Hold from $\overline{\text{PCIOWR}}$ High	10		10		ns
t63	Address Hold from $\overline{\text{PCIOWR}}$ High	10		10		ns

ASCI Receiver Timing (See Figure 12)

Specifications apply over Standard Operating Conditions unless otherwise noted. C_L = 50 pF for outputs.

Table 13. ASCI Receiver Timing

		Z80382		Z8L382		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t79	External Receive Clock Period	50		50		ns
t80	External Receive Clock Low Time	30		30		ns
t81	External Receive Clock High Time	30		30		ns
t82	External Receive Clock Fall Time		5		10	ns
t83	External Receive Clock Rise Time		5		10	ns
t84	RXA Setup to CKA Rise	20		25		ns
t85	RXA Hold from CKA High	5		5		ns

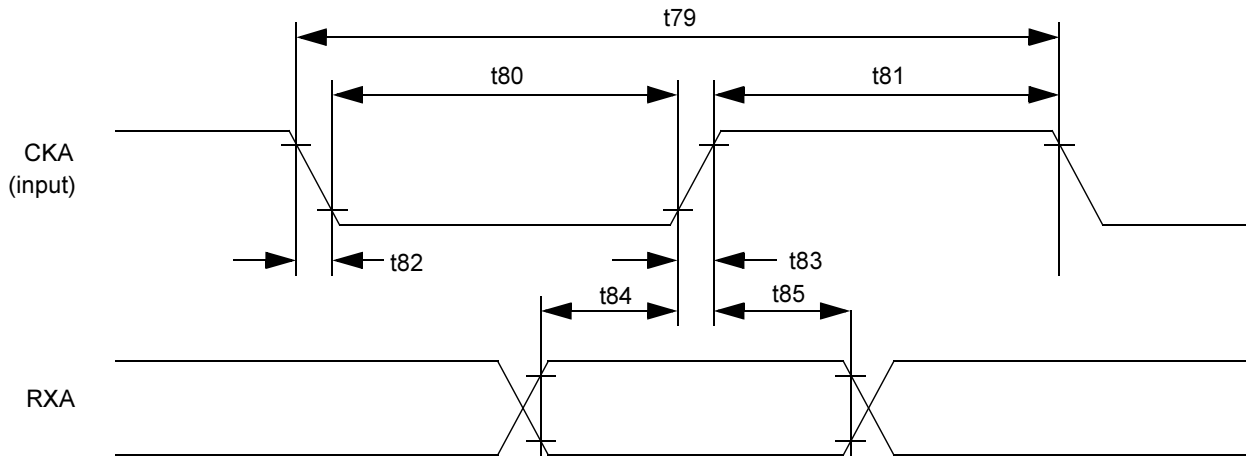

Figure 12. ASCI Receiver Timing Diagram

Table 21. Multiprocessor Unit (MPU) Signals (Continued)

Pin Name	Pin Number(s)	Description
D15-0	24 - 31 33 - 40	**D15-0 Data Bus** (input/output, active High, 3-state): This bidirectional 16-bit data bus is used for data transfer between the 380C and memory or I/O devices. In a memory word transfer, the even-addressed (A0=0) byte is transferred on D7-0, and the odd-addressed (A0=1) byte on D15-8. 8-bit memories should be connected to D7-0, while 8-bit I/O devices should be attached to D15-8 (this difference tends to equalize electrical loading). (See note under BLEN pin description on page 38.)
HALT STNBY	121 120	**HALT, STANDBY Status** (outputs, active Low): These two outputs indicate the status of the Z382 as follows: STNBY / HALT / Mode H / H / Normal instruction execution H / L / HALT instruction L / H / SLEEP Mode: clock runs but is blocked from most of the chip L / L / STANDBY Mode: oscillator is stopped
INT3 INT2 INT1	139 138 137	**Interrupt Requests** (inputs, active Low): Asynchronous maskable interrupt inputs. Can be selected as low- or high-level sensitive, or as falling- or rising-edge triggered.
INT0	136	**Interrupt Request** (input, active Low): INT0 is logically ORed (positive-logic ANDed) with the interrupt requests from the on-chip MIMIC, DMAs, and HDLC controllers, to create the processor's INT0 input.
IOCLK	114	**Input/Output Clock** (output, active High, 3-state): This signal is a program controlled divided-down version of BUSCLK. The division factor can be two, four, six or eight with I/O transactions and interrupt-acknowledge transactions occurring relative to IOCLK. IOCLK can be disabled, in which case BUSCLK is the timing reference for I/O transactions. Note: The INTACK output of the Z380 has been omitted on the Z382 for pinning reasons. A similar signal can be easily obtained by low-active-ANDing (positive-logic ORing) the M1 and IORQ outputs.
IORQ	115	**Input/Output Request** (output, active Low, 3-state): This signal is active during all I/O read and write transactions and interrupt acknowledge transactions.
IORD	125	**Input/Output Read Strobe** (output, active Low, 3-state): This signal is used to strobe data from the peripherals during I/O read transactions.
IOWR	123	**Input/Output Write Strobe** (output, active Low, 3-state): This signal is used to strobe data into the peripherals during I/O write transactions.
IOCS1 IOCS2	45 46	**Input/Output Chip Select** (output, active Low): These outputs may be used to access external I/O devices. The base I/O address and range are programmable.

Table 21. Multiprocessor Unit (MPU) Signals (Continued)

Pin Name	Pin Number(s)	Description
$\overline{M1}$	116	**Machine Cycle One** (output, active Low, 3-state): This signal is active during instruction fetch and interrupt acknowledge transactions. The Z382 does not support RETI decoding by Z80 peripherals (PIO, SIO, and CTC). It does support Z80-type interrupt daisy-chaining by devices that include explicit clearing of IUS (for example, SCC).
$\overline{MRD}$	126	**Memory Read** (output, active Low, 3-state): This signal indicates that the addressed memory location places its data on the data bus. $\overline{MRD}$ is active from the end of T1 until the end of T4 during memory read transactions.
$\overline{MSIZE}$	117	**Memory Size** (input/open-drain output, active Low): In 16-bit memory operations, this signal indicates whether the addressed memory location is word size (logic High) or byte size (logic Low). In the latter case, the 8-bit memory is connected to the D7-0 lines, and an additional memory transaction on D7-0 automatically is generated to transfer the other byte of the word. (See the note on pin name swapping after the $\overline{BLEN}$ pin description on page 38) $\overline{MSIZE}$ is driven as an open-drain output by the memory decoding modules, when they are enabled in 8-bit mode and the address falls within their range.
$\overline{MWR}$	124	**Memory Write** (output, active Low, 3-state): This signal indicates that the addressed memory location stores the data on the databus, as qualified by $\overline{BHEN}$ and $\overline{BLEN}$. $\overline{MWR}$ is active from the end of T2 until the end of T4 during memory write transactions.
$\overline{NMI}$	135	**Nonmaskable Interrupt** (input, falling edge-triggered): This input has higher priority than the maskable interrupt inputs INT3-INT0.
$\overline{RESET}$	134	**Reset** (input, active Low): This input must be active for a minimum of five BUSCLK periods to initialize the Z382. The effect of $\overline{RESET}$ is described in detail in the Reset section.
$\overline{ROMCS}$	42	**ROM Chip Select** (output, active Low): After Reset, the Z382 drives this output and $\overline{MSIZE}$ Low for all memory accesses with A23=0. Software can program the chip select logic to assert $\overline{ROMCS}$ for a different range of memory addresses. If ROM is 16 bits wide and composed of two 8-bit devices, connect the Chip Select inputs of both devices to $\overline{ROMCS}$, and program the hardware not to force $\overline{MSIZE}$ Low in the first two instructions of the ROM code.

Table 23. ISA Bus Signals

Pin Name	Pin Number(s)	Description
HD7-0	78 - 85	**Host Data Bus** (Input/Output, 3-state): ISA or PCMCIA data bus.
$\overline{\text{HDOEN}}$	62	**Host Data Output Enable** (Output, active Low): This signal goes Low when the Host reads data from the MIMIC, the I/O Mailbox, or the Plug and Play interface, and during Host DMA read cycles.
HA11-0	64 - 67 69 - 76	**Host Address** (Input): Part of the ISA or PCMCIA address bus. The MS bits can be decoded by the built-in address decoder; bits 2-0 determine which MIMIC register the Host accesses. Bits 11-10 are decoded only by the Plug and Play ISA module.
HAEN	63	**Host Address Enable** (Input): HAEN must be Low to qualify COM Port decoding, I/O Mailbox decoding, and Plug and Play decoding. To support 16-bit decoding of Host I/O addresses, provide an external decoder for HA15-12 and HAEN all Low and connect its Low-active output to this pin.
$\overline{\text{HWR}}$	60	**Host Write** (Input, active Low): The Host drives this input Low to signal the MIMIC that a write operation is taking place.
$\overline{\text{HRD}}$	61	**Host Read** (Input, active Low): This input is used by the Host to signal the MIMIC interface that a read operation is taking place.
HINT1 HINT2	87 88	**Host Interrupt** (Outputs, active High): One of these outputs is driven High by the Plug and Play module when the MIMIC requests an interrupt from the Host. The unused signal is 3-stated.
$\overline{\text{HDAK0}}$ HDAK1	89 90	**Host DMA Acknowledge** (Inputs, active Low): These inputs indicate that the Host DMA controller has acknowledged the request and is transferring data.
HDRQ0 HDRQ1	91 92	**Host DMA Request** (Outputs, active High, 3-state): These outputs request a DMA transfer operation from the Host.

Table 27. Other Signals

Pin Name	Pin Number(s)	Description
CLKI	128	**Clock/Crystal** (input, active High): An externally generated clock can be input at this pin. Alternatively, a crystal can be connected between CLKI and CLKO. In either case, the frequency at this pin can be used directly as the processor clock (BUSCLK), or divided by two or multiplied by two, under software control.
CLKO	129	**CLKO Crystal** (output, active High): Crystal oscillator connection.This pin must be left open if an externally generated clock is input at the CLKI pin. Feedback on this pin can be disabled by software to save power and noise when an external clock is used.
IEI	47	**Interrupt Enable In** (input, active High): If external devices are connected to INT0, and have higher interrupt priority than the on-chip MIMIC, DMAs, and HDLC controllers, this signal must be connected to the IEO output of the lowest-priority among such devices.
IEO	48	**Interrupt Enable Out** (output, active High): If external devices are connected to INT0, and have lower interrupt priority than the on-chip MIMIC, DMAs, and HDLC controllers, this signal must be connected to the IEI input of the highest-priority device.
V_{DD}	5, 23, 41, 59, 77, 95, 113, 131	**Power Supply**: These eight pins carry power to the device. They must be tied to the same voltage externally.
V_{SS}	14, 32, 50, 68, 86, 104, 122, 140	**Ground**: These eight pins are the ground references for the device. They must be tied to the same voltage externally.

Functional Description

The functional blocks within the Z382 can be broadly identified as central processing unit, host interface, serial communication channels, DMA control, timers and counters, and system interface logic. Each of these blocks are further described in the sections which follow.

For additional information, please refer to the Z382 User's Manual, available from your ZiLOG representative or distributor.

Central Processing Unit

The Central Processing Unit (CPU) core of the Z382 is the 380C (Z380), which is a binary-compatible extension of the Z80® and Z180™ CPU architectures. High

data are not transferred to the FIFO. Any time a break is detected, the receiver can not receive any more data until the RXA pin returns to a High state.

Data transfers from the receive FIFO can be performed using I/O instructions or by using one of the DMA channels. This DMA process reads characters from the RDR as an associated status bit indicates that data is available. The RxDMA request is disabled when any of the error flags (PE, FE or OVRN) is set, so that software can identify with which character a problem is associated.

ASCI Status FIFO/Register

This FIFO contains Parity Error, Framing Error, Rx Overrun, and Break status bits associated with each character in the receive data FIFO. The status of the oldest character (if any) can be read from the ASCI status register, which also provides several other status conditions which are non-FIFO.

The outputs of the error FIFO go to the set inputs of software-accessible error latches in the status register. Writing a 0 to the Error Flag Reset (EFR) bit in CNTLA is the only way to clear these latches. In other words, when an error bit reaches the top of the FIFO, the bit sets an error latch. If the FIFO has more data and the software reads the next byte out of the FIFO, the error latch remains set until the software writes a 0 to the EFR bit. The error bits are cumulative, so if additional errors are in the FIFO they set any unset error latches as they reach the top.

Baud Rate Generator

The baud rate generator (BRG) features two modes. The first mode provides a dual set of fixed clock divide ratios. In the second mode, the BRG is configured as a sixteen-bit down counter that divides the processor clock by the value in a software accessible, sixteen-bit, time constant register. This condition allows virtually any frequency to be created by appropriately selecting the main processor clock frequency. The BRG can also be disabled in favor of an external clock on the CKA pin.

The Receiver and Transmitter subsequently divide the output of the Baud Rate Generator (or the signal from the CKA pin) by 1, 16 or 64 under program control.

ASCI Register Set

Each ASCI contains a set of registers for programming various aspects of its operation. These registers are:

- Control Register A
- Control Register B
- Time Constant High Register

Baud Rate Generator and DPLL

If an HDLC channel's Tx clock is taken from its Baud Rate Generator (BRG), and/or its Rx clock is taken from its DPLL, then the channel's BRG operates. A BRG counts down from the 16-bit value programmed into its Time Constant LS and MS registers, using the processor's BUSCLK. Each time the value is zero, the BRG toggles its output to the DPLL, and one clock later it reloads the value from the Time Constant registers.

If an HDLC channel's Rx clocking is taken from its DPLL, software programs the channel's Time Constant registers with a 16-bit value corresponding to 16 times the nominal data rate. When the DPLL detects a change on the raw Rx Data (before NRZI decoding), a counter is cleared that is incremented at 16X the nominal bit rate. Half a bit time later, an active edge is provided on its Rx clock output. In the absence of further data transitions the Rx clock is provided as the BRG output divided by 16.

Per-Channel Registers

Each HDLC channel includes the following I/O-mapped registers that can be read and written by the 380C processor:

- Transmit Mode Register
- Transmit Control/Status Register
- Transmit Interrupt Register
- Transmit Fill Register
- Receive Mode Register
- Receive Interrupt Register
- DMA Select Register
- Counter Access Port

Transmit Mode Register. This register selects the main operating mode of the Transmitter (TRANSPARENT, HDLC, NRZI HDLC), its I/O configuration (TDM, I/O by means of device pins, and so on), when DMA data transfers are requested, and action to be taken if an underrun occurs.

Tx Control/Status Register. This register controls the minimum number of bits sent between frames and the minimum number of bits sent after the Transmitter is enabled before the first data character of a frame is sent, what the Transmitter sends between frames, and the type of CRC used. Feedback is also provided on the current state of the transmitter.

Monitor Channel Operation

The monitor channels are full duplex and operate on a pseudo-asynchronous basis, in other words, data transfers take place synchronized to frame sync but the flow is controlled by a handshake procedure using the MX and MR bits. Figure 32 illustrates the handshake procedure (flow of events).

Idle. The MX and MR pair being held inactive (High) for two or more frames constitutes the channel being idle in that direction. The data received in the monitor channel is invalid and should be 11111111.

Start of Transmission. The first byte of data is placed on the bus and MX is activated (Low). MX remains active, and the data is repeated until an inactive-to-active transition of MR is received, indicating that the data has been captured by the receiver.

Subsequent Transmissions. The second and subsequent bytes are placed on the bus after the inactive to active transition of MR. At the time that the second byte is transmitted, MX is returned inactive for one frame time only; the data is valid in the same frame. In the following frame, MX returns active again and the same byte is transmitted. Data is repeated in subsequent frames and MX remains active until acknowledgment is detected (MR transition from inactive to active).

Maximum Speed Case. The transmitter is capable of minimizing the delay between bytes to achieve higher data throughput than is provided by the general case described previously. The first and second bytes are transmitted normally, However, starting with the third byte, the transmitter deactivates MX and transmits new data one frame time after MR is deactivated. In this way, the transmitter anticipates that MR is reactivated, which it accomplishes one frame time after it is deactivated, unless an abort is signalled by the receiver.

End of Message (EOM). The transmitter sends an EOM, normally after the last byte of data has been transmitted, by not reactivating MX after deactivating it in response to MR going inactive.

Reception. At the time the receiver detects the first byte, indicated by the inactive-to-active transition of MX, MR is inactive. In response to the activation of MX, the data is read off the bus and MR is activated. MR remains active until the next byte is received or an end of message is detected. Subsequent data is received from the bus on each falling edge of MX, and a monitor channel receive data available interrupt is generated. The data may be valid at the time that MX went inactive, one frame time prior to going active. MR is deactivated after the data is read and reactivated one frame time later. The transmitter detects MR going inactive and anticipates its reactivation one frame later. The reception of data is terminated by the reception of an end of message indication.

Abort. The abort is a signal from the receiver to the transmitter indicating that the data has been missed. It is not an abort in the classical sense, which is an indica-

- I/OCS1 High and Low Address Registers
- I/OCS2 High and Low Address Registers

I/O Chip Select 1/2 High and Low Address Registers. Specify the base address and the I/O block size for I/O Chip Selects 1 and 2.

RAM and ROM Chip Selects

Three memory chip select outputs are provided: $\overline{\text{ROMCS}}$, $\overline{\text{RAMCSL}}$, and $\overline{\text{RAMCSH}}$. These outputs support both 8- and 16-bit memories, and are asserted for a selected address range (4 KB to 8 MB) during both memory and I/O cycles. Unlike Chip Select and $\overline{\text{MSIZE}}$ signalling, Wait State generation can be specified which occurs only during memory cycles.

For the selected ROM and/or RAM range, the $\overline{\text{MSIZE}}$ pin can be programmed to be forced Low in an open-drain fashion when the address is in the programmed range, forcing 8-bit accesses in one or both ranges. When $\overline{\text{MSIZE}}$ is forced for 8-bit RAM in this way, $\overline{\text{RAMCSL}}$ is asserted for all cycles in the selected address range, and the $\overline{\text{RAMCSH}}$ pin assumes its alternate use as port pin PC7. When $\overline{\text{MSIZE}}$ is not forced for 8-bit RAM, $\overline{\text{RAMCSL}}$ is qualified by $\overline{\text{BLEN}}$, and $\overline{\text{RAMCSH}}$ acts as a chip select output pin and is qualified by $\overline{\text{BHEN}}$.

RAM and ROM Chip Select Registers

The following I/O-mapped registers are associated with the RAM and ROM chip selects and can be read and written by the 380C processor:

- RAM Address High and Low Registers
- ROM Address High and Low Registers
- Memory Mode Register 1
- Memory Mode Register 2

RAM Address High and Low Registers. These registers specify which bits of the address bus are used in the address comparison and thus, the memory block size. The block size can range from 4 KB to 8 MB.

ROM Address High and Low Registers. These registers specify which bits of the address bus are used in the address comparison and thus, the memory block size. The block size can range from 4 KB to 8 MB.

Memory Mode Register 1. This register enables the ROM chip select, specifies the number of wait states for the ROM chip select, and specifies the number of T1 Wait states for the RAM chip select.

Memory Mode Register 2. This register enables the RAM chip select, specifies 8- or 16-bit memory accesses for the RAM and ROM chip selects independently, and specifies the number of T2 and T3 Wait states for the RAM chip select.

Table 39. Z80382 ASCI, PRT, CSIO, WDT Registers

Register Name	I/O Address	Access
ASCI Control Register A Ch 0	0000H	R/W
ASCI Control Register A Ch 1	0001H	R/W
ASCI Control Register B Ch 0	0002H	R/W
ASCI Control Register B Ch 1	0003H	R/W
ASCI Status Register Ch 0	0004H	R/W
ASCI Status Register Ch 1	0005H	R/W
ASCI TX Data Register Ch 0	0006H	R/W
ASCI TX Data Register Ch 1	0007H	R/W
ASCI RX Data Register Ch 0	0008H	R/W
ASCI RX Data Register Ch 1	0009H	R/W
CSIO Control Register	000AH	R/W
CSIO Tx/Rx Data Register	000BH	R/W
Timer Data Register Ch OL	000CH	R/W
Timer Data Register Ch OH	000DH	R/W
Reload Register Ch OL	000EH	R/W
Reload Register Ch OH	000FH	R/W
Timer Control Register	0010H	R/W
Timer Prescale Register	0011H	R/W
ASCI0 Extension Control Register	0012H	R/W
ASCI1 Extension Control Register	0013H	R/W
Timer Data Register Ch 1L	0014H	R/W
Timer Data Register Ch 1H	0015H	R/W
Reload Register Ch 1L	0016H	R/W
Reload Register Ch 1H	0017H	R/W
ASCI0 Time Constant Low	001AH	R/W
ASCI0 Time Constant High	001BH	R/W
ASCI1 Time Constant Low	001CH	R/W

Table 46. Plug-and-Play ISA Registers (Continued)

Register Name	I/O Address	Access	Host
Wake Register	None		PnP 03H, WO
PnP Master Register	0102H	R/W	None
Resource Data Register	0104H	WO	PnP 04H, RO
PnP Status Register	0105H	RO	PnP 05H, RO
Card Select Number (CSN) Register	0106H	RO	PnP 06H, R/W
Logical Device Number Register	None		PnP 07H, RO
Activate Register	0130H	R/W	PnP 30H, R/W
I/O Range Check Register	None		PnP 31H, R/W
I/O Mailbox Base Address Registers	0160,1H	R/W	PnP 60,1H, R/W
MIMIC Base Address Registers	0162,3H	R/W	PnP 62,3H, R/W
Interrupt Request Level Register	0170H	R/W	PnP 70H, R/W
DMA Channel 0,1 Registers	0174,5H	R/W	PnP 74,5H, R/W

Device Errata

The Z382 die revision that is currently shipping in production is the BB revision. This part contains the following errata:

1. The maximum clock speed for revision BB is 20 MHz (1x clock).
2. HAEN Low in address decoding is not included for the MIMIC and I/O Mailbox.
3. In the HDLC transmitter, Tx DMA Request when Tx FIFO is half empty: seems to work like “...when one slot available in Tx FIFO”. This condition is not a fatal error.
4. Bit seven of the System Configuration register was not taken into account in enabling pins 110, 111 and 112. Fixes for this situation include setting bit 5 to 1, or driving those lines to GND. When bit 5 is 0, these pins form an OR function with any other CTS, DCD pin which is enabled. Grounding pins 110, 111 and 112 and setting bit 5 of the System Configuration register to 0 allows the other enabled pin(s) to control the input(s).
5. There is a report that software cannot restart a DMA channel that has quit because it has reached the end of a list by setting the Run bit. This situation can be resolved by restarting the channel, loading the LAR.

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