Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z380C
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	144-LQFP
Supplier Device Package	144-VQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8l38210asg

This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact:

ZiLOG Worldwide Headquarters
910 E. Hamilton Avenue
Campbell, CA 95008
Telephone: 408.558.8500
Fax: 408.558.8300
www.ZiLOG.com

Document Disclaimer

Table of Contents

List of Figures

I/O Chip Selects. Two I/O chip selects are provided to support I/O access of external peripherals. Each has a programmable base address and provides I/O decode sizes ranging from 8 to 512 bytes.

ROM/RAM Chip Selects with Wait-State Generators. Chip select outputs are provided to decode memory addresses and provide memory chip enables. Each chip select has its own Wait State Generator to allow use of memories with different speeds.

Watch-Dog Timer. A Watch-Dog Timer (WDT) with a wide range of time-constants prevents code runaway and possible resulting system damage. The RESET input can be forced as an output upon the terminal count of the WDT. This allows external peripherals to be reset along with the Z382

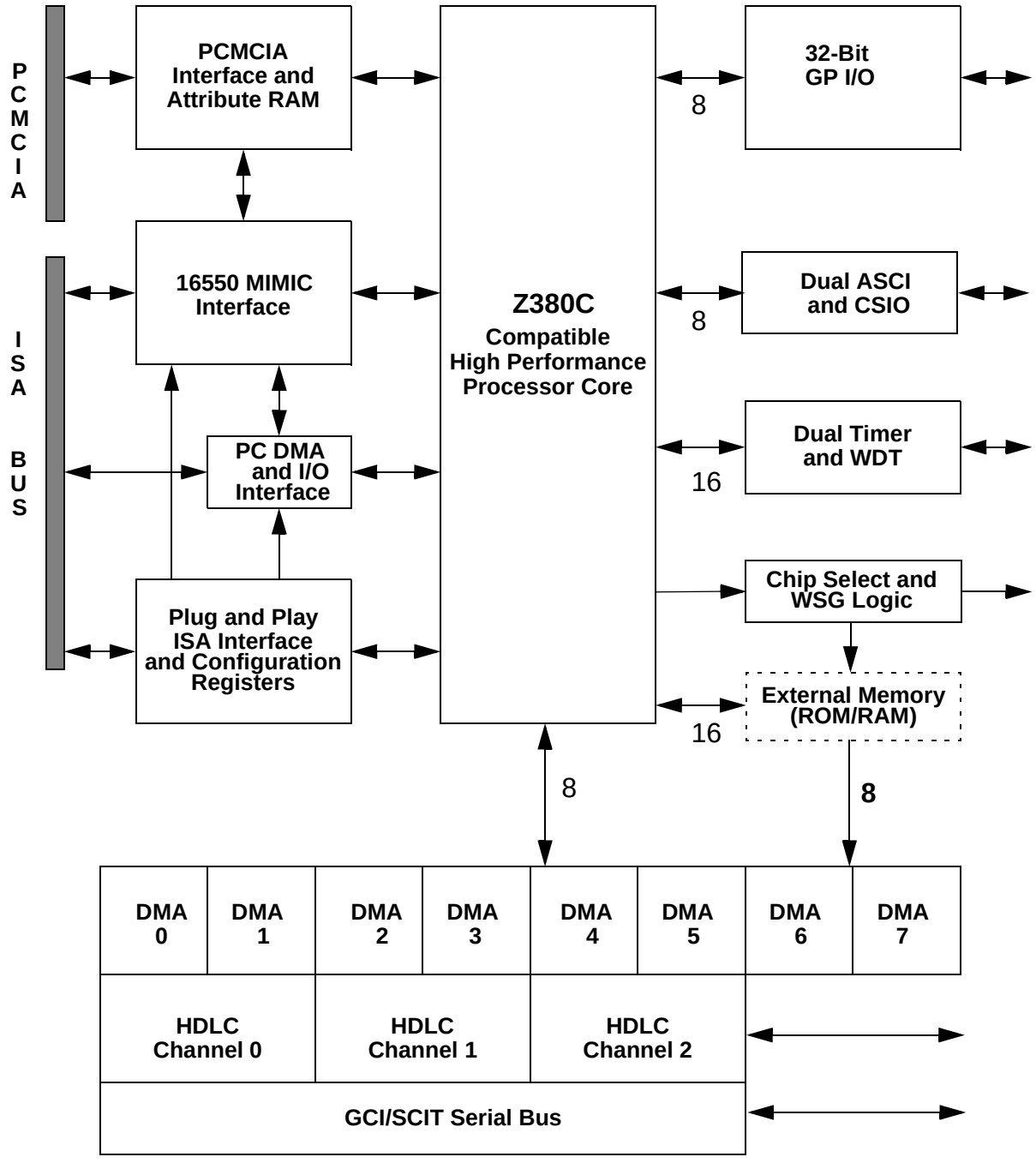


Figure 1. Z80382 Block Diagram

Host-PCMCIA Attribute Memory Write Timing (See Figure 6.)

Specifications apply over Standard Operating Conditions unless otherwise noted. C_L = 50 pF for outputs.

Table 7. Host-PCMCIA Attribute Memory Write Timing

		Z80382		Z8L382		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
t34	Address Setup to $\overline{\text{PCCE1}}$ Fall	30		35		ns
t35	Address Setup to $\overline{\text{PCWE}}$ Fall	30		35		ns
t36	Address Hold from $\overline{\text{PCCE1}}$ High	10		10		ns
t37	Address Hold from $\overline{\text{PCWE}}$ High	10		10		ns
t38	Data Setup to $\overline{\text{PCCE1}}$ Rise	20		20		ns
t39	Data Setup to $\overline{\text{PCWE}}$ Rise	20		20		ns
t40	Data Hold from $\overline{\text{PCCE1}}$ High	10		10		ns
t41	Data Hold from $\overline{\text{PCWE}}$ High	10		10		ns
Note: Timings also apply for writes to registers located in the attribute memory space.						

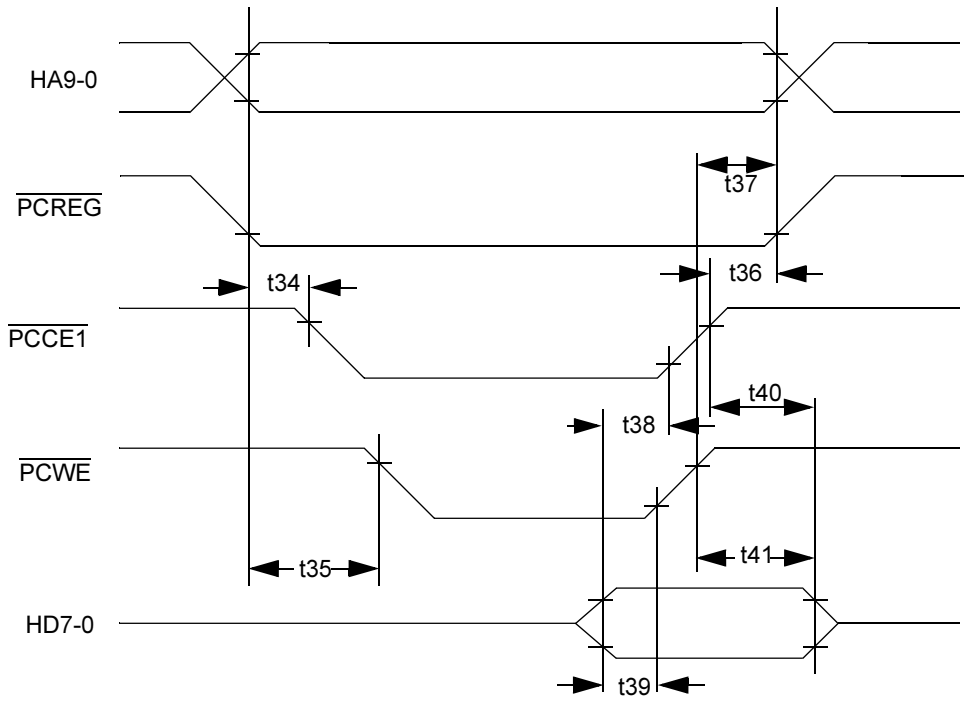


Figure 6. Host - PCMCIA Attribute Memory Write Timing Diagram

Timer Output Timing (See Figure 9)

Specifications apply over Standard Operating Conditions unless otherwise noted. C_L = 50 pF for outputs.

Table 10. Timer Output Timing

		Z80382		Z8L382		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t64	BUSCLK Low to TOUT Valid		20		20	ns

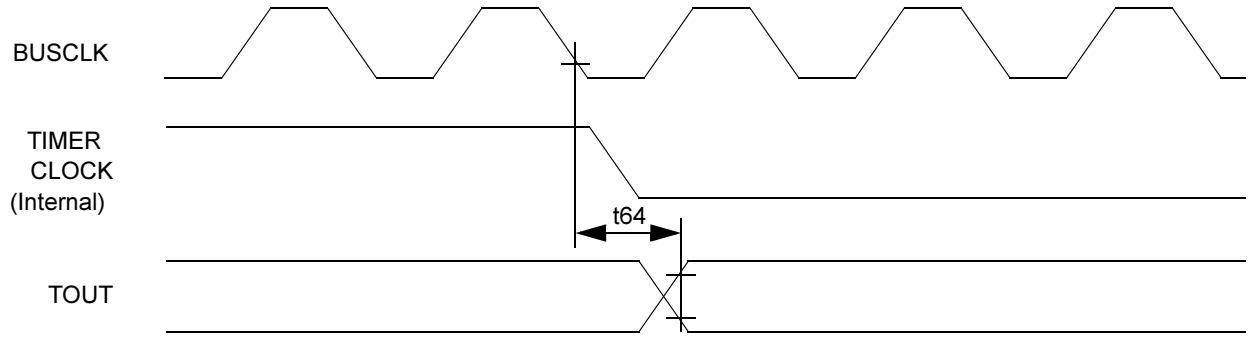


Figure 9. Timer Output Timing Diagram

HDLC Timing - Non-GCI TDM mode (See Figure 20)

Specifications apply over Standard Operating Conditions unless otherwise noted.
C_L = 50 pF for outputs

Table 18. HDLC Timing - Non-GCI TDM Mode

		Z80382		Z8L382		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t120	FSC Setup to BCL Fall	30		50		ns
t121	FSC Hold from BCL Low	20		30		ns
t122	BCL Period	50		50		ns
t123	BCL High Time	15		15		ns
t124	BCL Low Time	15		15		ns
t125	BCL High to $\overline{\text{TxEN}}$ Low		15		20	ns
t126	BCL High to $\overline{\text{TxEN}}$ High		15		20	ns
t127	BCL High to TxD Valid		15		20	ns
t128	BCL High to TxD Invalid	15		20		ns
t129	RxD Setup to BCL Fall (Rise)[1]	15		20		ns
t130	RxD Hold from BCL Low (High)[1]	5		5		ns

Note: 1. Receive clock sampling edge is configurable by means of RIRn[6]. See Z80382 User Manual.

extended to 32 bits by the z extension to the register to form three 32-bit general-purpose registers. The HL register serves as the 16-bit or 32-bit accumulator for word operations.

CPU Flag Register. The Flag register contains six flags that are set or reset by various CPU operations:

- Carry
- Add/Subtract
- Parity/Overflow
- Half Carry
- Zero
- Sign

Index Registers. The four Index registers, IX, IX', IY and IY', each hold a 32-bit base address that is used in the Indexed addressing mode. The Index registers can also function as general-purpose registers with the upper and lower bytes of the lower 16 bits accessed individually.

Interrupt Register. The Interrupt register (I) is used in interrupt modes 2 and 3 for INT0 to generate a 32-bit indirect address to an interrupt service routine. The I register supplies the upper 24 or 16 bits of the indirect address and the interrupting peripheral supplies the lower 8 or 16 bits. In the Assigned Vectors mode for INT1-3, the upper 16 bits of the vector are supplied by the I register; bits 15-9 are the assigned vector base and bits 8-0 are the assigned vector unique to each of INT1-3.

Program Counter. The Program Counter (PC) is used to sequence through instructions in the currently executing program and to generate relative addresses. The PC contains the 32-bit address of the current instruction being fetched from memory. In the NATIVE mode, the PC is effectively only 16 bits long, as carries from bit 15 to bit 16 are inhibited in this mode. In EXTENDED mode, the PC is allowed to increment across all 32 bits.

R Register. The R register can be used as a general-purpose 8-bit read/write register.

Stack Pointer. The Stack Pointer (SP) is used for saving information when an interrupt or trap occurs and for supporting subroutine calls and returns. Stack Pointer relative addressing allows parameter passing using the SP.

Select Register. The Select Register (SR) controls the register set selection and the operating modes of the 380C CPU.

source. If the transmitter FIFO is non-empty and no Host write or 380C read of the FIFO has taken place within the timer interval, a timeout occurs, causing a corresponding interrupt to the 380C.

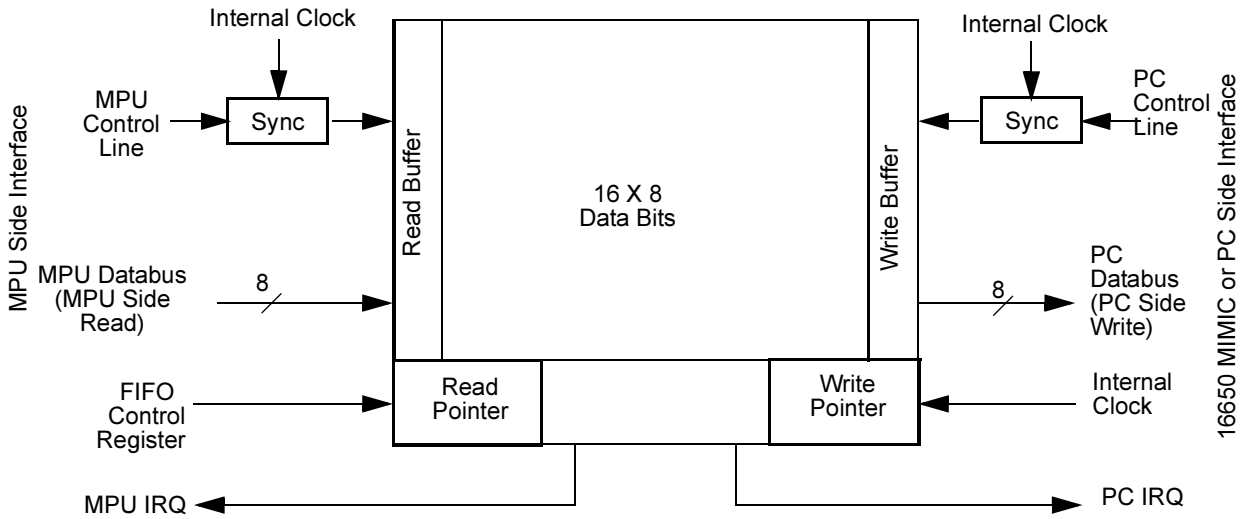


Figure 25. 16550 MIMIC Transmitter FIFO Block Diagram

Transmit And Receive Timers

Because of the speed at which data transfers can take place between the Z382 and the Host, there are two timers to alleviate any software problems that a high speed data transfer might cause. These timers allow the programmer to slow down the data transfer to simulate the MIMIC receiving and transmitting the data serially. The timers receive their input from the MIMIC BRG clock. This condition allows the programmer access to a 24-bit timer to slow the data transfers.

MIMIC Programming Registers

The MIMIC module contains a set of registers for programming various aspects of MIMIC operation. These are:

Table 28. MIMIC Programming Registers

Register	380C I/O Address
MIMIC Master Control Register	00FFH
MIMIC DMA Control Register	00EFH
MIMIC IUS/IP Register	00FEH
Interrupt Enable Register	00FDH

Table 28. MIMIC Programming Registers (Continued)

Interrupt Vector Register	00FCH
FIFO Status and Control Register	00ECH
Rx Timeout Time Constant Register	00EAH
Tx Timeout Time Constant Register	00EBH
Transmitter Time Constant Register	00FAH
Receiver Time Constant Register	00FBH

MIMIC-Host Interface Registers

In addition to the MIMIC programming registers, the Z382 contains a register set for interfacing with the Host by means of the MIMIC. These registers are used to emulate the 16550 UART so that the Host can access these registers in a manner similar to interfacing with the UART. This feature provides software compatibility with existing Host communication software. The registers are:

can be used on the other side. Thus, several modes of operation can be programmed:

- Host DMA Write, Z382 Polled Input
- Host DMA Read, Z382 Polled Output
- Host DMA Write with Z382 DMA
- Host DMA Read with Z382 DMA

On the ISA bus, the Z382 can use two independent DMA Mailbox facilities. When either of these facilities is enabled in the Plug and Play module, that module signals a DMA request by driving HDREQ0 or HDREQ1 High; if a facility is disabled, the corresponding HDREQ pin is 3-stated. A Low on one of the Acknowledge signals, HDACK0 or HDACK1, more or less simultaneously with HWR or HRD Low when the corresponding HDREQ line is being driven High, indicates a DMA cycle.

In a PCMCIA socket, only one DMA Mailbox can be used. When an option bit in one of the PCMCIA registers is 1, a DMA request is signalled by setting the INPACK output Low. A DMA cycle is signalled by having the PCREG line High while PCIORD or PCIOWR goes Low.

Plug-and-Play Interface

This module, with support from appropriate Z382-based firmware, complies with version 1.0a of the Microsoft™ /Intel™ “Plug-and-Play ISA” specification.

The Z382’s Plug-and-Play (PnP) module provides for I/O address decoding, interrupt channel selection and DMA channel selection. Pin limitations constrain the internal address decoding for I/O addresses to 12 bits. Because 16-bit decoding is preferred for full Plug-and-Play compliance, an additional input, HAEN, is provided which must be Low for a valid address decode. This input permits external decoding of HA15-12.

Figure 26 illustrates the Plug-and-Play Interface block diagram.

Centralized DMA Registers

Two registers listed below provide overall DMA subsystem control and status:

DMA Control Register	(DMACR)
DMA Vector Register	(DMAVR)

DMA Control Register (DMACR)

This register controls when bus control is returned to the 380C processor after a DMA channel has operated. It also provides modes whereby the Buffer Address and Buffer Length per-channel registers can be read and written.

DMA Vector Register (DMAVR)

This register contains the base interrupt vector for the DMA channels. It also identifies, during an interrupt acknowledge cycle, the interrupting DMA Channel.

Serial Communication Channels

The Z382 provides several means of serial data communications. These are the Asynchronous Serial Communication Interface (ASCI), the HDLC controllers, the GCI/SCIT interface and the Clocked Serial I/O Channel.

Asynchronous Serial Communications Interface (ASCI)

The Z382 provides two independently programmable ASCIs, each including a flexible baud rate generator. Key ASCI features include:

- Full-duplex operation
- Programmable data format
  - 7- or 8- data bits with optional ninth bit for multiprocessor communication
  - One or two stop bits
  - Odd, even or no parity
- Programmable baud rate generator
  - Divide-by-one, divide-by-16 and divide-by-64 modes
  - Up to three modem control signals per channel, depending on operating mode of the Z382
- Programmable interrupt conditions
- Four level data/status FIFOs for the receivers

Data transfers into the TDR can be performed using I/O instructions or by using one of the DMA channels. This DMA process loads characters into the TDR as an associated status bit indicates that it has become available for data.

Transmit Shift Register

When the ASCI Transmit Shift Register receives data from the ASCI Transmit Data Register, the data is shifted out to the TxA pin. When transmission is complete, the next byte (if available) is automatically loaded from the TDR into the TSR and the next transmission starts. If no data is available for transmission, the TSR idles at a continuous High level.

Receive Shift Register

When the receiver is enabled, the RXA pin is monitored for a Low. One-half bit time after a Low is sensed at RXA, the ASCI samples RXA again. If RXA has returned to High, the ASCI ignores the previous Low and resumes looking for a new one. If RXA is still Low, the ASCI considers this bit a start bit and proceeds to clock in the data based upon the internal baud rate generator or the external clock at the CKA pin. The number of data bits, parity, multiprocessor and stop bits are selected by means of control bits in the CNTLA and CNTLB registers.

After the data is received, the appropriate MP, parity and one stop bit are checked. If there is an empty position available data and any errors are clocked into the receive data and status FIFOs during the stop bit. Interrupts, Receive Data Register Full Flag, and DMA requests also go active during this time. If there is no space in the FIFO at the time that the RSR attempts to transfer the received data into it, an overrun error occurs.

Receive Data FIFO

When a complete incoming data byte is assembled in the RSR, it is automatically transferred to the FIFO, which serves to reduce the incidence of overrun errors. The top (oldest) character in the FIFO (if any) can be read by means of the Receive Data Register (RDR).

An overrun occurs if the receive FIFO is still full when the receiver completes assembly of a character and is ready to transfer it to the FIFO. If this occurs, the overrun error bit associated with the previous byte in the FIFO is set. The latest data byte is not transferred from the shift register to the FIFO in this case, and is lost. After an overrun occurs, the receiver does not place any further data in the FIFO until the last good byte received has come to the top of the FIFO and sets the Overrun latch. Software then clears the Overrun latch.

When a break occurs (defined as a framing error with the data equal to all zeros), the all-zero byte with its associated error bits are transferred to the FIFO if it is not full. If the FIFO is full, an overrun is generated, but the break, framing error and

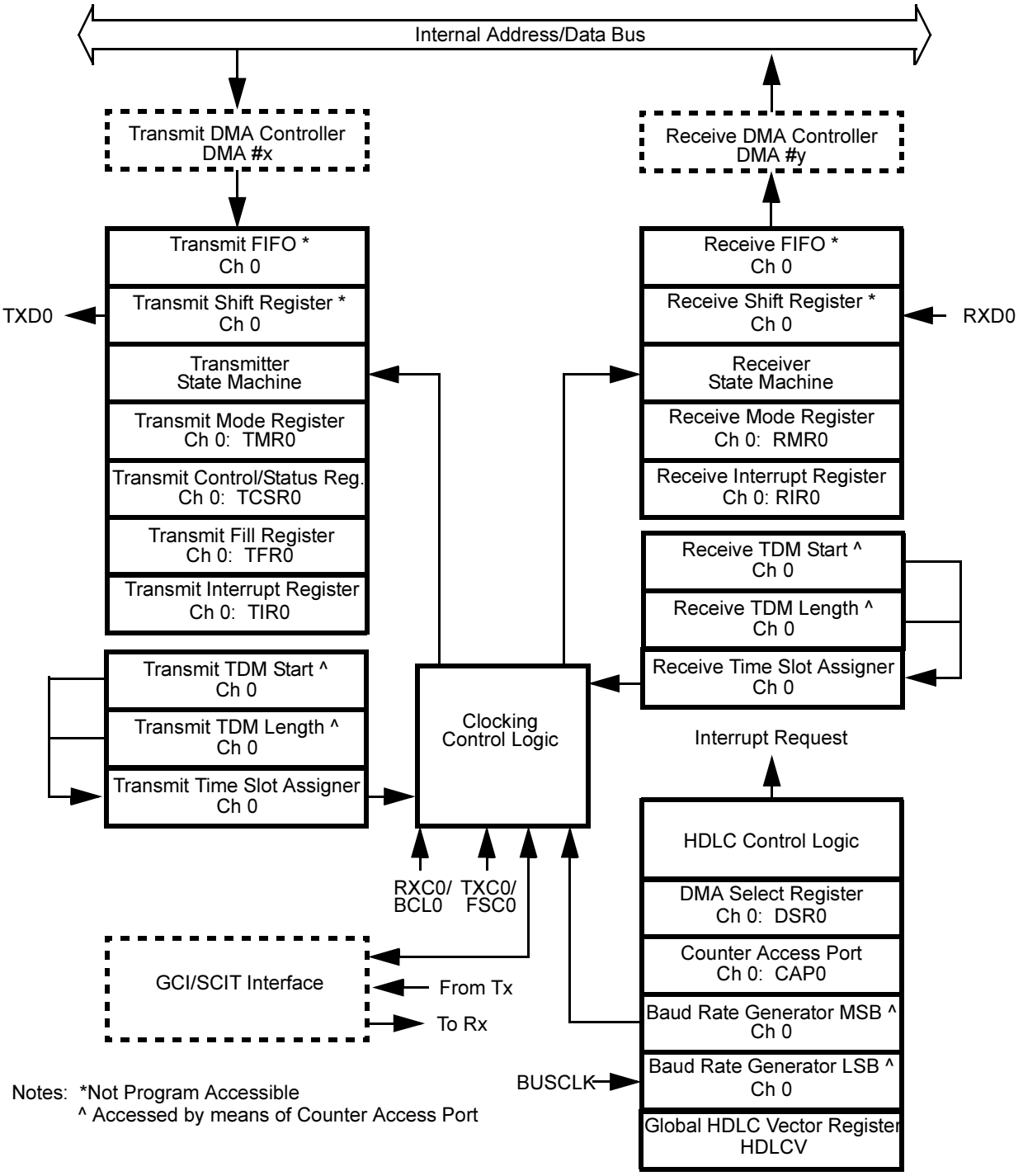


Figure 31. HDLC Channel Block Diagram (One of Three Channels Illustrated)

Transmit Interrupt Register. This register controls and provides status of potential interrupting conditions in the transmitter. The mechanism is also provided for clearing conditions which are causing an interrupt.

Transmit Fill Register. This register holds a character that can be sent between frames in HDLC mode, or in case of an Underrun, in TRANSPARENT mode.

Receive Mode Register. This register selects the main operating mode of the Receiver (TRANSPARENT, HDLC, NRZI HDLC), its I/O configuration (TDM, I/O by means of device pins, and so on), when DMA data transfers are requested, when the receiver begins assembling characters, when it is switched from the Inactive state to TRANSPARENT mode, and the type of CRC used in HDLC modes.

Receive Interrupt Register. This register handles incoming interrupts. Most of the interrupt requirements for HDLC reception can be handled by enabling Status interrupts in the DMA channel associated with each Receiver. The only Receiver interrupt condition that is not handled by this means is the Idle condition. Idle interrupts are controlled by this register. This register also allows several commands which deal with interrupts and HUNT mode to be issued to the receiver.

DMA Select Register. This register selects the DMA channels to be used by the receiver and transmitter and enables their operation.

Counter Access Port. This port allows the 380C to write and read the starting values for various counters in the HDLC channel. These counters are the Baud Rate Generator time constant, the Transmitter TDM start and length values, and the Receiver TDM start and length values.

Global HDLC Vector Register. This register provides the base interrupt vector for the HDLC channels and identifies the HDLC device which is causing an interrupt to be issued.

GCI/SCIT Interface

GCI/SCIT Frame Structure (Terminal Mode)

GCI/SCIT includes three sub-frames called channels 0, 1, and 2, each containing 32 bits. This 12-byte frame is repeated at a rate of 8 KHz, giving an aggregate data rate of 768 Kbps. Figure 32 depicts the frame structure.

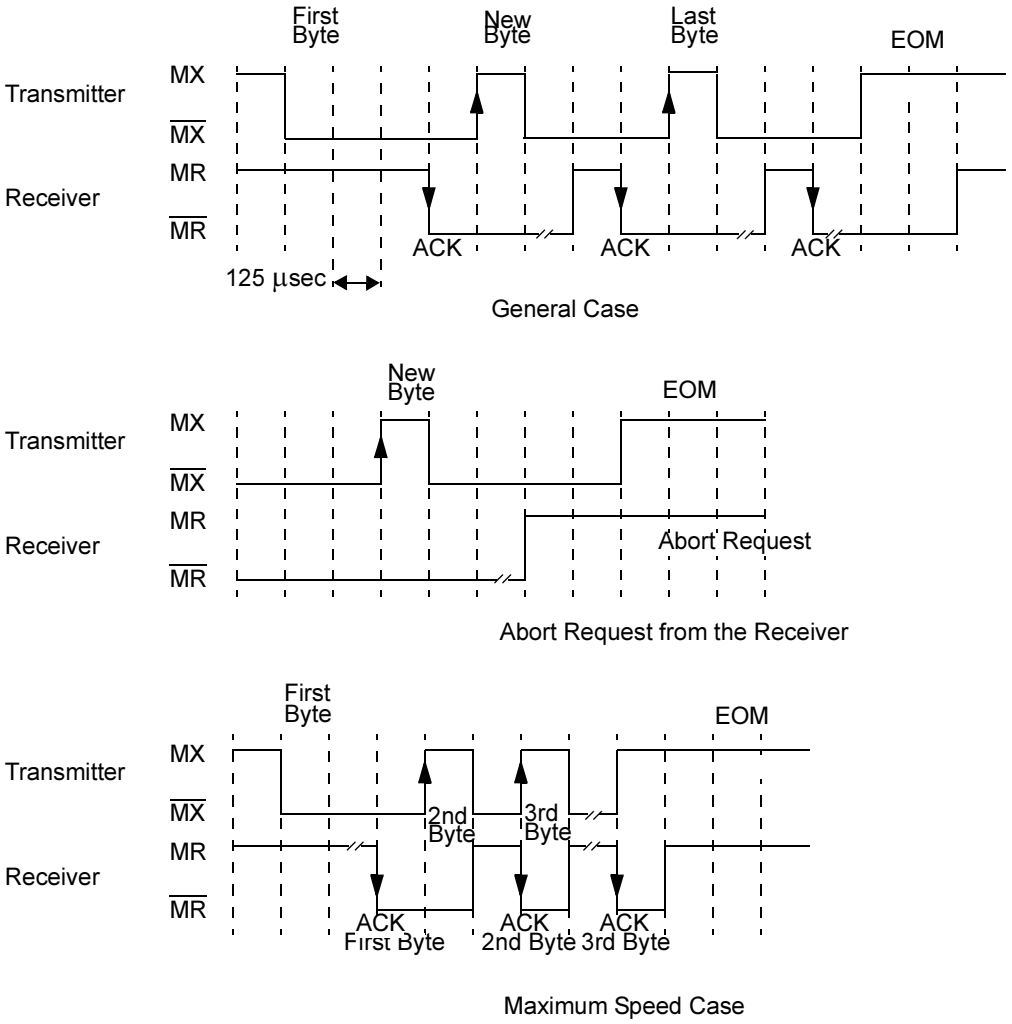


Figure 33. Monitor Handshake Timing Diagram

C/I Channel Operation

Data on C/I0 and C/I1 is transmitted continuously in each frame until new data is to be sent. A change in C/I channel data is considered valid if it has been received in two consecutive frames.

GCI/SCIT Bus Activation and Deactivation

Deactivation, Upstream to Downstream. The upstream (clock master) unit initiates deactivation by issuing a series of software handshakes by means of the C/I0 channel. The upstream unit waits for a deactivation indication from all down-

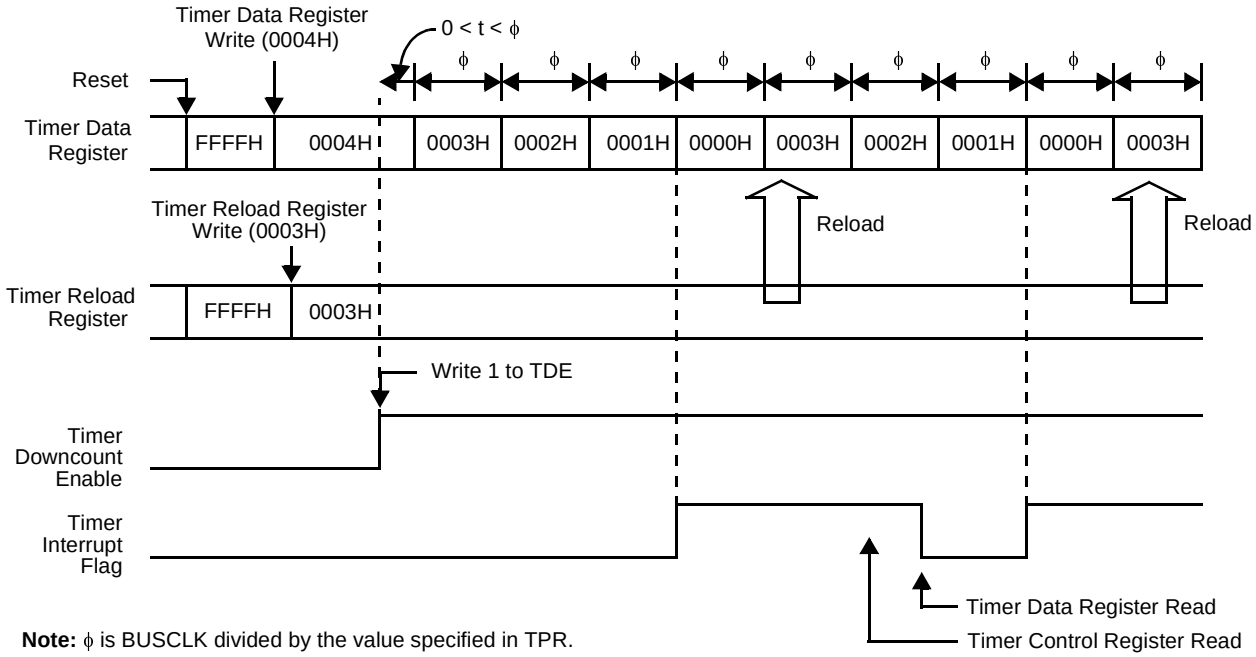
PRT Per-Channel Registers

The I/O-mapped per-channel registers in each PRT are:

- Timer Data Registers High/Low
- Timer Reload Registers High/Low

Timer Data Registers. Each PRT has a 16-bit Timer Data Register (TMDR). TMDR is decremented once every clock output from the timer prescaler, which divides the BUSCLK signal of the Z382 by a value which is specified, independently for PRT1 and PRT0, in the TPR. When TMDR counts down to 0, it is automatically reloaded with the value contained in its Timer Reload Register (RLDR).

Timer Reload Registers. Each PRT has a 16-bit Timer Reload Register (RLDR) When a PRT channel's TMDR counts down to 0, it is automatically reloaded with the contents of its RLDR. Figure 36 illustrates the operation of the PRT.



Note: ϕ is BUSCLK divided by the value specified in TPR.

Figure 36. PRT Operation Timing Diagram

Watch-Dog Timer

A Watch-Dog Timer (WDT) with programmable timeout intervals prevents code runaway and possible resulting system damage. The $\overline{\text{RESET}}$ input can be forced as an output upon the terminal count of the WDT, allowing external peripherals to be reset along with the Z382. Unlike other on-chip functions, the WDT is enabled

Peripheral Function Control Registers

The functions described previously are controlled by a number of I/O mapped on-chip registers:

- Clock Control Register
- I/O Waits Register
- Refresh Registers 0, 1 and 2
- Refresh Wait Register
- Standby Mode Control Register

Clock Control Register. This register controls how BUSCLK is derived from the input clock (CLKI, CLKI/2 or CLKI x 2), provides a means of disabling CLKO to save power and reduce noise if an external clock is used, and controls the I/O Clock Rate (BUSCLK/8 to BUSCLK).

I/O Waits Register. This register allows for up to seven wait states to be inserted in external I/O read and write transactions, and at the latter portions of interrupt transactions to capture interrupt vectors. Also allows for up to seven wait states to be inserted at the early portions of interrupt acknowledge transactions, for the interrupt daisy chain through on-chip and possibly external I/O devices to settle.

Refresh Register 0. This register defines the interval between refresh requests to the Z382's External Interface Logic.

Refresh Register 1. This register provides the Missed Requests Count. This count increments by one when a refresh request is made and decrements by one when the Z382's External Interface Logic completes each burst of refresh transactions. A user can read the count status, and if necessary, take corrective actions such as adjusting the burst size.

Refresh Register 2. This register enables the refresh function and defines the number of refresh transactions per refresh request made to the Z382's External Interface Logic.

Refresh Wait Register. This register defines the number of T1, T2 and T3 wait states to be inserted in refresh transactions.

STANDBY Mode Control Register. This register enables the Z382 to go into low-power STANDBY mode when the Sleep instruction is executed, allows asserting BREQ to exit the mode, and specifies the approximate running duration of a warm-up counter that provides a delay before the Z382 resumes its clocking and operations, from the time an interrupt or bus request (if so enabled) is asserted to exit STANDBY mode.

D

E

F

G