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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z380C |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 10MHz |
| Co-Processors/DSP | - |
| RAM Controllers | - |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 3.3V |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Security Features | - |
| Package / Case | 144-QFP |
| Supplier Device Package | 144-QFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8l38210fsc |

**Table 1. Pin Numbers and Input/Output Classifications (Continued)**

| Pin | Input Class[1] | Output Class[1] | Pin Number(s) |
|---|---|---|---|
| IOCLK | I | O | 114 |
| PA7-0/HD7-0 | I | H | 78 -85 |
| PB0/CKS | I | 3 | 58 |
| PB1/RXS | i | 3 | 57 |
| PB2/TXS | I | 3 | 56 |
| PB3/RXA1 | I | 3 | 55 |
| PB4/TXA1 | I | 3 | 54 |
| PB5/CKA0 | I | 3 | 53 |
| PB6/RXA0 | I | 3 | 52 |
| PB7/TXA0 | I | 3 | 51 |
| PC2/$\overline{\text{TXEN2}}$/TOUT | I | 3 | 109 |
| PC3/CKA1 | I | 3 | 49 |
| PC4/IEO | I | 3 | 48 |
| PC5/IEI | I | 3 | 47 |
| PC6/$\overline{\text{IOCS1}}$ | I | 3 | 45 |
| PC7/$\overline{\text{RAMCSH}}$ | I | 3 | 44 |
| PD7-0/HA7-0 | I | 3 | 69 - 76 |
| RXA0/$\overline{\text{HDAK1}}$/$\overline{\text{PCOE}}$ | I | D | 90 |
| RXA1/HA8 | I | 3 | 67 |
| RXC1-0/BCL1-0/PC1-0 | I | 3 | 101, 97 |
| RXD1-0/RXA1-0 | I | O | 103, 99 |
| RXS/HAEN/$\overline{\text{PCREG}}$ | I | D | 63 |
| TOUT/$\overline{\text{IOCS2}}$ | | 3 | 46 |
| TXA0/HDRQ0/$\overline{\text{PCCE1}}$ | I | H | 91 |
| TXA1/HINT1/$\overline{\text{PCIRQ}}$ | | H | 87 |
| TXC1-0/FSC1-0/CKA1-0 | I | 3 | 100, 96 |
| TXD1-0/TXA1-0 | | O | 102, 98 |
| TXS/$\overline{\text{HDOEN}}$/$\overline{\text{INPACK}}$ | | O | 62 |

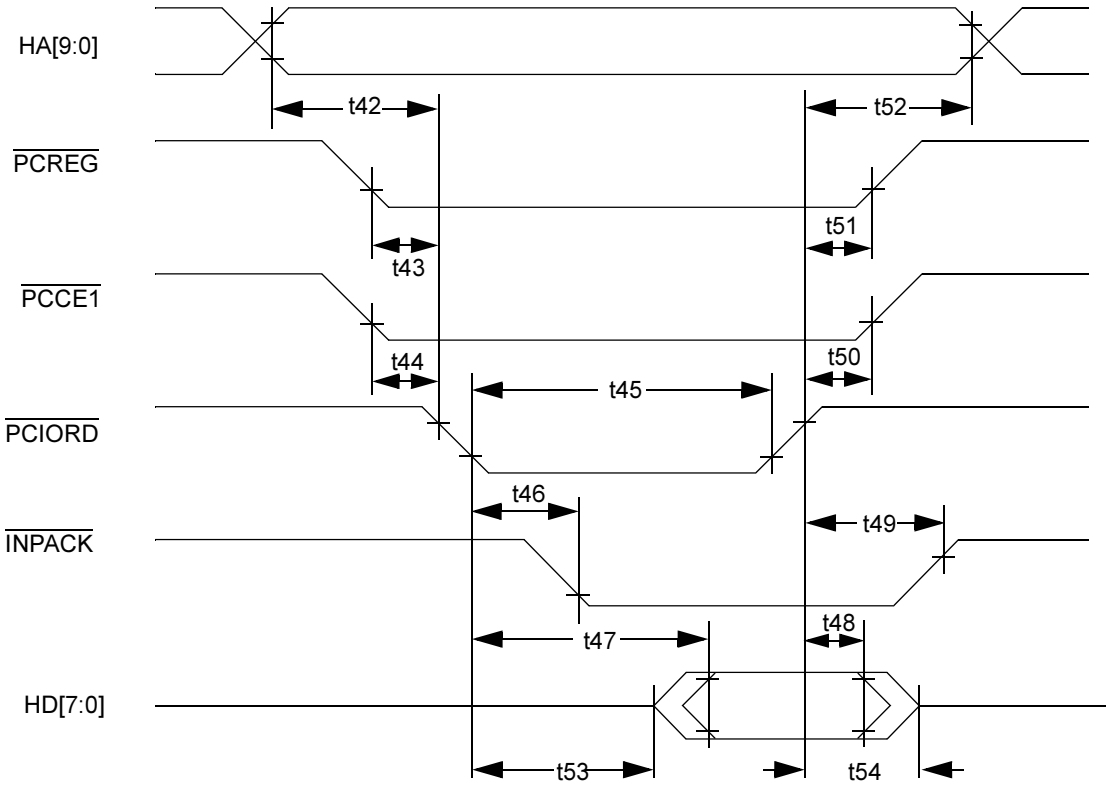



**Figure 7. Host - PCMCIA I/O Read Timing Diagram**

## HDLC Transmit Timing- Full Time HDLC Mode (See Figure 19)

**Table 17. HDLC Transmit Timing**

| | | Z80382 | | Z8L382 | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| t113 | External Transmit Clock Period[1] | 50 | | 50 | | ns |
| t114 | External Transmit Clock High Time | 15 | | 15 | | ns |
| t115 | External Transmit Clock Low Time | 15 | | 15 | | ns |
| t116 | External Transmit Clock Fall Time | | 5 | | 10 | ns |
| t117 | External Transmit Clock Rise Time | | 5 | | 10 | ns |
| t118 | TxC Low to TxD Data Valid | | 20 | | 25 | ns |

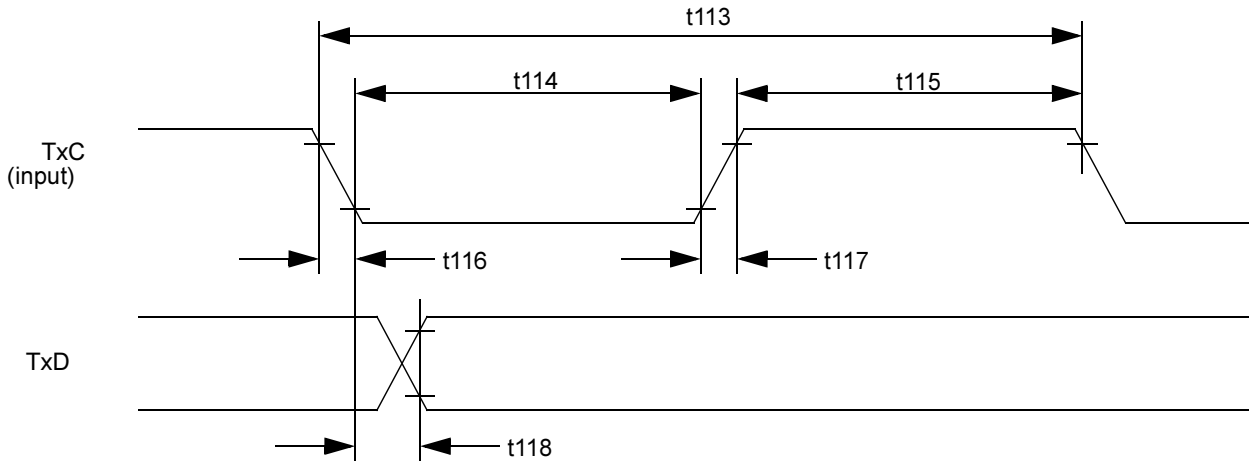



**Figure 19. HDLC Transmit Timing Diagram (Full Time HDLC)**

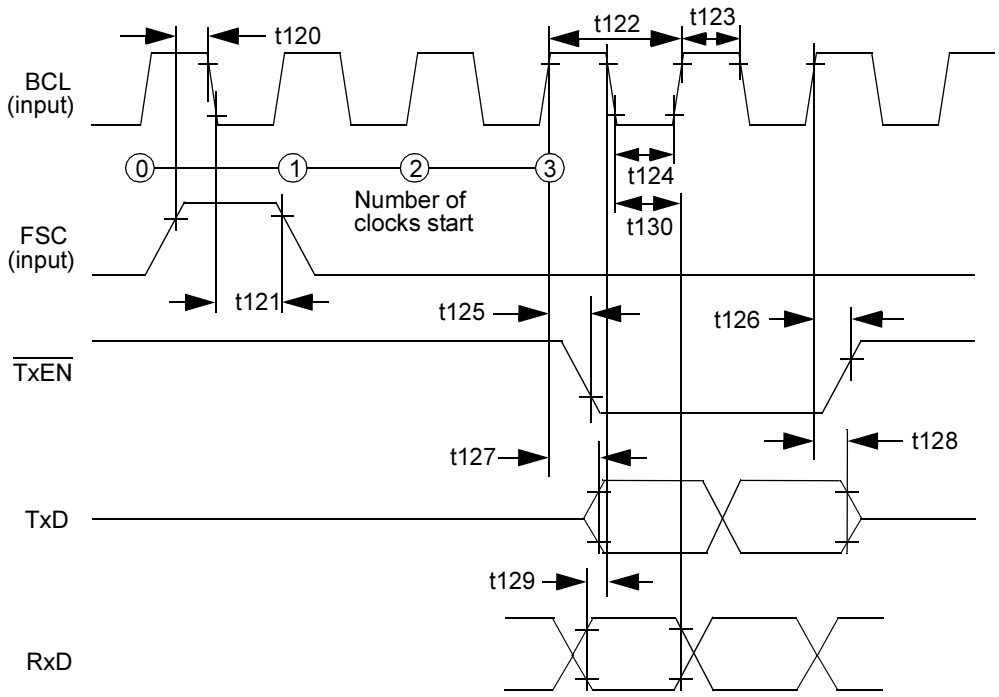



**Figure 20. HDLC Timing Diagram - Non-GCI TDM Mode (for Start = 3, Length = 2, Negative Edge RxD Sampling**

### GCI/SCIT Timing-Slave Characteristics (See Figure 21)

Specifications apply over Standard Operating Conditions unless otherwise noted. $C_L$ = 50 pF for outputs.

**Table 19. GCI/SCIT Timing - Slave Characteristics**

| | | Z80382 | | Z8L382 | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| t131 | DCL Data Clock Rise/Fall Time | | 5 | | 10 | ns |
| t132 | DCL Clock Period | 50 | | 50 | | ns |
| t133 | DCL Pulse Width High | 15 | | 15 | | ns |
| t134 | FSC Setup to DCL Fall | 30 | | 30 | | ns |
| t135 | FSC Hold from DCL Low | 5 | | 10 | | ns |
| t136 | DCL High to DU/DD Transmit Data Valid | | 15 | | 20 | ns |

### CPU Control Register Space

The CPU control register space consists of the 32-bit Select Register (SR). The contents of SR determine the CPU operating mode, which register bank is used, the interrupt mode in effect, and other items of this type.

### Memory Address Space

The actual usable memory space in the Z382 is 16 MB, because the lower 24 bits of the address are output on the external address bus. The 8-bit byte is the basic addressable element in the 380C memory address space. However, there are other addressable data elements; bits, 2-byte words, byte strings, and 4-byte words. The size of the data element being addressed depends on the instruction being executed as well as the WORD/LONG WORD mode.

When a word is stored in memory, the least significant byte precedes the more significant byte of the word, as in the Z80 CPU architecture. Also, the lower-addressed byte is present on the upper byte of the external data bus.

### On-Chip and External I/O Address Space

The 380C CPU architecture distinguishes between the memory and I/O spaces and, therefore, requires specific I/O instructions. I/O instructions are used to access the Z382's internal peripherals as well as a number of control registers which deal with functions such as interrupts and traps. I/O instructions are also used to access external peripheral controllers connected to the Z382's external address, data and control busses.

## Data Types

The Z380 CPU can operate on bits, Binary-Coded Decimal (BCD) digits (4 bits), bytes (8 bits), words (16 bits or 32 bits), byte strings, and word strings. Bits in registers can be set, cleared, and tested. BCD digits, packed two to a byte, can be manipulated with the Decimal Adjust Accumulator instruction (in conjunction with binary addition and subtraction) and the Rotate Digit instructions. Bytes are operated on by 8-bit load, arithmetic, logical, and shift and rotate instructions. Words are operated on in a similar manner by the word load, arithmetic, logical, and shift and rotate instructions. Block move and search operations can manipulate byte strings and word strings up to 64 KB or words long. Block I/O instructions have identical capabilities.

## Addressing Modes

Addressing modes are used by the 380C to calculate the effective address of an operand needed for execution of an instruction. Seven addressing modes are supported by the CPU. Of these seven, one is an addition to the Z80 CPU

addressing modes (Stack Pointer Relative) and the remaining six modes are either existing or extensions to the Z80 CPU addressing modes.

### Register Addressing

The operand is one of the 8-bit registers (A, B, C, D, E, H, L, IXU, IXL, IYU, IYL, A', B', C', D', E', H' or L'); or is one of the 16-bit or 32-bit registers (BC, DE, HL, IX, IY, BC', DE', HL', IX', IY' or SP) or one of the special registers (I or R).

### Immediate Addressing

The operand is in the instruction itself and has no effective address. The DDIR IB and DDIR IW decoder directives allow specification of 24-bit and 32-bit immediate operands, respectively.

### Indirect Register Addressing

The contents of a register specify the effective address of an operand. The HL register is the primary register used for memory accesses, but BC and DE can also be used. (For the JP instruction, IX and IY can also be used for indirection.) The BC register is used for I/O space accesses.

### Direct Addressing

The effective address of the operand is the location whose address is contained in the instruction. Depending on the instruction, the operand is either in the I/O or memory address space. Sixteen bits of direct address is the norm, but the Decoder Directive Immediate Byte (DDIR IB) and Decoder Directive Immediate Word (DDIR IW) allow 24-bit and 32-bit direct addresses, respectively.

### Indexed Addressing

The effective address of the operand is the location computed by adding the two's-complement signed displacement contained in the instruction to the contents of the IX or IY register. Eight bits of index is the norm, but the DDIR IB and DDIR IW decoder directives allow 16-bit and 24-bit indexes, respectively.

### Program Counter Relative Addressing

An 8-, 16- or 24-bit displacement contained in the instruction is added to the Program Counter to generate the effective address. This mode is available only for Jump and Call instructions.

### Stack Pointer Relative Addressing

The effective address of the operand is the location computed by adding the two's-complement signed displacement contained in the instruction to the con-

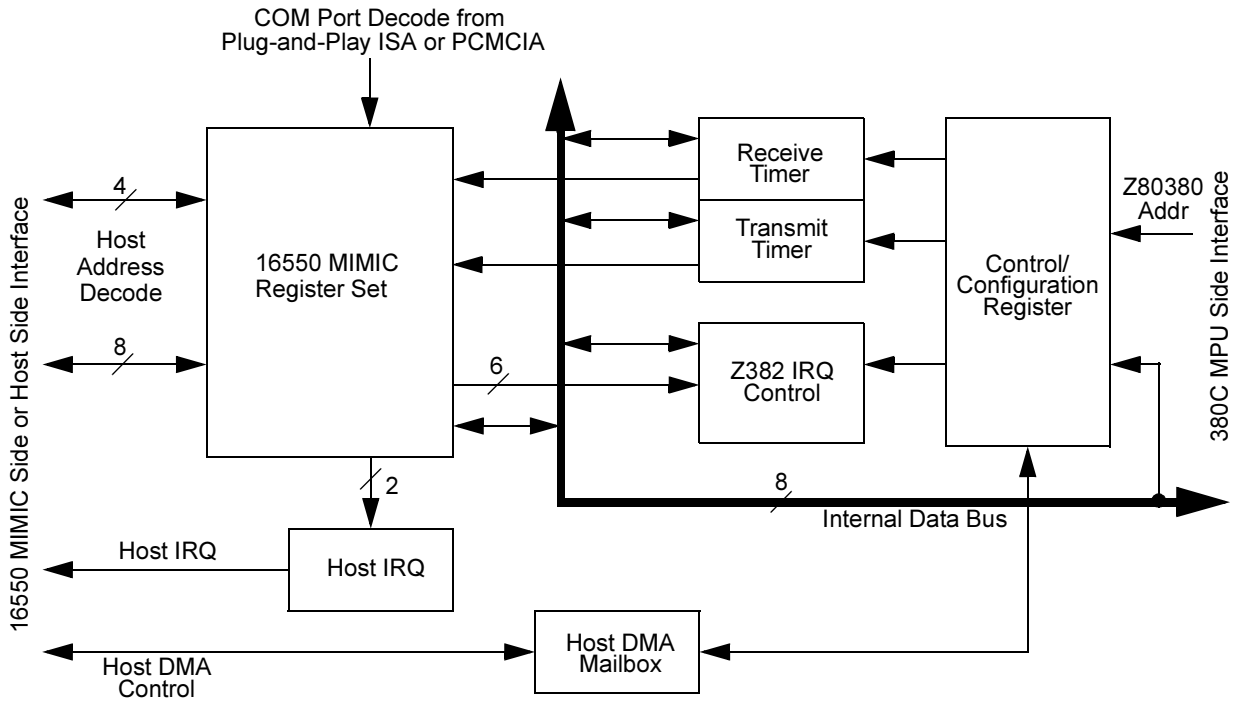



**Figure 23. 16550 MIMIC Block Diagram**

### MIMIC Receiver FIFO

The receiver FIFO is 16-words deep and stores eight data bits and three error bits (Parity error, Framing error and Break detect) for each character received. The data and error bits move together in the FIFO. The error bits become available to the Host side of the interface when that particular location becomes the next address to read (top of FIFO). At that time these bits may either be read by the Host or they may cause an interrupt to the Host interface if so enabled. The error bits are set by the error status of the byte at the top of the FIFO but may only be cleared by reading the Line Status Register (LSR). If successive reads of the receiver FIFO are performed without reading the LSR, the status bits are set if any of the bytes read have the respective error bit set.

The Host interface may be interrupted when 1, 4, 8 or 14 bytes are available in the receiver FIFO. If the FIFO is not empty, but below the programmed trigger value, a timeout interrupt is available if the receiver FIFO is not written by the 380C or read by the Host by an interval determined by the Character Timeout Timer. This timer is an additional timer with 380C access-only which is used to emulate the 16550 four-character timeout delay. The timer receives the BRG as its input clock. Software determines the correct values to program into the Receiver Timeout Register

source. If the transmitter FIFO is non-empty and no Host write or 380C read of the FIFO has taken place within the timer interval, a timeout occurs, causing a corresponding interrupt to the 380C.

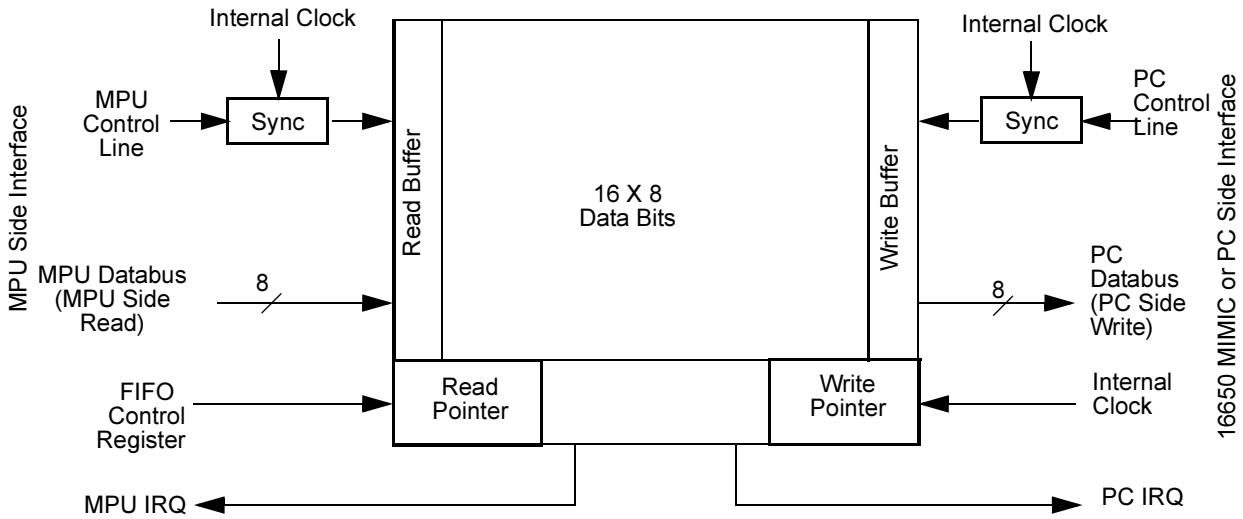



**Figure 25. 16550 MIMIC Transmitter FIFO Block Diagram**

### Transmit And Receive Timers

Because of the speed at which data transfers can take place between the Z382 and the Host, there are two timers to alleviate any software problems that a high speed data transfer might cause. These timers allow the programmer to slow down the data transfer to simulate the MIMIC receiving and transmitting the data serially. The timers receive their input from the MIMIC BRG clock. This condition allows the programmer access to a 24-bit timer to slow the data transfers.

### MIMIC Programming Registers

The MIMIC module contains a set of registers for programming various aspects of MIMIC operation. These are:

**Table 28. MIMIC Programming Registers**

| Register | 380C I/O Address |
|---|---|
| MIMIC Master Control Register | 00FFH |
| MIMIC DMA Control Register | 00EFH |
| MIMIC IUS/IP Register | 00FEH |
| Interrupt Enable Register | 00FDH |

**Table 28. MIMIC Programming Registers (Continued)**

| | |
|---|---|
| Interrupt Vector Register | 00FCH |
| FIFO Status and Control Register | 00ECH |
| Rx Timeout Time Constant Register | 00EAH |
| Tx Timeout Time Constant Register | 00EBH |
| Transmitter Time Constant Register | 00FAH |
| Receiver Time Constant Register | 00FBH |

### MIMIC-Host Interface Registers

In addition to the MIMIC programming registers, the Z382 contains a register set for interfacing with the Host by means of the MIMIC. These registers are used to emulate the 16550 UART so that the Host can access these registers in a manner similar to interfacing with the UART. This feature provides software compatibility with existing Host communication software. The registers are:

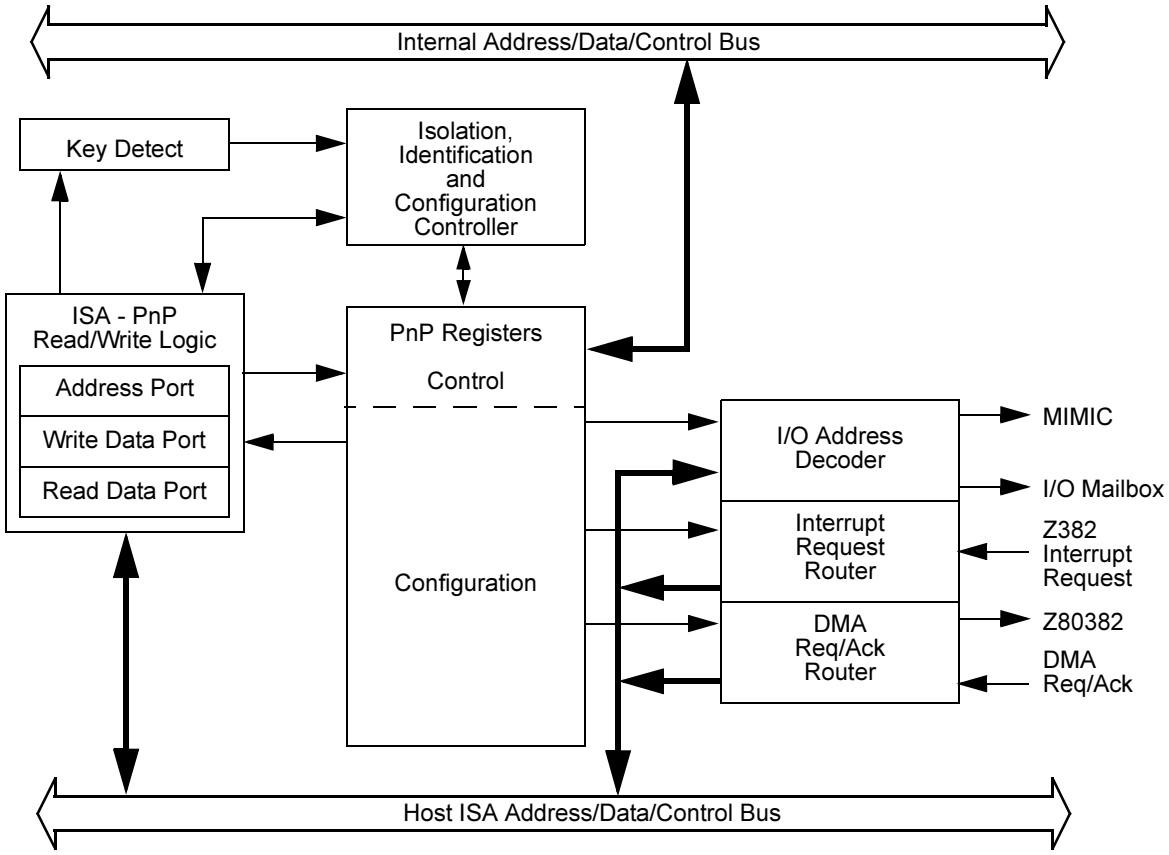



**Figure 26. Plug-and-Play Interface Block Diagram**

### ISA Port

The PnP interface implements three 8-bit ports on the ISA bus. The Address port is a write-only port at the fixed address 0279H. The Write Data port is a write-only port at the fixed address 0A79H. The Read Data port is a read-only port at a programmable address among 0203H, 0207H, 020BH, ..., 03FFH.

The Host may write to the Address port for three reasons:

1. As part of sending an *Initiation key* to all the PnP cards in the system.
2. To select a register on one or all PnP cards as the destination of a subsequent write to the Write Data port.
3. To select a register on one card, or the *Isolation* facility on multiple cards, as the source of data in a subsequent read from the Read Data port.

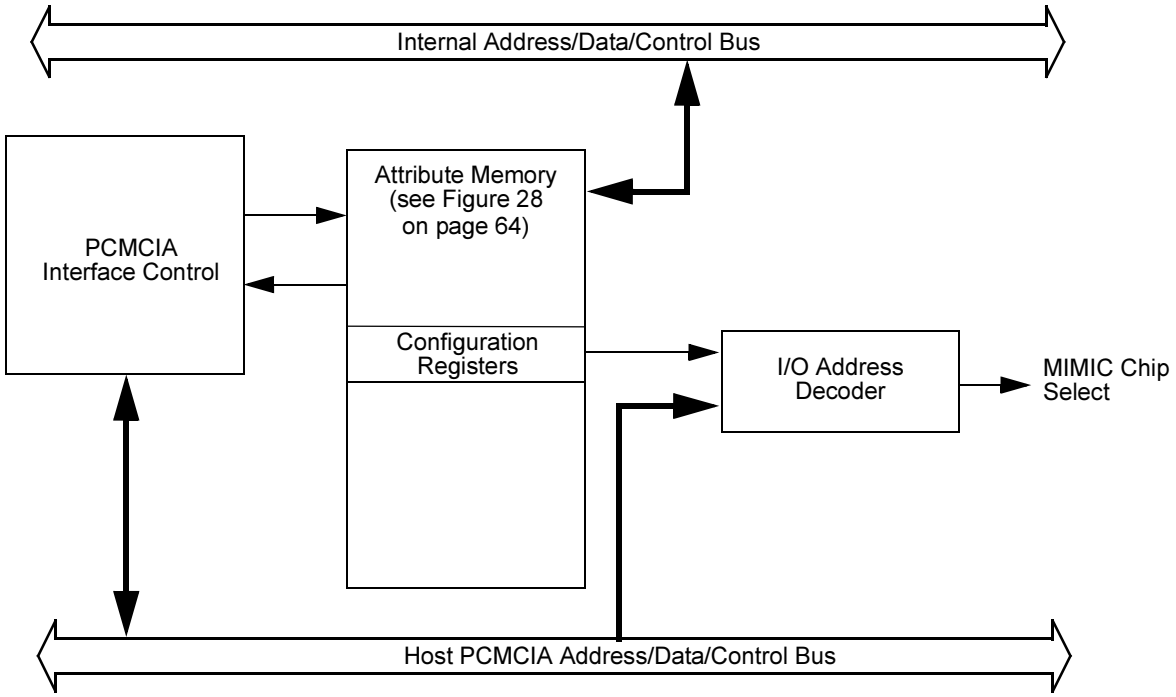



**Figure 27. PCMCIA Interface Block Diagram**

### PCMCIA I/O Interface Control

The I/O interface contains the main functionality of the PCMCIA block. The interface decodes addesses for I/O accesses by the Host according to the PCMCIA standard. The Host writes to the Configuration Option Register an index to select the base address of the desired I/O address range. After configuration, I/O accesses to this address range are recognized, and the MIMIC chip select is asserted when a valid I/O access is performed and the address is in the configured address range.

### Attribute Memory

The attribute memory is the primary mechanism for transfers of configuration data and status between the host system and the PCMCIA card. As depicted in Figure 28, the attribute memory is segmented into several sections. The Card Information section is 240 bytes of RAM which is loaded by the 380C with information describing the card and its resource requirements, data needed by the Host to configure the card. A portion of the attribute memory allows the host to access the I/O Mailbox registers. Lastly, sections in the attribute memory space are assigned to the Configuration Registers and the Base Address Registers.

## Per-Channel Registers

There are eight DMA channels in the Z382. Each channel includes the following registers:

**Table 32. Per-Channel Registers**

| | |
|---|---|
| List Address Register | (LAR, 21 bits) |
| Buffer Address Register | (BAR, 24 bits) |
| Buffer Length Register | (BLR, 16 bits) |
| DMA Control/Status Register | (DCSR, 8 bits) |

The LAR and DCSR are read/write registers. Software tracks the progress of a DMA by monitoring its LAR. BARs and BLRs are accessible only by using special modes selected in the centralized DMA Control Register. The DMA channel stores ending BLR values in the list.

### List Address Register

A three-byte register whose 21 most significant bits contain the base address of the current list. The DMA channel begins operation when the 380C writes the most significant byte of this register. The DMA controller updates this register as it processes new lists in response to links from previous lists. The three LS bits of the LAR are ignored on writing, and are read back as 100 (pointing at the current Type/Status byte in the list).

### Buffer Address Register

The DMA controller loads the initial value of the current buffer address into this register from the address field of the current list. At the end of each data transfer, the DMA channel increments the BAR by one.

### Buffer Length Register

The DMA controller loads the initial value of the current buffer length into this register from the buffer length field of the current list. At the end of each data transfer, the DMA channel decrements the BLR by one.

### DMA Control/Status Register

Controls items such as I/O Direction, enabling/disabling BURST Mode, and enabling and disabling interrupts. Also provides certain per channel DMA and interrupt status conditions.

- Receive parity, framing and overrun error detection
- Optional operation with on-chip DMA controllers

Figure 30 illustrates the major functional blocks within the ASCI.

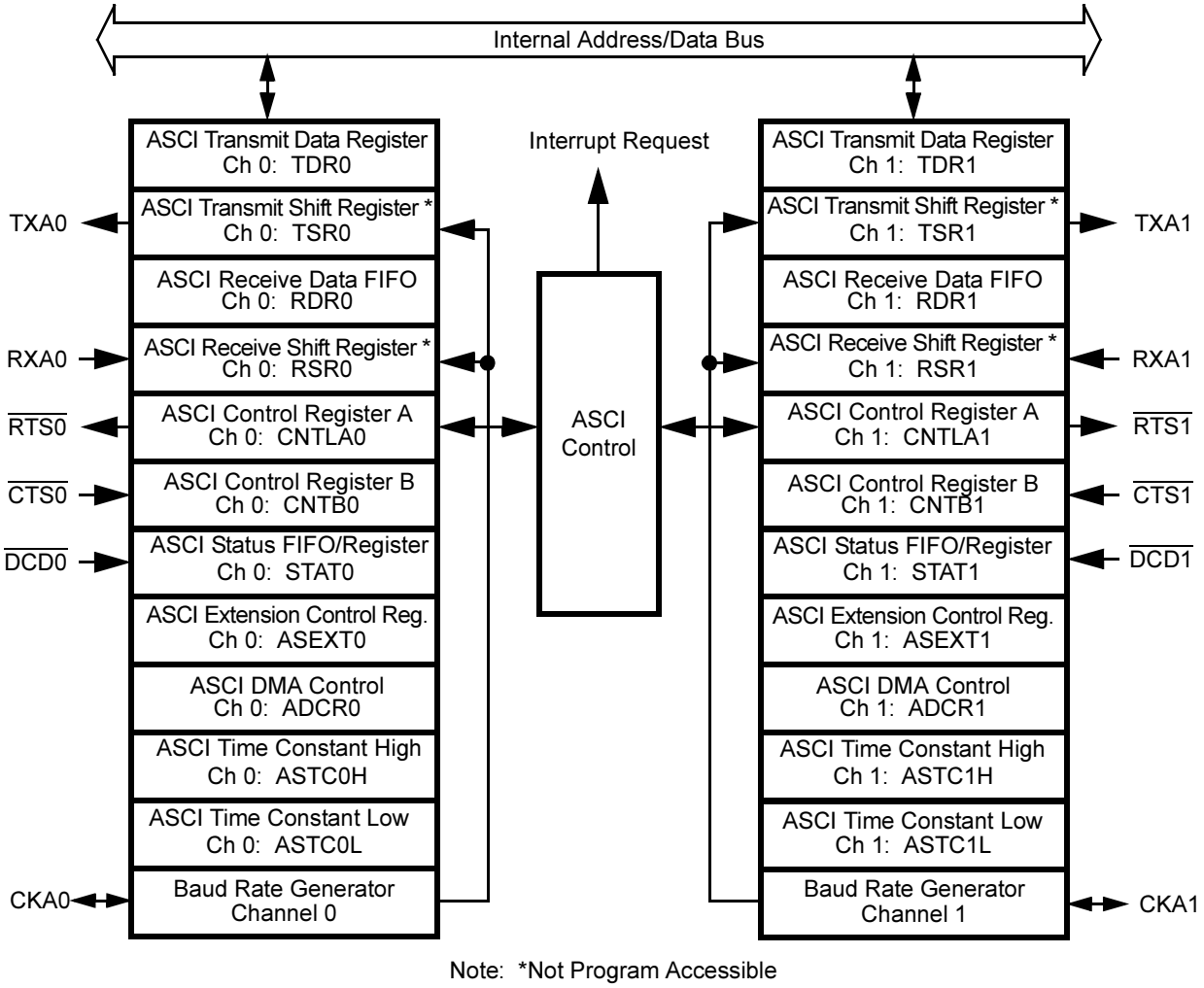



**Figure 30. Asynchronous Serial Communications Interface (ASCI) Block Diagram**

### Transmit Data Register

Data written to the ASCI Transmit Data Register (TDR) is transferred to the Transmit Shift Register (TSR) as soon as the TSR is empty. Data can be written while the TSR is shifting out the previous byte of data, providing double buffering for the transmit data.

**Transmit Interrupt Register.** This register controls and provides status of potential interrupting conditions in the transmitter. The mechanism is also provided for clearing conditions which are causing an interrupt.

**Transmit Fill Register.** This register holds a character that can be sent between frames in HDLC mode, or in case of an Underrun, in TRANSPARENT mode.

**Receive Mode Register.** This register selects the main operating mode of the Receiver (TRANSPARENT, HDLC, NRZI HDLC), its I/O configuration (TDM, I/O by means of device pins, and so on), when DMA data transfers are requested, when the receiver begins assembling characters, when it is switched from the Inactive state to TRANSPARENT mode, and the type of CRC used in HDLC modes.

**Receive Interrupt Register.** This register handles incoming interrupts. Most of the interrupt requirements for HDLC reception can be handled by enabling Status interrupts in the DMA channel associated with each Receiver. The only Receiver interrupt condition that is not handled by this means is the Idle condition. Idle interrupts are controlled by this register. This register also allows several commands which deal with interrupts and HUNT mode to be issued to the receiver.

**DMA Select Register.** This register selects the DMA channels to be used by the receiver and transmitter and enables their operation.

**Counter Access Port.** This port allows the 380C to write and read the starting values for various counters in the HDLC channel. These counters are the Baud Rate Generator time constant, the Transmitter TDM start and length values, and the Receiver TDM start and length values.

**Global HDLC Vector Register.** This register provides the base interrupt vector for the HDLC channels and identifies the HDLC device which is causing an interrupt to be issued.

## GCI/SCIT Interface

### GCI/SCIT Frame Structure (Terminal Mode)

GCI/SCIT includes three sub-frames called channels 0, 1, and 2, each containing 32 bits. This 12-byte frame is repeated at a rate of 8 KHz, giving an aggregate data rate of 768 Kbps. Figure 32 depicts the frame structure.

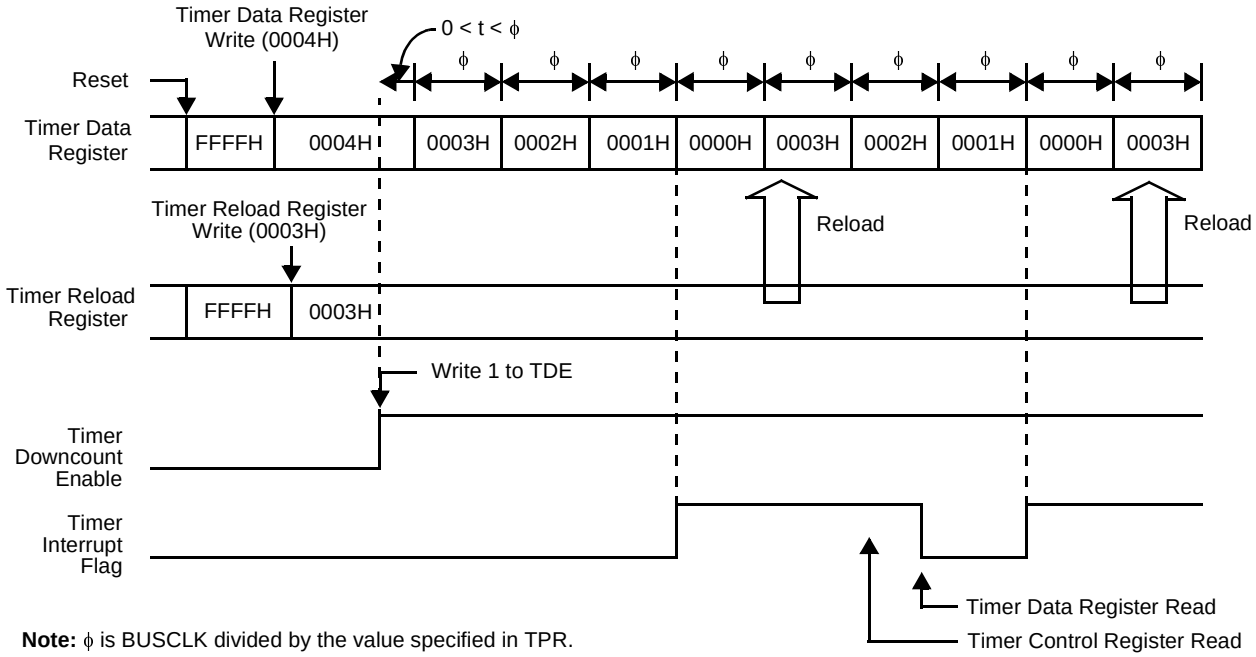
### PRT Per-Channel Registers

The I/O-mapped per-channel registers in each PRT are:

- Timer Data Registers High/Low
- Timer Reload Registers High/Low

**Timer Data Registers.** Each PRT has a 16-bit Timer Data Register (TMDR). TMDR is decremented once every clock output from the timer prescaler, which divides the BUSCLK signal of the Z382 by a value which is specified, independently for PRT1 and PRT0, in the TPR. When TMDR counts down to 0, it is automatically reloaded with the value contained in its Timer Reload Register (RLDR).

**Timer Reload Registers.** Each PRT has a 16-bit Timer Reload Register (RLDR) When a PRT channel's TMDR counts down to 0, it is automatically reloaded with the contents of its RLDR. Figure 36 illustrates the operation of the PRT.




**Note:** ϕ is BUSCLK divided by the value specified in TPR.

**Figure 36. PRT Operation Timing Diagram**

## Watch-Dog Timer

A Watch-Dog Timer (WDT) with programmable timeout intervals prevents code runaway and possible resulting system damage. The $\overline{\text{RESET}}$ input can be forced as an output upon the terminal count of the WDT, allowing external peripherals to be reset along with the Z382. Unlike other on-chip functions, the WDT is enabled

- I/OCS1 High and Low Address Registers
- I/OCS2 High and Low Address Registers

**I/O Chip Select 1/2 High and Low Address Registers.** Specify the base address and the I/O block size for I/O Chip Selects 1 and 2.

## RAM and ROM Chip Selects

Three memory chip select outputs are provided: $\overline{\text{ROMCS}}$, $\overline{\text{RAMCSL}}$, and $\overline{\text{RAMCSH}}$. These outputs support both 8- and 16-bit memories, and are asserted for a selected address range (4 KB to 8 MB) during both memory and I/O cycles. Unlike Chip Select and $\overline{\text{MSIZE}}$ signalling, Wait State generation can be specified which occurs only during memory cycles.

For the selected ROM and/or RAM range, the $\overline{\text{MSIZE}}$ pin can be programmed to be forced Low in an open-drain fashion when the address is in the programmed range, forcing 8-bit accesses in one or both ranges. When $\overline{\text{MSIZE}}$ is forced for 8-bit RAM in this way, $\overline{\text{RAMCSL}}$ is asserted for all cycles in the selected address range, and the $\overline{\text{RAMCSH}}$ pin assumes its alternate use as port pin PC7. When $\overline{\text{MSIZE}}$ is not forced for 8-bit RAM, $\overline{\text{RAMCSL}}$ is qualified by $\overline{\text{BLEN}}$, and $\overline{\text{RAMCSH}}$ acts as a chip select output pin and is qualified by $\overline{\text{BHEN}}$.

### RAM and ROM Chip Select Registers

The following I/O-mapped registers are associated with the RAM and ROM chip selects and can be read and written by the 380C processor:

- RAM Address High and Low Registers
- ROM Address High and Low Registers
- Memory Mode Register 1
- Memory Mode Register 2

**RAM Address High and Low Registers.** These registers specify which bits of the address bus are used in the address comparison and thus, the memory block size. The block size can range from 4 KB to 8 MB.

**ROM Address High and Low Registers.** These registers specify which bits of the address bus are used in the address comparison and thus, the memory block size. The block size can range from 4 KB to 8 MB.

**Memory Mode Register 1.** This register enables the ROM chip select, specifies the number of wait states for the ROM chip select, and specifies the number of T1 Wait states for the RAM chip select.

**Memory Mode Register 2.** This register enables the RAM chip select, specifies 8- or 16-bit memory accesses for the RAM and ROM chip selects independently, and specifies the number of T2 and T3 Wait states for the RAM chip select.

### RETI Instruction

The original Z80 family I/O devices (PIO, SIO, CTC) are designed to monitor the Return from Interrupt Op Codes in the instruction stream, signifying the end of the current interrupt service routine. On the Z382, the M1 signal is active during all instruction fetch transactions. Because the Z382 may not execute an RETI that it fetches, and because it supports a 16-bit data bus, only half of which is visible to an 8-bit peripheral, the Z382 does not support RETI decoding by the PIO, SIO, and CTC.

### Interrupt Registers

The following I/O-mapped registers are associated with interrupts and can be read and written by the 380C processor:

- Interrupt Enable Register
- Assigned Vectors Base Register
- INT3-1 Control Register
- Trap and Break Register

**Interrupt Enable Register.** This register provides the current status of the $\overline{\text{INT3-0}}$ pins and controls whether $\overline{\text{INT3}}$, $\overline{\text{INT2}}$, $\overline{\text{INT1}}$, and $\overline{\text{INT0}}$ are enabled or disabled. These flags are also affected by enable and disable interrupt instructions (DI (n) and EI (n)).

**Assigned Vectors Base Register.** The Interrupt Register Extension, Iz, together with the contents in bits 1-7 of this register, define the base address of the assigned interrupt vectors table in memory space.

**INT3-1 Control Register.** This register controls when and how the Z382 recognizes an interrupt on the corresponding pins (High or Low Level sensitive, Falling or Rising Edge Triggered) and provides the means for clearing edge triggered interrupt requests if such are specified for $\overline{\text{INT3-1}}$.

**Trap and Break Register.** Two bits of this register provide status on traps. One bit is set if an undefined opcode is fetched in the instruction stream. A second bit is set if an undefined opcode is returned as a vector in an interrupt acknowledge transaction in mode 0.

## Z380-Compatible Peripheral Functions

The Z382 incorporates a number of Z80380 compatible functions. The Z382's I/O bus can be programmed to run at a slower rate than its memory bus. In addition, a heartbeat transaction can be generated on the I/O bus that emulates a Z80 instruction fetch cycle. Such cycles are needed for a particular Z80 family I/O

- Whether the pins normally used for HDLC 0 are used for ASCI0 signals instead.
- Whether the pins normally used for HDLC 1 are used for ASCI1 signals instead.
- The functions of pins 47, 48, 49, 53, 56, 57, 58 and 109.

### Programmable Low-Noise Drivers

To help reduce noise generated by the Z382 output switching, selected outputs can be placed in a reduced drive configuration. When a pin is placed in LOW NOISE mode, its drive is reduced to 1/3 of its normal output drive current. This decreases the slew rate of the driver, which reduces current spikes induced onto the power bussing of the Z382.

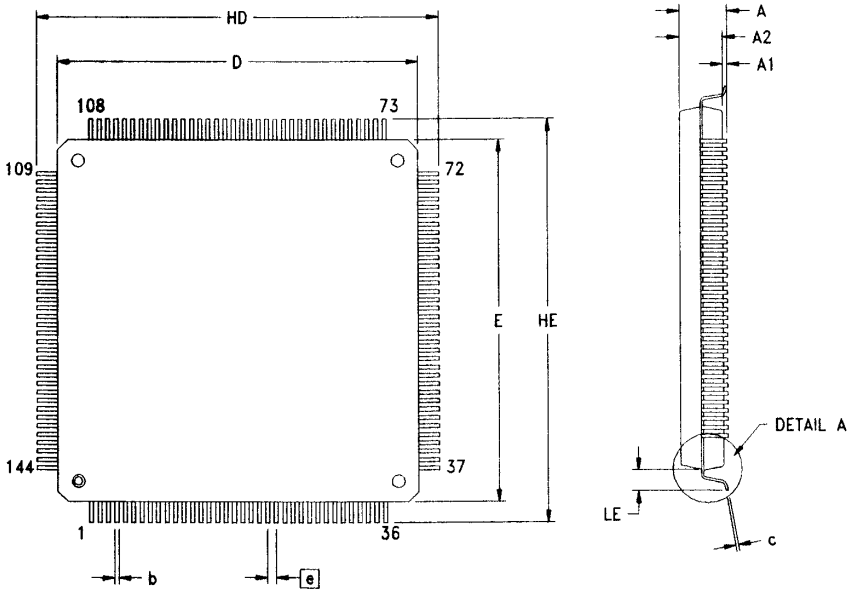
The Output Drive Control Register provides this function for a number of groups of Z382 output or I/O pins.

## Z382 I/O Register Maps

**Table 38. Z80380-Compatible Registers**

| Register Name | Z382 Address | Z380 Address | Access |
|---|---|---|---|
| Assigned Vectors Base Register | 0018H | 0018H | R/W |
| Trap and Break Register | 0019H | 0019H | R/W |
| I/O Waits Register | 001EH | 000EH | R/W |
| Refresh Waits Register | 001FH | 000FH | R/W |
| Clock Control Register | 0021H | 0011H | R/W |
| Refresh Register 0 | 0023H | 0013H | R/W |
| Refresh Register 1 | 0024H | 0014H | R/W |
| Refresh Register 2 | 0025H | 0015H | R/W |
| Standby Mode Control Register | 0026H | 0016H | R/W |
| Interrupt Enable Register | 0027H | 0017H | R/W |
| Chip Version ID Register | 0020H | 00FFH | RO |

# Package Information




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 3.42 | 4.07 | .135 | .160 |
| A1 | 0.25 | – | .010 | – |
| A2 | 3.17 | 3.67 | .125 | .144 |
| b | 0.22 | 0.38 | .009 | .015 |
| c | 0.13 | 0.23 | .004 | .009 |
| HD | 30.95 | 31.45 | 1.219 | 1.238 |
| D | 27.90 | 28.10 | 1.098 | 1.106 |
| HE | 30.95 | 31.45 | 1.219 | 1.238 |
| E | 27.90 | 28.10 | 1.098 | 1.106 |
| e | 0.65 TYP | | .026 TYP | |
| L | 0.65 | 0.95 | .026 | .037 |
| LE | 1.60 REF | | .063 REF | |

CONTROLLING DIMENSIONS : MM
MAX COPLANARITY : .10mm (.004")

**Figure 38. 144-Lead Plastic QFP Package Diagram**

## H