Nuvoton Technology Corporation - W77L532A25FL Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, Serial Port
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w77l532a25fl

Pin Description, continued

SYMBOL	TYPE	DESCRIPTIONS
P3.0–P3.7	I/O	**PORT 3:** Port 3 is a bi-directional I/O port with internal pull-ups. All bits have alternate functions, which are described below: RXD(P3.0) : Serial Port 0 input TXD(P3.1) : Serial Port 0 output $\overline{INT0}$ (P3.2) : External Interrupt 0 $\overline{INT1}$ (P3.3) : External Interrupt 1 T0(P3.4) : Timer 0 External Input T1(P3.5) : Timer 1 External Input $\overline{WR}$ (P3.6) : External Data Memory Write Strobe $\overline{RD}$ (P3.7) : External Data Memory Read Strobe
P4.0–P4.3	I/O	**PORT 4:** Port 4 is a 4-bit bi-directional I/O port. The P4.0 also provides the alternate function $\overline{WAIT}$ which is the wait state control signal. The P4.3 also provide the alternate function /REBOOT which is H/W reboot from LD flash.

*** Note: TYPE** I: input, O: output, I/O: bi-directional.

5. FUNCTIONAL DESCRIPTION

The W77L532 is 8052 pin compatible and instruction set compatible. It includes the resources of the standard 8052 such as four 8-bit I/O Ports, three 16-bit timer/counters, full duplex serial port and interrupt sources.

The W77L532 features a faster running and better performance 8-bit CPU with a redesigned core processor without wasted clock and memory cycles. it improves the performance not just by running at high frequency but also by reducing the machine cycle duration from the standard 8052 period of twelve clocks to four clock cycles for the majority of instructions. This improves performance by an average of 1.5 to 3 times. The W77L532 also provides dual Data Pointers (DPTRs) to speed up block data memory transfers. It can also adjust the duration of the MOVX instruction (access to off-chip data memory) between two machine cycles and nine machine cycles. This flexibility allows the W77L532 to work efficiently with both fast and slow RAMs and peripheral devices. In addition, the W77L532 contains on-chip 1KB MOVX SRAM, the address of which is between 0000H and 03FFH. It only can be accessed by MOVX instruction; this on-chip SRAM is optional under software control.

The W77L532 is an 8052 compatible device that gives the user the features of the original 8052 device, but with improved speed and power consumption characteristics. It has the same instruction set as the 8051 family, with one addition: DEC DPTR (op-code A5H, the DPTR is decreased by 1). While the original 8051 family was designed to operate at 12 clock periods per machine cycle, the W77L532 operates at a much reduced clock rate of only 4 clock periods per machine cycle. This naturally speeds up the execution of instructions. Consequently, the W77L532 can run at a higher speed as compared to the original 8052, even if the same crystal is used. Since the W77L532 is a fully static CMOS design, it can also be operated at a lower crystal clock, giving the same throughput in terms of instruction execution, yet reducing the power consumption.

The 4 clocks per machine cycle feature in the W77L532 is responsible for a three-fold increase in execution speed. The W77L532 has all the standard features of the 8052, and has a few extra peripherals and features as well.

I/O Ports

The W77L532 has four 8-bit ports and one extra 4-bit port. Port 0 can be used as an Address/Data bus when external program is running or external memory/device is accessed by MOVC or MOVX instruction. In these cases, it has strong pull-ups and pull-downs, and does not need any external pull-ups. Otherwise it can be used as a general I/O port with open-drain circuit. Port 2 is used chiefly as the upper 8-bits of the Address bus when port 0 is used as an address/data bus. It also has strong pull-ups and pull-downs when it serves as an address bus. Port 1 and 3 act as I/O ports with alternate functions. Port 4 is only available on 44-pin PLCC/QFP package type. It serves as a general purpose I/O port as Port 1 and Port 3. The P4.0 has an alternate function $CP/\overline{RL2}$ which is the wait state control signal. When wait state control signal is enabled, P4.0 is input only.

Serial I/O

The W77L532 has two enhanced serial ports that are functionally similar to the serial port of the original 8052 family. However the serial ports on the W77L532 can operate in different modes in order to obtain timing similarity as well. **Note that the serial port 0 can use Timer 1 or 2 as baud rate generator, but the serial port 1 can only use Timer 1 as baud rate generator**. The serial ports have the enhanced features of Automatic Address recognition and Frame Error detection.

6. MEMORY ORGANIZATION

The W77L532 separates the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

Program Memory

The Program Memory on the standard 8052 can only be addressed to 64 Kbytes long. By invoking the banking methodology, W77L532 can extend to two 64KB flash EPROM banks, APFLASH0 and APFLASH1. There are on-chip ROM banks which can be used similarly to that of the 8052. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region. There is an auxiliary 4KB Flash EPROM bank (LDFLASH) resided user loader program for In-System Programming (ISP). Both APFLASHs allow serial or parallel download according to user loader program in LDFLASH.

Data Memory

The W77L532 can access up to 64Kbytes of external Data Memory. This memory region is accessed by the MOVX instructions. Unlike the 8051 derivatives, the W77L532 contains on-chip 1K bytes MOVX SRAM of Data Memory, which can only be accessed by MOVX instructions. These 1K bytes of SRAM are between address 0000H and 03FFH. Access to the on-chip MOVX SRAM is optional under software control. When enabled by software, any MOVX instruction that uses this area will go to the on-chip RAM. MOVX addresses greater than 03FFH automatically go to external memory through Port 0 and 2. When disabled, the 1KB memory area is transparent to the system memory map. Any MOVX directed to the space between 0000H and FFFFH goes to the expanded bus on Port 0 and 2. This is the default condition. In addition, the W77L532 has the standard 256 bytes of on-chip Scratchpad RAM. This can be accessed either by direct addressing or by indirect addressing. There are also some Special Function Registers (SFRs), which can only be accessed by direct addressing. Since the Scratchpad RAM is only 256 bytes, it can be used only when data contents are small. In the event that larger data contents are present, two selections can be used. One is on-chip MOVX SRAM , the other is the external Data Memory. The on-chip MOVX SRAM can only be accessed by a MOVX instruction, the same as that for external Data Memory. However, the on-chip RAM has the fastest access times.

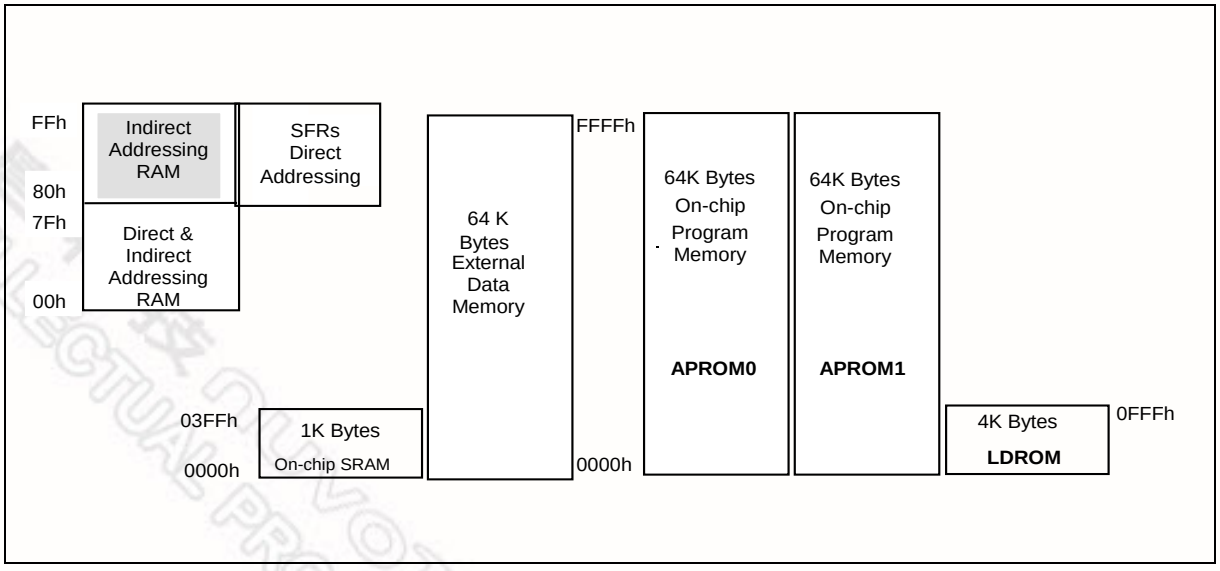


Figure 1. Memory Map

A brief description of the SFRs now follows.

PORT 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

Port 0 is an open-drain bi-directional I/O port. This port also provides a multiplexed low order address/data bus during accesses to external memory. Besides, it has internal pull-up resisters enabled by setting P0UP of P4CSIN (A2H) to high.

STACK POINTER

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

The Stack Pointer stores the Scratchpad RAM address where the stack begins. In other words, it always points to the top of the stack.

DATA POINTER LOW

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

This is the low byte of the standard 8052 16-bit data pointer.

DATA POINTER HIGH

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

This is the high byte of the standard 8052 16-bit data pointer.

DATA POINTER LOW1

Bit:	7	6	5	4	3	2	1	0
	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0

Mnemonic: DPL1 Address: 84h

M1, M0: Mode Select bits:

M1	M0	MODE
0	0	Mode 0: 8-bits with 5-bit prescale.
0	1	Mode 1: 16-bits, no prescale.
1	0	Mode 2: 8-bits with auto-reload from THx
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer 0 control bits. TH0 is a 8-bit timer only controlled by Timer 1 control bits. (Timer 1) Timer/counter is stopped.

TIMER 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

TL0.7-0: Timer 0 LSB

TIMER 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

TL1.7-0:Timer 1 LSB

TIMER 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

TH0.7-0: Timer 0 MSB

TIMER 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

TH1.7-0: Timer 1 MSB

PORT 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7-0: General purpose I/O port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. Some pins also have alternate input or output functions. This alternate functions are described below:

P1.0 : T2	External I/O for Timer/Counter 2
P1.1 : T2EX	Timer/Counter 2 Capture/Reload Trigger
P1.2 : RXD1	Serial Port 1 Receive
P1.3 : TXD1	Serial Port 1 Transmit
P1.4 : INT2	External Interrupt 2
P1.5 : $\overline{\text{INT3}}$	External Interrupt 3
P1.6 : INT4	External Interrupt 4
P1.7 : $\overline{\text{INT5}}$	External Interrupt 5

EXTERNAL INTERRUPT FLAG

Bit:	7	6	5	4	3	2	1	0
	IE5	IE4	IE3	IE2	-	-	-	-

Mnemonic: EXIF Address: 91h

IE5: External Interrupt 5 flag. Set by hardware when a falling edge is detected on $\overline{\text{INT5}}$.

IE4: External Interrupt 4 flag. Set by hardware when a rising edge is detected on INT4.

IE3: External Interrupt 3 flag. Set by hardware when a falling edge is detected on $\overline{\text{INT3}}$.

IE2: External Interrupt 2 flag. Set by hardware when a rising edge is detected on INT2.

PORT 4 CONTROL REGISTER A

Bit:	7	6	5	4	3	2	1	0
	P41M1	P41M0	P41C1	P41C0	P40M1	P40M0	P40C1	P40C0

Mnemonic: P4CONA Address: 92h

PORT 4 CONTROL REGISTER B

Bit:	7	6	5	4	3	2	1	0
	P43M1	P43M0	P43C1	P43C0	P42M1	P42M0	P42C1	P42C0

Mnemonic: P4CONB Address: 93h

SLAVE ADDRESS

Bit:	7	6	5	4	3	2	1	0

Mnemonic: SADDR Address: A9h

SADDR: The SADDR should be programmed to the given or broadcast address for serial port 0 to which the slave processor is designated.

SLAVE ADDRESS 1

Bit:	7	6	5	4	3	2	1	0

Mnemonic: SADDR1 Address: AAh

SADDR1: The SADDR1 should be programmed to the given or broadcast address for serial port 1 to which the slave processor is designated.

ROM BANKING CONTROL

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	EN128K	DCP12	DCP11	DCP10

Mnemonic: ROMCON Address: ABh

EN128K: On-chip ROM banking enable. Set this bit to enable APFLASH0 and APFLASH1 by banking mechanism. The P1.x is selected to be the auxiliary highest address line A16.

DCP1x: A16 selection. By default, P1.7 is defined as A16.

A16	P1.0	P1.1	P1.2	P1.3	P1.4	P1.5	P1.6	P1.7
DCP12	0	0	0	0	1	1	1	1
DCP11	0	0	1	1	0	0	1	1
DCP10	0	1	0	1	0	1	0	1

ISP ADDRESS LOW BYTE

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Mnemonic: SFRAL Address: ACh

Low byte destination address for In System Programming operations. SFRAH and SFRAL address a specific ROM bytes for erasure, porgramming or read.

ACCUMULATOR

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

ACC.7-0: The A (or ACC) register is the standard 8052 accumulator.

EXTENDED INTERRUPT ENABLE

Bit:	7	6	5	4	3	2	1	0
	-	-	-	EWDI	EX5	EX4	EX3	EX2

Mnemonic: EIE Address: E8h

EIE.7-5: Reserved bits, will read high

EWDI: Enable Watchdog timer interrupt

EX5: External Interrupt 5 Enable.

EX4: External Interrupt 4 Enable.

EX3: External Interrupt 3 Enable.

EX2: External Interrupt 2 Enable.

B REGISTER

Bit:	7	6	5	4	3	2	1	0
	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0

Mnemonic: B Address: F0h

B.7-0: The B register is the standard 8052 register that serves as a second accumulator.

EXTENDED INTERRUPT PRIORITY

Bit:	7	6	5	4	3	2	1	0
	-	-	-	PWDI	PX5	PX4	PX3	PX2

Mnemonic: EIP Address: F8h

EIP.7-5: Reserved bits.

PWDI: Watchdog timer interrupt priority.

PX5: External Interrupt 5 Priority. 0 = Low priority, 1 = High priority.

PX4: External Interrupt 4 Priority. 0 = Low priority, 1 = High priority.

PX3: External Interrupt 3 Priority. 0 = Low priority, 1 = High priority.

PX2: External Interrupt 2 Priority. 0 = Low priority, 1 = High priority.

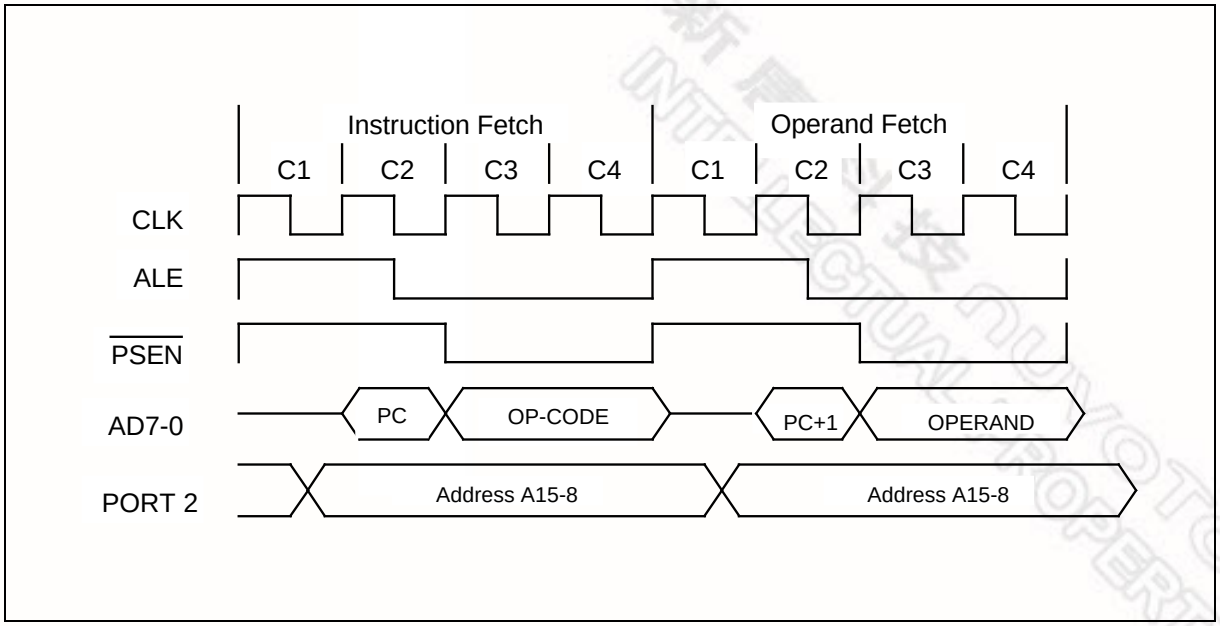


Figure 4. Two Cycle Instruction Timing

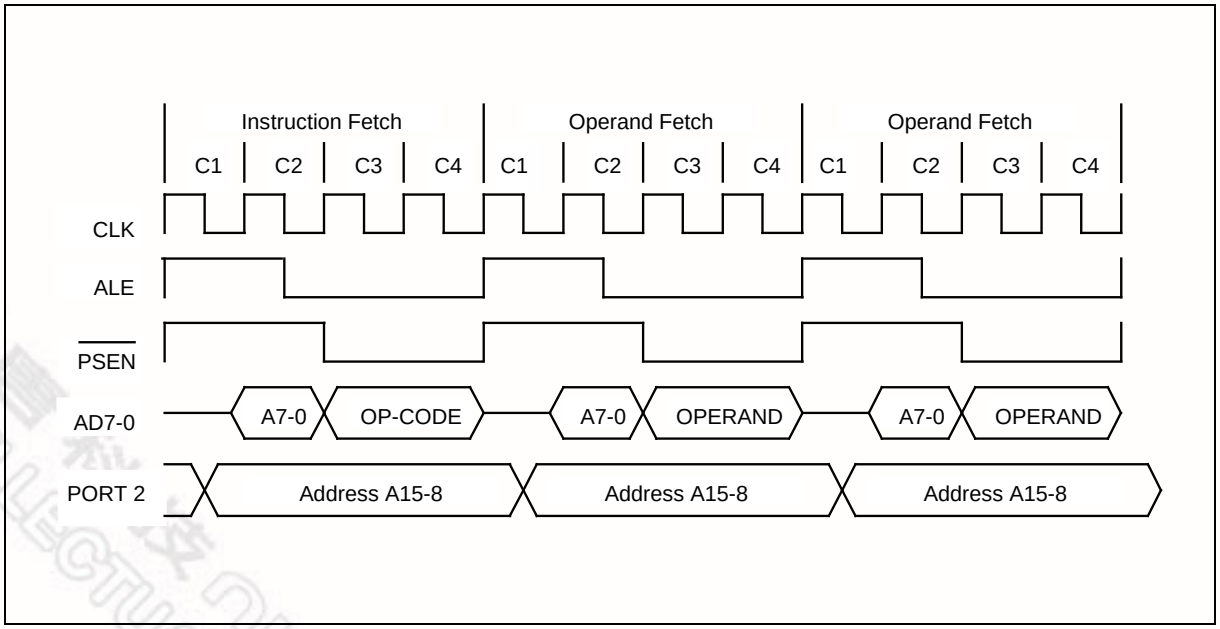


Figure 5. Three Cycle Instruction Timing

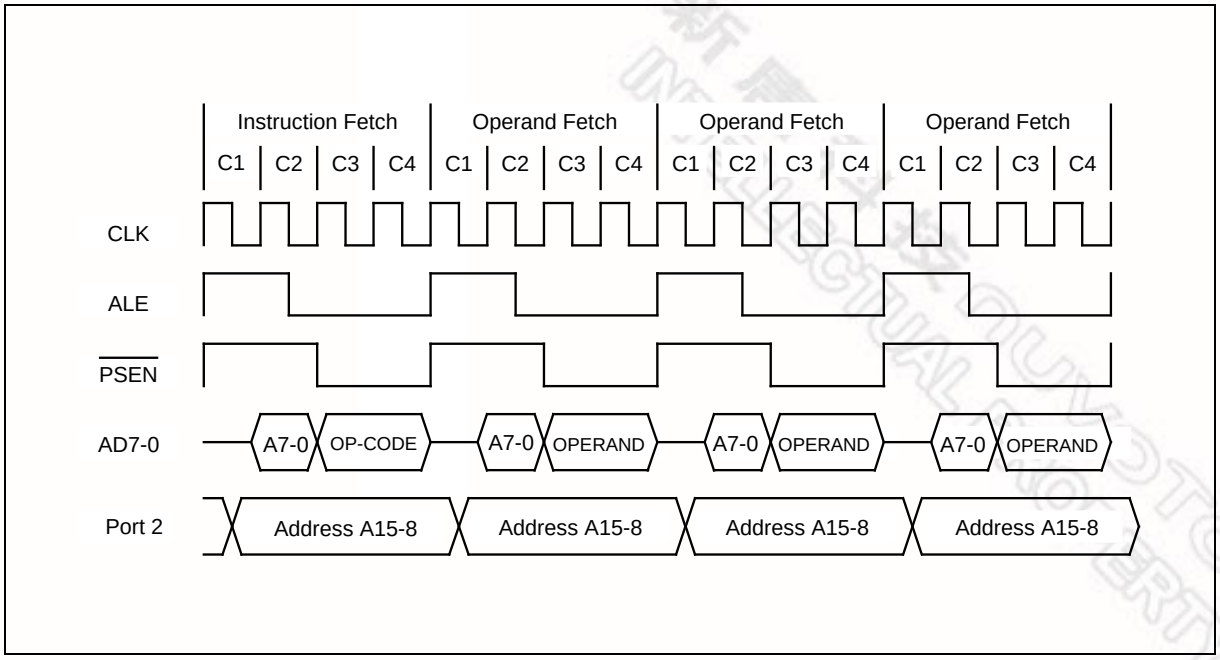


Figure 6. Four Cycle Instruction Timing

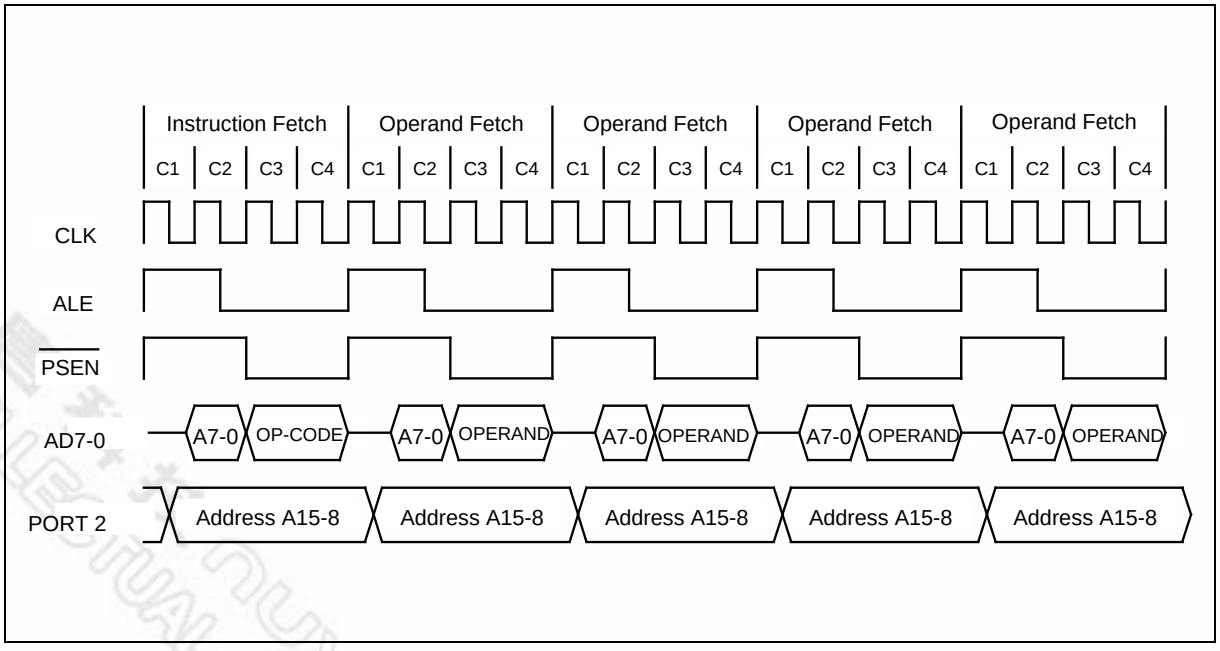


Figure 7. Five Cycle Instruction Timing

10. RESET CONDITIONS

The user has several hardware related options for placing the W77L532 into reset condition. In general, most register bits go to their reset value irrespective of the reset condition, but there are a few flags whose state depends on the source of reset. The user can use these flags to determine the cause of reset using software. There are two ways of putting the device into reset state. They are External reset and Watchdog reset.

External Reset

The device continuously samples the RST pin at state C4 of every machine cycle. Therefore the RST pin must be held for at least 2 machine cycles to ensure detection of a valid RST high. The reset circuitry then synchronously applies the internal reset signal. Thus the reset is a synchronous operation and requires the clock to be running to cause an external reset.

Once the device is in reset condition, it will remain so as long as RST is 1. Even after RST is deactivated, the device will continue to be in reset state for up to two machine cycles, and then begin program execution from 0000h. There is no flag associated with the external reset condition. However since the other two reset sources have flags, the external reset can be considered as the default reset if those two flags are cleared.

The software must clear the POR flag after reading it, otherwise it will not be possible to correctly determine future reset sources. If the power fails, i.e. falls below Vrst, then the device will once again go into reset state. When the power returns to the proper operating levels, the device will again perform a power on reset delay and set the POR flag.

Watchdog Timer Reset

The Watchdog timer is a free running timer with programmable time-out intervals. The user can clear the watchdog timer at any time, causing it to restart the count. When the time-out interval is reached an interrupt flag is set. If the Watchdog reset is enabled and the watchdog timer is not cleared, then 512 clocks from the flag being set, the watchdog timer will generate a reset . This places the device into the reset condition. The reset condition is maintained by hardware for two machine cycles. Once the reset is removed the device will begin execution from 0000h.

11. RESET STATE

Most of the SFRs and registers on the device will go to the same condition in the reset state. The Program Counter is forced to 0000h and is held there as long as the reset condition is applied. However, the reset state does not affect the on-chip RAM. The data in the RAM will be preserved during the reset. However, the stack pointer is reset to 07h, and therefore the stack contents will be lost. The RAM contents will be lost if the V_{DD} falls below approximately 2V, as this is the minimum voltage level required for the RAM to operate normally. Therefore after a first time power on reset the RAM contents will be indeterminate. During a power fail condition, if the power falls below 2V, the RAM contents are lost.

After a reset most SFRs are cleared. Interrupts and Timers are disabled. The Watchdog timer is disabled if the reset source was a POR. The port SFRs have FFh written into them which puts the port pins in a high state. Port 0 floats as it does not have on-chip pull-ups.

Table 6. SFR Reset Value

SFR NAME	RESET VALUE	SFR NAME	RESET VALUE
P0	11111111b	IE	00000000b
SP	00000111b	SADDR	00000000b
DPL	00000000b	P3	11111111b
DPH	00000000b	IP	x0000000b
DPL1	00000000b	SADEN	00000000b
DPH1	00000000b	T2CON	00000000b
DPS	00000000b	T2MOD	00000x00b
PCON	00xx0000b	RCAP2L	00000000b
TCON	00000000b	RCAP2H	00000000b
TMOD	00000000b	TL2	00000000b
TL0	00000000b	TH2	00000000b
TL1	00000000b	TA	11111111b
TH0	00000000b	PSW	00000000b
TH1	00000000b	WDCON	0x0x0xx0b
CKCON	00000001b	ACC	00000000b
P1	11111111b	EIE	xxx00000b
P4CONA	00000000b	P4CONB	00000000b
P40AL	00000000b	P40AH	00000000b
P41AL	00000000b	P41AH	00000000b
P42AL	00000000b	P42AH	00000000b
P43Al	00000000b	P43AH	00000000b
CHPCON	00000000b	P4CSIN	00000000b
ROMCON	00000111b	SFRAL	00000000b
SFRAH	00000000b	SFRFD	00000000b
SFRCN	00111111b		

AUTO-RELOAD MODE, COUNTING UP/DOWN

Timer/Counter 2 will be in auto-reload mode as an up/down counter if CP / $\overline{RL2}$ bit in T2CON is cleared and the DCEN bit in T2MOD is set. In this mode, Timer/Counter 2 is an up/down counter whose direction is controlled by the T2EX pin. A 1 on this pin cause the counter to count up. An overflow while counting up will cause the counter to be reloaded with the contents of the capture registers. The next down count following the case where the contents of Timer/Counter equal the capture registers will load an FFFFh into Timer/Counter 2. In either event a reload will set the TF2 bit. A reload will also toggle the EXF2 bit. However, the EXF2 bit can not generate an interrupt while in this mode.

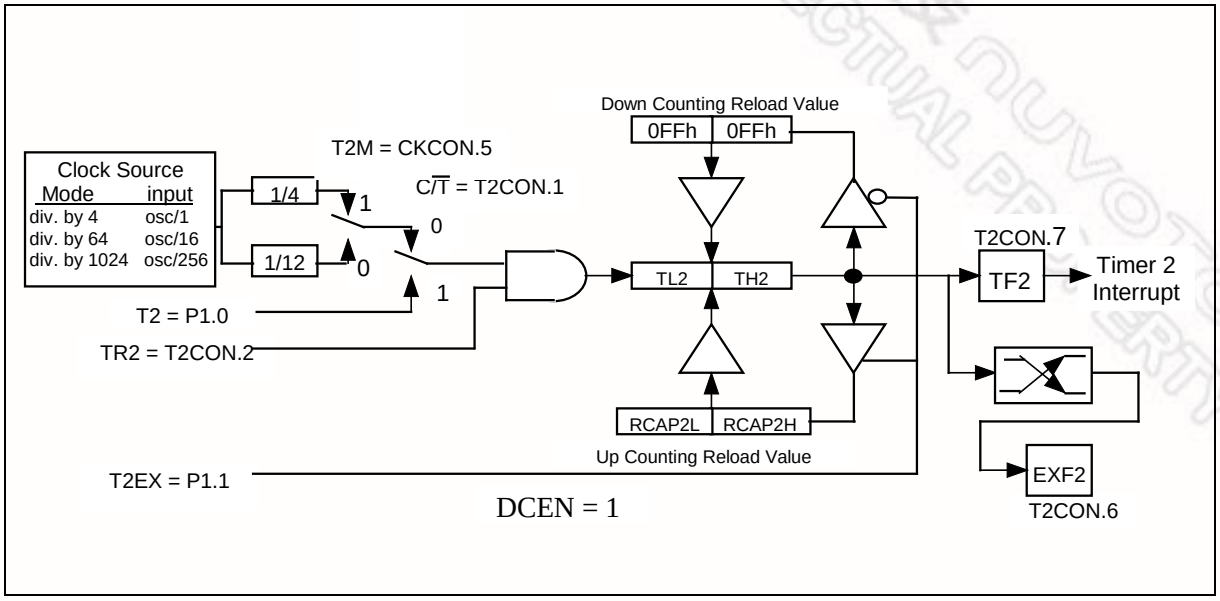


Figure 16. 16-Bit Auto-reload Up/Down Counter

BAUD RATE GENERATOR MODE

The baud rate generator mode is enabled by setting either the RCLK or TCLK bits in T2CON register. While in the baud rate generator mode, Timer/Counter 2 is a 16 bit counter with auto reload when the count rolls over from FFFFh. However, rolling over does not set the TF2 bit. If EXEN2 bit is set, then a negative transition of the T2EX pin will set EXF2 bit in the T2CON register and cause an interrupt request.

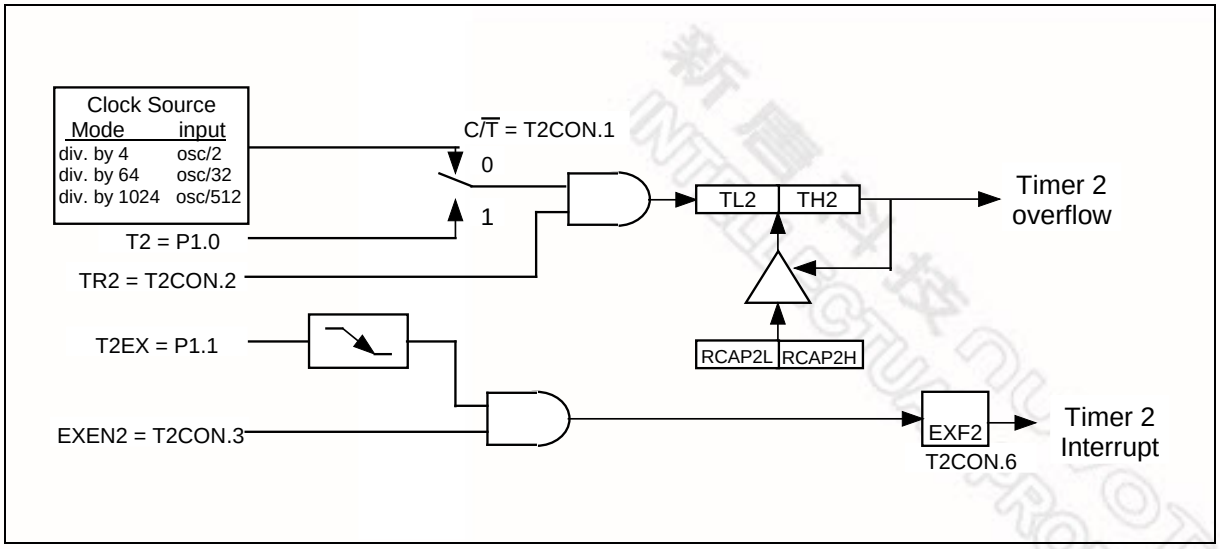


Figure 17. Baud Rate Generator Mode

PROGRAMMABLE CLOCK-OUT

Timer 2 is equipped with a new clock-out feature which outputs a 50% duty cycle clock on P1.0. It can be invoked as a programmable clock generator. To configure Timer 2 with clock-out mode, software must initiate it by setting bit T2OE = 1, C/T2 = 0 and CP/RL = 0. Setting bit TR2 will start the timer. This mode is similar to the baud rate generator mode, it will not generate an interrupt while Timer 2 overflow. So it is possible to use Timer 2 as a baud rate generator and a clock generator at the same time. The clock-out frequency is determined by the following equation:

The Clock-Out Frequency = Oscillator Frequency / [4 X (65536-RCAP2H, RCAP2L)]

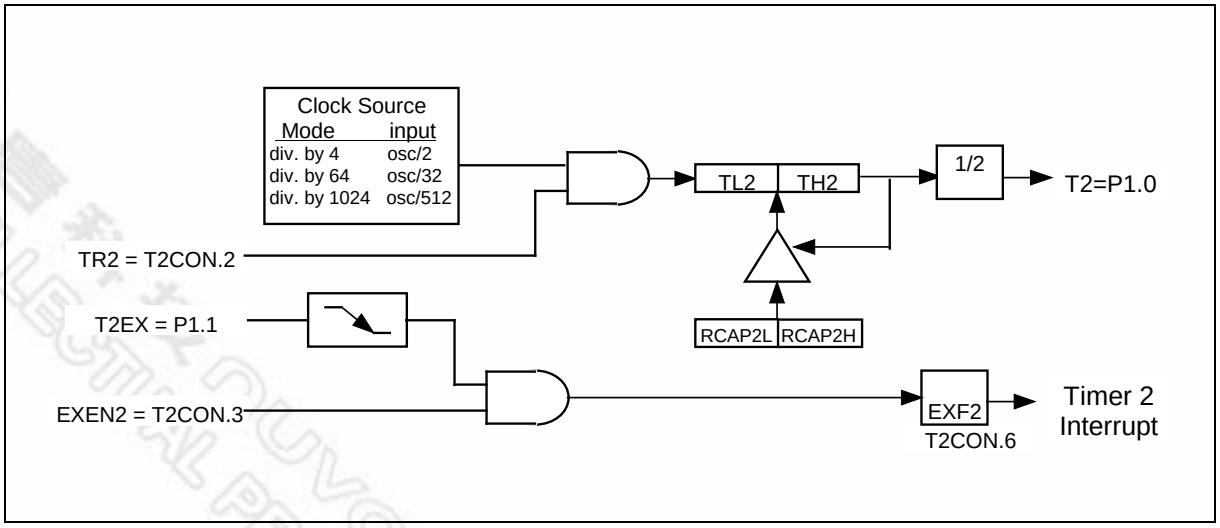


Figure 18. Programmable Clock-Out Mode

WATCHDOG TIMER

The Watchdog timer is a free-running timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs a flag is set, which can cause an interrupt if enabled, and a system reset can also be caused if it is enabled. The interrupt will occur if the individual interrupt enable and the global enable are set. The interrupt and reset functions are independent of each other and may be used separately or together depending on the users software.

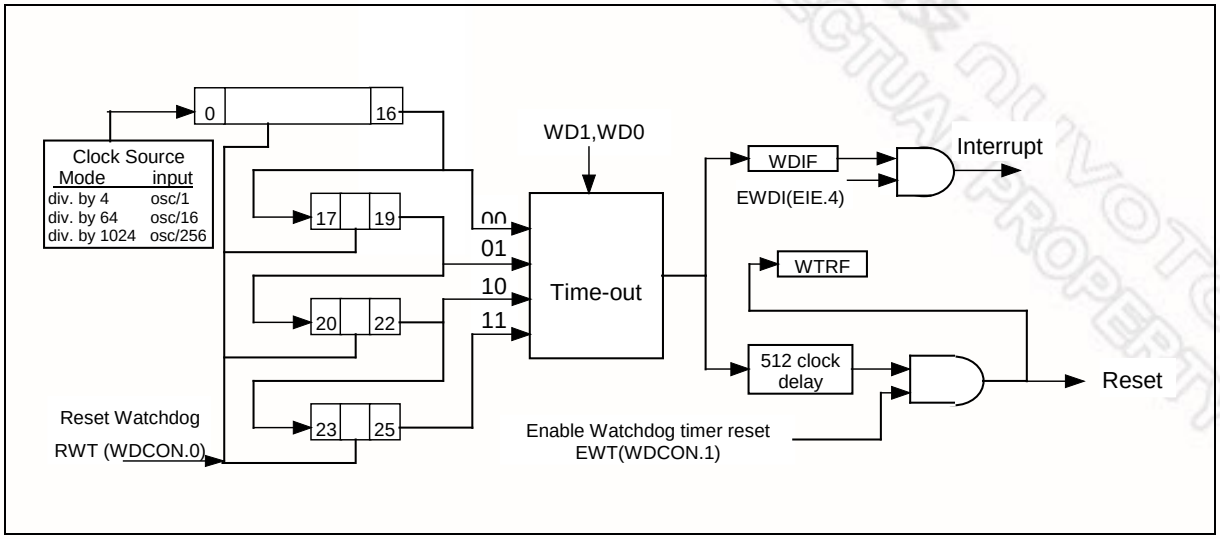


Figure 19. Watchdog Timer

The Watchdog timer should first be restarted by using RWT. This ensures that the timer starts from a known state. The RWT bit is used to restart the watchdog timer. This bit is self clearing, i.e. after writing a 1 to this bit the software will automatically clear it. The watchdog timer will now count clock cycles. The time-out interval is selected by the two bits WD1 and WD0 (CKCON.7 and CKCON.6). When the selected time-out occurs, the Watchdog interrupt flag WDIF (WDCON.3) is set. After the time-out has occurred, the watchdog timer waits for an additional 512 clock cycles. If the Watchdog Reset EWT (WDCON.1) is enabled, then 512 clocks after the time-out, if there is no RWT, a system reset due to Watchdog timer will occur. This will last for two machine cycles, and the Watchdog timer reset flag WTRF (WDCON.2) will be set. This indicates to the software that the watchdog was the cause of the reset.

When used as a simple timer, the reset and interrupt functions are disabled. The timer will set the WDIF flag each time the timer completes the selected time interval. The WDIF flag is polled to detect a time-out and the RWT allows software to restart the timer. The Watchdog timer can also be used as a very long timer. The interrupt feature is enabled in this case. Every time the time-out occurs an interrupt will occur if the global interrupt enable EA is set.

The main use of the Watchdog timer is as a system monitor. This is important in real-time control applications. In case of some power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. Using the watchdog timer interrupt during software development will allow the user to select ideal watchdog reset locations. The code is first written without the watchdog interrupt or reset. Then the watchdog interrupt is enabled to identify code locations where interrupt occurs. The user can now insert instructions to reset the watchdog timer which will allow the code to run without any watchdog timer interrupts. Now the

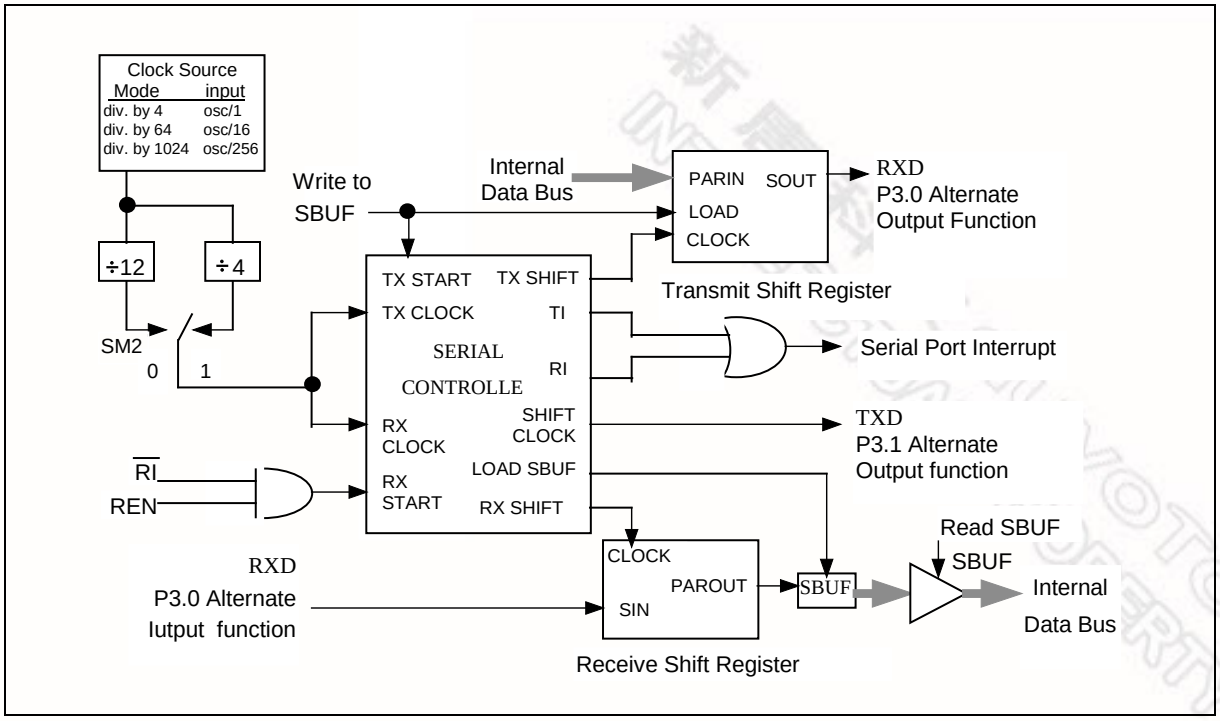


Figure 20. Serial Port Mode 1

The TI flag is set high in C1 following the end of transmission of the last bit. The serial port will receive data when REN is 1 and RI is zero. The shift clock (TxD) will be activated and the serial port will latch data on the rising edge of shift clock. The external device should therefore present data on the falling edge on the shift clock. This process continues till all the 8 bits have been received. The RI flag is set in C1 following the last rising edge of the shift clock on TxD. This will stop reception, till the RI is cleared by software.

MODE 1

In Mode 1, the full duplex asynchronous mode is used. Serial communication frames are made up of 10 bits transmitted on TXD and received on RXD. The 10 bits consist of a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in the SFR SCON. The baud rate in this mode is variable. The serial baud can be programmed to be 1/16 or 1/32 of the Timer 1 overflow. Since the Timer 1 can be set to different reload values, a wide variation in baud rates is possible.

Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at C1 following the first roll-over of divide by 16 counter. The next bit is placed on TxD pin at C1 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counter and not directly to the write to SBUF signal. After all 8 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the C1 state after the stop bit has been put out on TxD pin. This will be at the 10th rollover of the divide by 16 counter after a write to SBUF.

Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counter.

17. SECURITY BITS

Using device programmer, the Flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of Flash EPROM and those operations on it are described below. The W77L532 has Special Setting Register which can be accessed by device programmer. The register can only be accessed from the Flash EPROM operation mode. Those bits of the Security Registers can not be changed once they have been programmed from high to low. They can only be reset through erase-all operation.

B7	B6	B5	B4	B3	B2	B1	B0

Security Bits

B5 : 0 -> Eable H/W reboot with P4.3
B4 : 0 -> Enable H/W reboot with P2.6, P2.7
B1 : 0 -> MOVC Inhibited
B0 : 0-> Data out lock
Default 1 for each bit.

Special Setting Registers

B0: Lock bit

This bit is used to protect the customer's program code in the W77L532. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the Flash EPROM data and Special Setting Registers can not be accessed again.

B1: MOVC Inhibit

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

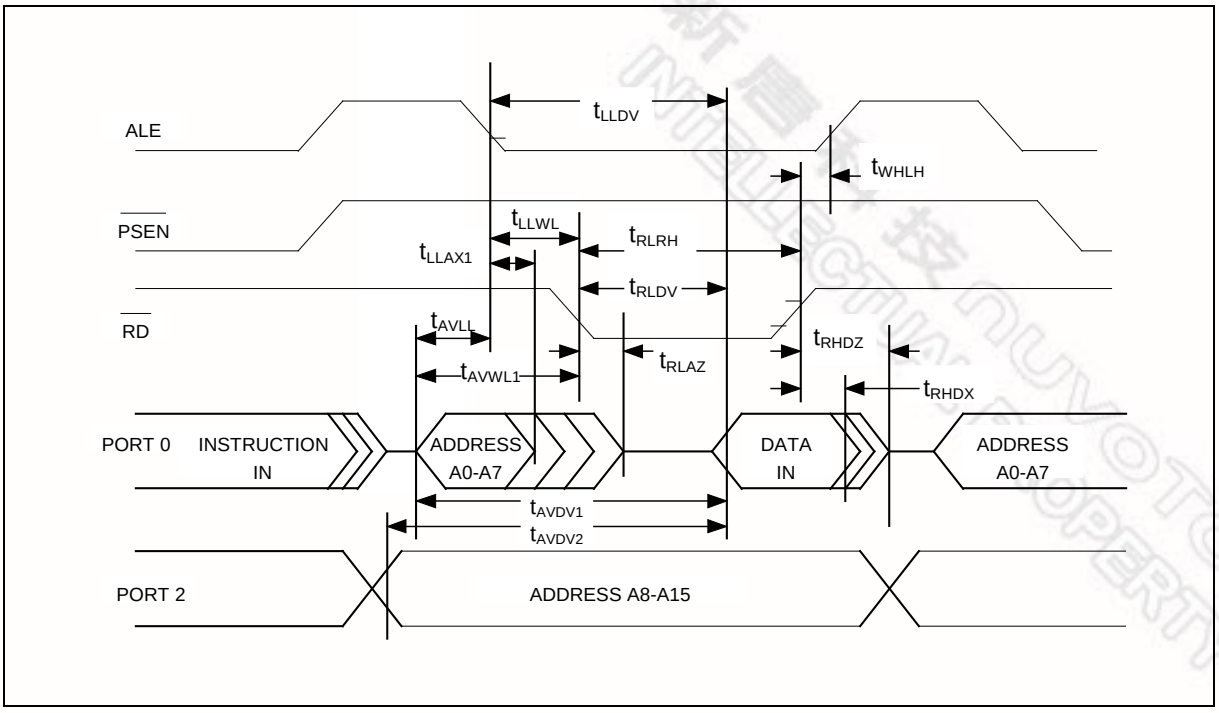
B4: H/W Reboot with P2.6 and P2.7

If this bit is set to logic 0, enable to reboot 4k LDFLASH mode while RST =H, P2.6 = L and P2.7 = L state. CPU will start from LDFLASH to update the user's program.

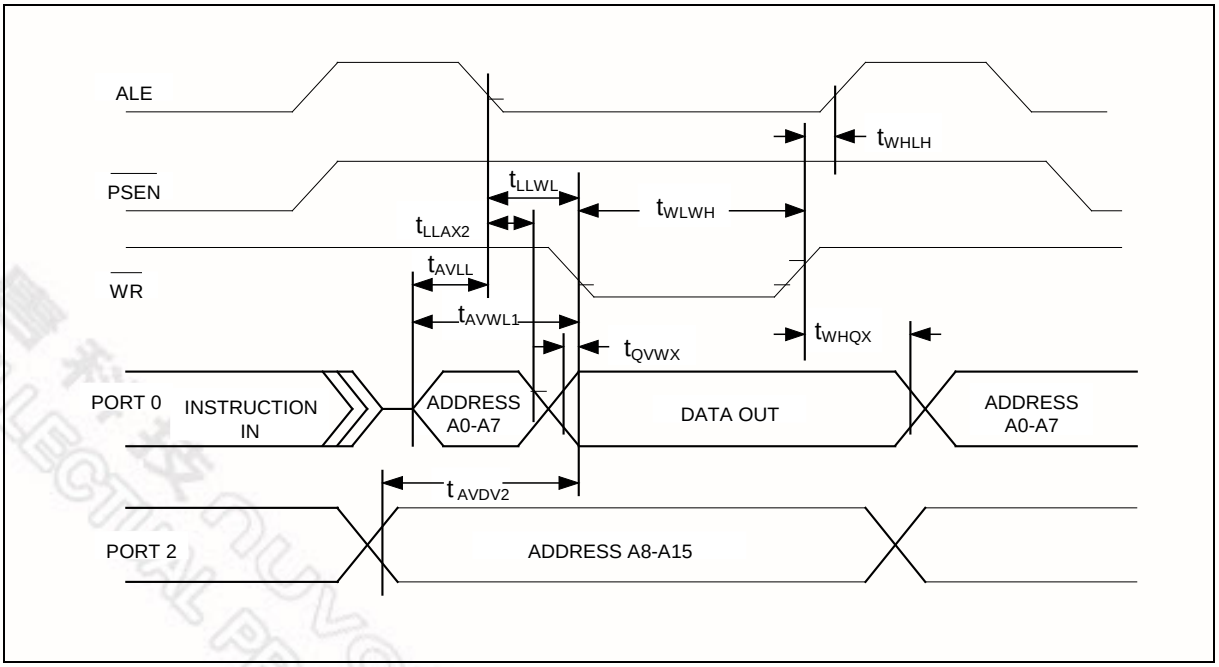
B5: H/W Reboot with P4.3

If this bit is set to logic 0, enable to reboot 4k LDFLASH mode while RST =H and P4.3 = L state. CPU will start from LDFLASH to update the user's program.

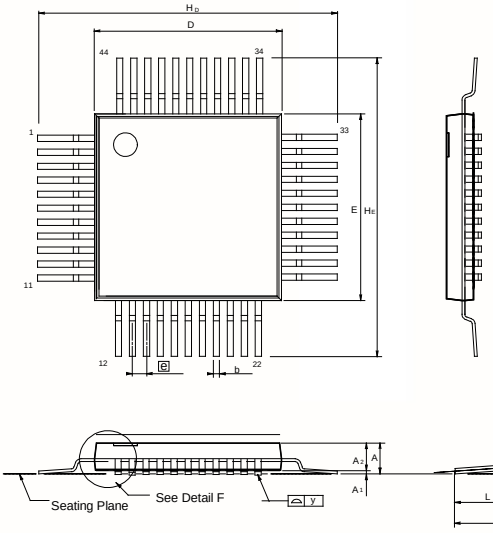
DATA MEMORY READ CYCLE



DATA MEMORY WRITE CYCLE



20.3 44-pin QFP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	---	---	---	---
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.510	0.520	0.530	12.95	13.2	13.45
H_E	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

```
        MOV  CHPCON, #03H       ; CHPCON = 03H, ENABLE IN-SYSTEM PROGRAMMING.
        MOV  SFRCN, #0H
        MOV  TCON, #00H         ; TCON = 00H, TR = 0 TIMER0 STOP
        MOV  TMOD, #01H         ; TMOD = 01H, SET TIMER0 A 16BIT TIMER
        MOV  IP, #00H           ; IP = 00H
        MOV  IE, #82H           ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV  R6, #F0H
        MOV  R7, #FFH
        MOV  TL0, R6
        MOV  TH0, R7
        MOV  TCON, #10H         ; TCON = 10H, TR0 = 1, GO
        MOV  PCON, #01H         ; ENTER IDLE MODE

 UPDATE_64K:
        MOV  TCON,#00H          ; TCON = 00H , TR = 0 TIM0 STOP
        MOV  IP, #00H           ; IP = 00H
        MOV  IE, #82H           ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV  TMOD, #01H         ; TMOD = 01H, MODE1
        MOV  R6, #D0H           ; SET WAKE-UP TIME FOR ERASE OPERATION, ABOUT 15 ms
                                  DEPENDING ON USER'S SYSTEM CLOCK RATE.
        MOV  R7, #8AH
        MOV  TL0, R6
        MOV  TH0, R7

ERASE_P_4K:
        MOV  SFRCN, #22H        ; SFRCN = 22H, ERASE 64K  APFLASH0
                                ; SFRCN = A2H, ERASE 64K APFLASH1
        MOV  TCON, #10H         ; TCON = 10H, TR0 = 1,GO
        MOV  PCON, #01H         ; ENTER IDLE MODE (FOR ERASE OPERATION)

;*********************************************************************
;* BLANK CHECK
;*********************************************************************
        MOV  SFRCN, #0H         ; SFRCN = 00H, READ 64KB APFLASH0
                                ; SFRCN = 80H, READ 64KB APFLASH1
        MOV  SFRAH, #0H         ; START ADDRESS = 0H
        MOV  SFRAL, #0H
        MOV  R6, #FDH           ; SET TIMER FOR READ OPERATION, ABOUT 1.5 μS.
        MOV  R7, #FFH
        MOV  TL0, R6
        MOV  TH0, R7

BLANK_CHECK_LOOP:
        SETB  TR0               ; ENABLE TIMER 0
        MOV  PCON, #01H         ; ENTER IDLE MODE
        MOV  A, SFRFD           ; READ ONE BYTE
        CJNE  A, #FFH, BLANK_CHECK_ERROR
        INC  SFRAL              ; NEXT ADDRESS
        MOV  A, SFRAL
        JNZ   BLANK_CHECK_LOOP
        INC  SFRAH
        MOV  A, SFRAH
        CJNE  A, #0H, BLANK_CHECK_LOOP   ; END ADDRESS = FFFFH
        JMP  PROGRAM_64KROM

BLANK_CHECK_ERROR:
```