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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	14-SOIC (0.154", 3.90mm Width)
Supplier Device Package	14-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/attiny404-ssnr

6.10.4.4 System Configuration 0

Name: SYSCFG0
Offset: 0x05
Reset: 0xC4
Property: -

Bit	7	6	5	4	3	2	1	0
	CRCSRC[1:0]							EESAVE
Access	R	R						R
Reset	1	1						0

Bits 7:6 – CRCSRC[1:0] CRC Source
See CRC description for more information about the functionality.

Value	Name	Description
00	FLASH	CRC of full Flash (boot, application code and application data)
01	BOOT	CRC of boot section
10	BOOTAPP	CRC of application code and boot sections
11	NOCRC	No CRC

Bit 0 – EESAVE EEPROM Save During Chip Erase
If the device is locked the EEPROM is always erased by a chip erase, regardless of this bit.

Value	Description
0	EEPROM erased during chip erase
1	EEPROM not erased under chip erase

8.7.3 Status Register

Name: SREG
Offset: 0x0F
Reset: 0x00
Property: -

The Status register contains information about the result of the most recently executed arithmetic or logic instruction. For details about the bits in this register and how they are affected by the different instructions, see the Instruction Set Summary.

Bit	7	6	5	4	3	2	1	0
	I	T	H	S	V	N	Z	C
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – I Global Interrupt Enable
Writing a '1' to this bit enables interrupts on the device.

Writing a '0' to this bit disables interrupts on the device, independent of the individual interrupt enable settings of the peripherals.

This bit is not cleared by hardware after an interrupt has occurred.

This bit can be set and cleared by software with the `SEI` and `CLI` instructions.

Changing the I flag through the I/O register results in a one-cycle Wait state on the access.

Bit 6 – T Bit Copy Storage
The bit copy instructions bit load (`BLD`) and bit store (`BST`) use the T bit as source or destination for the operated bit.

A bit from a register in the register file can be copied into this bit by the `BST` instruction, and this bit can be copied into a bit in a register in the register file by the `BLD` instruction.

Bit 5 – H Half Carry Flag
This bit indicates a half carry in some arithmetic operations. Half carry is useful in BCD arithmetic.

Bit 4 – S Sign Bit, S = N ⊕ V
The sign bit (S) is always an exclusive or (*xor*) between the negative flag (N) and the two's complement overflow flag (V).

Bit 3 – V Two's Complement Overflow Flag
The two's complement overflow flag (V) supports two's complement arithmetic.

Bit 2 – N Negative Flag
The negative flag (N) indicates a negative result in an arithmetic or logic operation.

Bit 1 – Z Zero Flag
The zero flag (Z) indicates a zero result in an arithmetic or logic operation.

12.5.1 Reset Flag Register

Name: RSTFR
Offset: 0x00
Reset: 0xXX
Property: -

All flags are cleared by writing a '1' to them. They are also cleared by a Power-on Reset, with the exception of the Power-On Reset Flag (PORF).

Bit	7	6	5	4	3	2	1	0
			UPDIRF	SWRF	WDRF	EXTRF	BORF	PORF
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	x	x	x	x	x	x

Bit 5 – UPDIRF UPDI Reset Flag
This bit is set if a UPDI Reset occurs.

Bit 4 – SWRF Software Reset Flag
This bit is set if a Software Reset occurs.

Bit 3 – WDRF Watchdog Reset Flag
This bit is set if a Watchdog Reset occurs.

Bit 2 – EXTRF External Reset Flag
This bit is set if an External Reset occurs.

Bit 1 – BORF Brown-Out Reset Flag
This bit is set if a Brown-out Reset occurs.

Bit 0 – PORF Power-On Reset Flag
This bit is set if a Power-on Reset occurs.

This flag is only cleared by writing a '1' to it.

After a POR, only the POR flag is set and all other flags are cleared. No other flags can be set before a full system boot is run after the POR.

16.5.8 Output Value Toggle

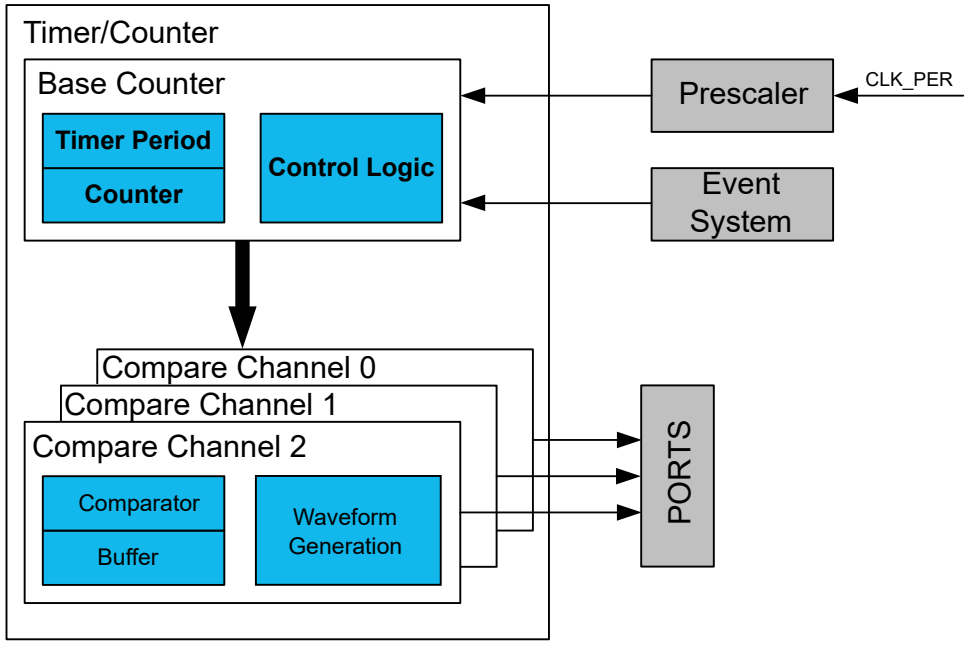
Name: OUTTGL
Offset: 0x07
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	OUTTGL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – OUTTGL[7:0] Output Value Toggle
This register can be used instead of a read-modify-write to toggle the output value of individual pins. Writing a '1' to OUTTGL[n] will toggle the corresponding bit in PORT.OUT.

Reading this bit field will always return the value of PORT.OUT.

Figure 20-1. 16-bit Timer/Counter and Closely Related Peripherals

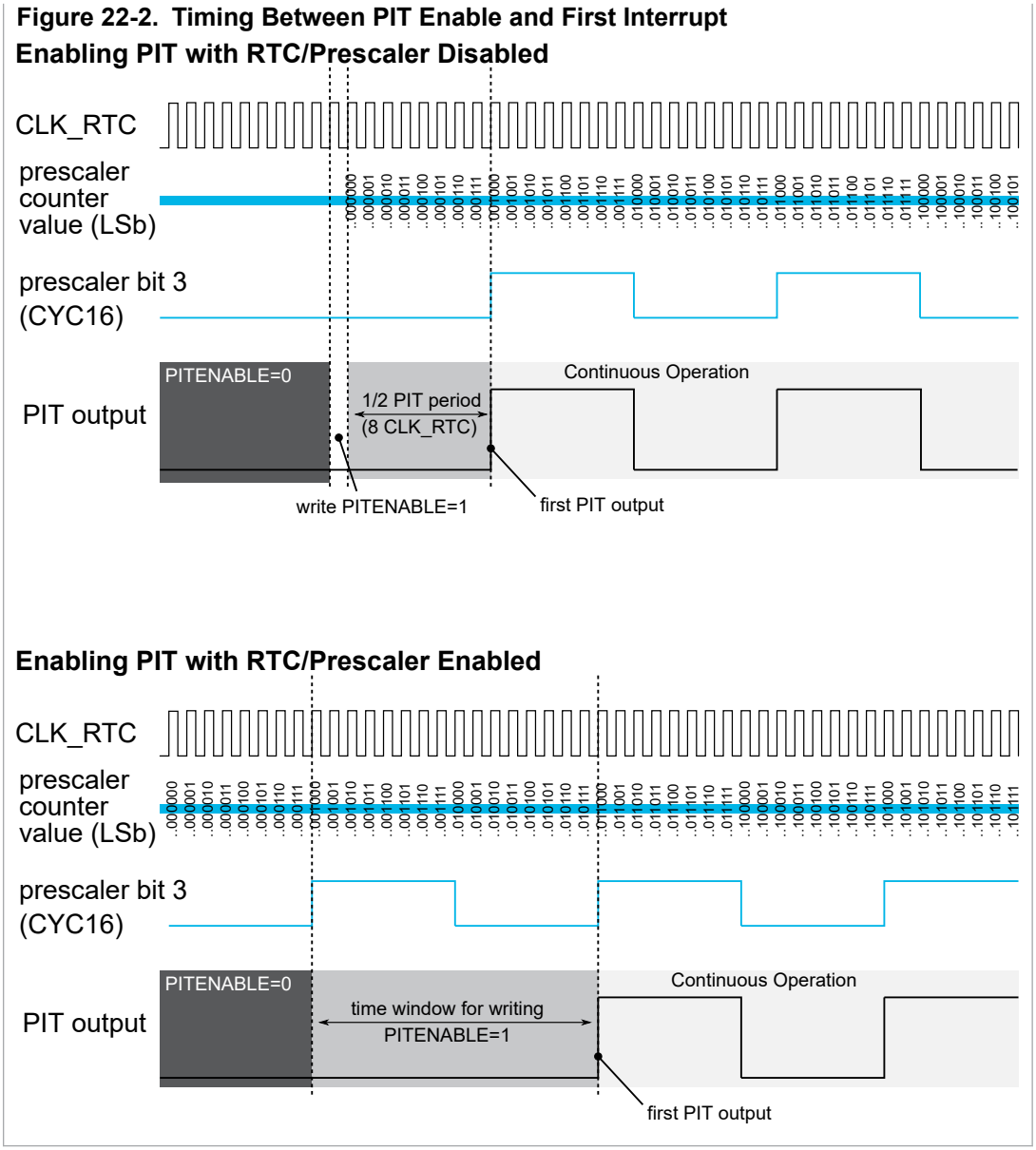


This device provides one instance of the TCA peripheral, TCA0.

20.2.1 Block Diagram

The figure below shows a detailed block diagram of the timer/counter.

Figure 22-2. Timing Between PIT Enable and First Interrupt



22.5 Events

The RTC, when enabled, will generate the following output events:

- Overflow (OVF): Generated when the counter has reached its top value and wrapped to zero. The generated strobe is synchronous with CLK_RTC and lasts one CLK_RTC cycle.
- Compare (CMP): Indicates a match between the counter value and the Compare register. The generated strobe is synchronous with CLK_RTC and lasts one CLK_RTC cycle.

When enabled, the PIT generates the following 50% duty cycle clock signals on its event outputs:

- Event 0: Clock period = 8192 RTC clock cycles
- Event 1: Clock period = 4096 RTC clock cycles
- Event 2: Clock period = 2048 RTC clock cycles

Signal	Type	Description
XCK	Input/output	Clock for synchronous operation
XDIR	Output	Transmit Enable for RS485

Related Links

I/O Multiplexing and Considerations

23.2.2 System Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

Table 23-1. USART System Dependencies

Dependency	Applicable	Peripheral
Clocks	Yes	CLKCTRL
I/O Lines and Connections	Yes	PORT
Interrupts	Yes	CPUINT
Events	Yes	EVSYS
Debug	Yes	UPDI

Related Links

Debug Operation
Clocks
I/O Lines and Connections
Interrupts
Events

23.2.2.1 Clocks

This peripheral depends on the peripheral clock.

Related Links

Clock Controller (CLKCTRL)

23.2.2.2 I/O Lines and Connections

Using the I/O lines of the peripheral requires configuration of the I/O pins.

Related Links

I/O Pin Configuration (PORT)
I/O Multiplexing and Considerations

23.2.2.3 Interrupts

Using the interrupts of this peripheral requires the interrupt controller to be configured first.

Related Links

CPU Interrupt Controller (CPUINT)
SREG
Interrupts

When the entire frame in the Shift register has been shifted out and there is no new data present in the transmit buffer, the Transmit Complete Interrupt Flag (TXCIF in USARTn.STATUS) is set and the optional interrupt is generated.

TXDATA can only be written when the Data Register Empty Flag (DREIF in USARTn.STATUS) is set, indicating that the register is empty and ready for new data.

When using frames with fewer than eight bits, the Most Significant bits written to TXDATA are ignored. If 9-bit characters are used, DATA[8] in USARTn.TXDATAH has to be written before DATA[7:0] in USARTn.TXDATAL.

Disabling the Transmitter

A disabling of the transmitter will not become effective until ongoing and pending transmissions are completed; i.e. when the Transmit Shift register and Transmit Buffer register do not contain data to be transmitted. When the transmitter is disabled, it will no longer override the TxDn pin, and the pin direction is set as input automatically by hardware, even if it was configured as output by the user.

23.3.2.4 Data Reception - USART Receiver

When the receiver is enabled, the RxD pin functions as the receiver's serial input. The direction of the pin n must be set as an input in the Direction register of the Port (PORTx.DIR[n]=0), which is the default pin setting.

Receiving Frames

The receiver starts data reception when it detects a valid Start bit. Each bit that follows the Start bit will be sampled at the baud rate or XCK clock, and shifted into the Receive Shift register until the first Stop bit of a frame is received. A second Stop bit will be ignored by the receiver. When the first Stop bit is received and a complete serial frame is present in the Receive Shift register, the contents of the Shift register will be moved into the receive buffer. The receive complete interrupt flag (RXCIF in USARTn.STATUS) is set, and the optional interrupt is generated.

The receiver buffer can be read by reading RXDATA, comprising of DATA[7:0] in USARTn.RXDATAL, and DATA[8] in USARTn.RXDATAH. RXDATA should not be read unless the Receive Complete Interrupt Flag (RXCIF in USARTn.STATUS) is set. When using frames with fewer than eight bits, the unused Most Significant bits are read as zero. If 9-bit characters are used, the ninth bit (DATA[8] in USARTn.RXDATAH) must be read before the low byte (DATA[7.0] in USARTn.RXDATAL).

Receiver Error Flags

The USART receiver has three error flags in the Receiver Data Register High Byte register (USARTn.RXDATAH):

- Frame Error (FERR)
- Buffer Overflow (BUFOVF)
- Parity Error (PERR)

The error flags are located in the receive FIFO buffer together with their corresponding frame. Due to the buffering of the error flags, the USARTn.RXDATAH must be read before the USARTn.RXDATAL, since reading the USARTn.RXDATAL changes the FIFO buffer.

Parity Checker

When enabled, the parity checker calculates the parity of the data bits in incoming frames and compares the result with the parity bit of the corresponding frame. If a parity error is detected, the Parity Error flag (PERR in USARTn.RXDATAH) is set.

If USART LIN mode is enabled (by writing RXMODE to '1' in USARTn.CTRLB), a parity check is only performed on the protected identifier field. A parity error is detected if one of the equations below is not true which sets PERR in USARTn.RXDATAH.

23.5.1 Receiver Data Register Low Byte

Name: RXDATAL
Offset: 0x00
Reset: 0x00
Property: R

Reading the USARTn.RXDATAL Register will return the contents of the Receive Data Buffer register (RXB).
The receive buffer consists of a two-level FIFO. The FIFO and the corresponding flags in the high byte of RXDATA will change state whenever the receive buffer is accessed (read). If CHSIZE in USARTn.CTRLC is set to 9BIT Low byte first, read USARTn.RXDATAL before USARTn.RXDATAH. Otherwise, always read USARTn.RXDATAH before USARTn.RXDATAL in order to get the correct flags.

Bit	7	6	5	4	3	2	1	0
	DATA[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – DATA[7:0] Receiver Data Register

23.5.5 USART Status Register

Name: STATUS
Offset: 0x04
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	RXCIF	TXCIF	DREIF	RXSIF	ISFIF		BDF	WFB
Access	R	R/W	R	R/W	R/W		R/W	R/W
Reset	0	0	0	0	0		0	0

Bit 7 – RXCIF USART Receive Complete Interrupt Flag
This flag is set to ‘1’ when there is unread data in the receive buffer and cleared when the receive buffer is empty (i.e. does not contain any unread data). When the receiver is disabled, the receive buffer will be flushed and consequently, the RXCIF will become '0'.

When interrupt-driven data reception is used, the receive complete interrupt routine must read the received data from RXDATA in order to clear the RXCIF. If not, a new interrupt will occur directly after the return from the current interrupt.

Bit 6 – TXCIF USART Transmit Complete Interrupt Flag
This flag is set when the entire frame in the Transmit Shift register has been shifted out and there are no new data in the transmit buffer (TXDATA).

This flag is automatically cleared when the transmit complete interrupt vector is executed. The flag can also be cleared by writing a ‘1’ to its bit location.

Bit 5 – DREIF USART Data Register Empty Flag
The DREIF indicates if the transmit buffer (TXDATA) is ready to receive new data. The flag is set to ‘1’ when the transmit buffer is empty and is ‘0’ when the transmit buffer contains data to be transmitted that has not yet been moved into the Shift register. DREIF is set after a Reset to indicate that the transmitter is ready. Always write this bit to ‘0’ when writing the STATUS register.

DREIF is cleared to ‘0’ by writing TXDATAL. When interrupt-driven data transmission is used, the Data Register Empty interrupt routine must either write new data to TXDATA in order to clear DREIF or disable the Data Register Empty interrupt. If not, a new interrupt will occur directly after the return from the current interrupt.

Bit 4 – RXSIF USART Receive Start Interrupt Flag
The RXSIF flag indicates a valid Start condition on RxD line. The flag is set when the system is in standby modes and a high (IDLE) to low (START) valid transition is detected on the RxD line. If the start detection is not enabled, the RXSIF will always be read as '0'. This flag can only be cleared by writing a ‘1’ to its bit location. This flag is not used in the Master SPI mode operation.

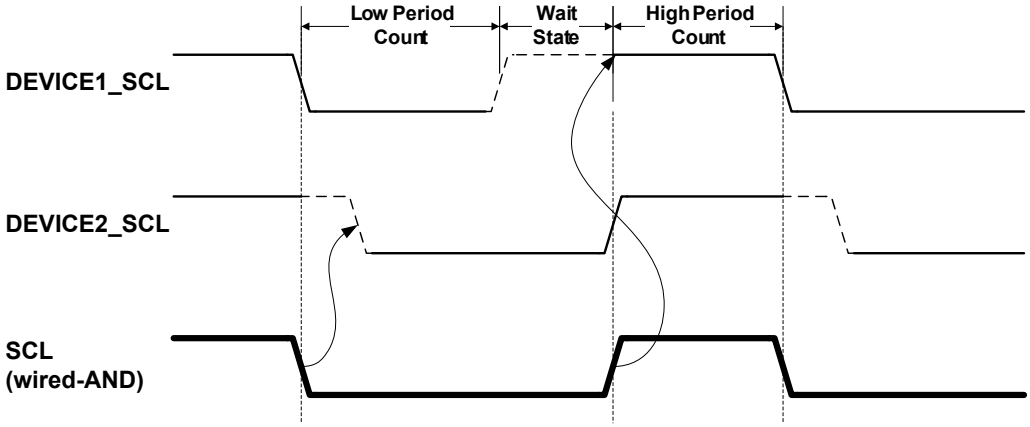
Bit 3 – ISFIF Inconsistent Sync Field Interrupt Flag
This bit is set when the auto-baud is enabled and the sync field bit time is too fast or too slow to give a valid baud setting. It will also be set when USART is set to LINAUTO mode and the SYNC character differ from data value 0x55.

Writing a ‘1’ to this bit will clear the flag and bring the USART back to Idle state.

Value	Name	Description
0x2	GENAUTO	Generic Auto-baud mode
0x3	LINAUTO	LIN Constrained Auto-baud mode

Bit 0 – MPCM Multi-Processor Communication Mode
Writing a ‘1’ to this bit enables the Multi-Processor Communication mode: the USART receiver ignores all the incoming frames that do not contain address information. The transmitter is unaffected by the MPCM setting. For more detailed information see Multiprocessor Communication Mode.

Figure 25-11. Clock Synchronization



A high-to-low transition on the SCL line will force the line low for all masters on the bus, and they will start timing their low clock period. The timing length of the low clock period can vary among the masters. When a master (DEVICE1 in this case) has completed its low period, it releases the SCL line. However, the SCL line will not go high until all masters have released it. Consequently, the SCL line will be held low by the device with the longest low period (DEVICE2). Devices with shorter low periods must insert a wait state until the clock is released. All masters start their high period when the SCL line is released by all devices and has gone high. The device, which first completes its high period (DEVICE1), forces the clock line low, and the procedure is then repeated. The result is that the device with the shortest clock period determines the high period, while the low period of the clock is determined by the device with the longest clock period.

25.3.3 TWI Bus State Logic

The bus state logic continuously monitors the activity on the TWI bus lines when the master is enabled. It continues to operate in all Sleep modes, including power-down.

The bus state logic includes Start and Stop condition detectors, collision detection, inactive bus time-out detection, and a bit counter. These are used to determine the bus state. The software can get the current bus state by reading the Bus State bits in the master STATUS register. The bus state can be unknown, idle, busy, or owner, and is determined according to the state diagram shown in Figure 25-12. The values of the Bus State bits according to state, are shown in binary in the figure below.

28.2.3.4 Events

The events of this peripheral are connected to the Event System.

28.2.3.5 Debug Operation

This peripheral is unaffected by entering Debug mode.

If the peripheral is configured to require periodical service by the CPU through interrupts or similar, improper operation or data loss may result during halted debugging.

28.3 Functional Description

28.3.1 Initialization

For basic operation, follow these steps:

- Configure the desired input pins in the port peripheral
- Select the positive and negative input sources by writing the Positive and Negative Input MUX Selection bit fields (MUXPOS and MUXNEG) in the MUX Control A register (AC.MUXCTRLA)
- Optional: Enable the output to pin by writing a '1' to the Output Pad Enable bit (OUTEN) in the Control A register (AC.CTRLA)
- Enable the AC by writing a '1' to the ENABLE bit in AC.CTRLA

During the start-up time after enabling the AC, the output of the AC may be invalid.

The start-up time of the AC by itself is at most 2.5 µs. If an internal reference is used, the reference start-up time is normally longer than the AC start-up time. The VREF start-up time is 60 µs at most.

28.3.2 Operation

28.3.2.1 Input Hysteresis

Applying an input hysteresis helps to prevent constant toggling of the output when the noise-afflicted input signals are close to each other.

The input hysteresis can either be disabled or have one of three levels. The hysteresis is configured by writing to the Hysteresis Mode Select bit field (HYSMODE) in the Control A register (ACn.CTRLA).

28.3.2.2 Input Sources

The AC has one positive and one negative input. The inputs can be pins and internal sources, such as a voltage reference.

Each input is selected by writing to the Positive and Negative Input MUX Selection bit field (MUXPOS and MUXNEG) in the MUX Control A register (AC.MUXTRLA).

Pin Inputs

The following Analog input pins on the port can be selected as input to the analog comparator:

- AINN0
- AINP0

Internal Inputs

One internal input is available for the analog comparator:

- AC voltage reference

28.3.2.3 Low-Power Mode

For power sensitive applications, the AC provides a Low-Power mode with reduced power consumption and increased propagation delay.

28.5.4 Status

Name: STATUS
Offset: 0x07
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
				STATE				CMP
Access				R				R/W
Reset				0				0

Bit 4 – STATE Analog Comparator State
This shows the current status of the OUT signal from the AC. This will have a synchronizer delay to get updated in the I/O register (three cycles).

Bit 0 – CMP Analog Comparator Interrupt Flag
This is the interrupt flag for AC. Writing a '1' to this bit will clear the Interrupt Flag.

29.5.10 Interrupt Control

Name: INTCTRL
Offset: 0x0A
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
							WCOMP	RESRDY
Access							R/W	R/W
Reset							0	0

Bit 1 – WCOMP Window Comparator Interrupt Enable
Writing a '1' to this bit enables window comparator interrupt.

Bit 0 – RESRDY Result Ready Interrupt Enable
Writing a '1' to this bit enables result ready interrupt.

30.5.3 Control A

Name: CTRLA
Offset: 0x02
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	IBDLY		PARD	DTD	RSD	GTVAL[2:0]		
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit 7 – IBDLY Inter-Byte Delay Enable
Writing a '1' to this bit enables a fixed inter-byte delay between each data byte transmitted from the UPDI when doing multi-byte LD(S). The fixed length is two IDLE characters. Before the first transmitted byte, the regular GT delay used for direction change will be used.

Bit 5 – PARD Parity Disable
Writing this bit to '1' will disable parity detection in the UPDI by ignoring the Parity bit. This feature is recommended only during testing.

Bit 4 – DTD Disable Time-out Detection
Setting this bit disables the time-out detection on the PHY layer, which requests a response from the ACC layer within a specified time (65536 UPDI clock cycles).

Bit 3 – RSD Response Signature Disable
Writing a '1' to this bit will disable any response signatures generated by the UPDI. This is to reduce the protocol overhead to a minimum when writing large blocks of data to the NVM space. Disabling the Response Signature should be used with caution, and only when the delay experienced by the UPDI when accessing the system bus is predictable, otherwise loss of data may occur.

Bits 2:0 – GTVAL[2:0] Guard Time Value
This bit field selects the Guard Time Value that will be used by the UPDI when the transmission mode switches from RX to TX.

Value	Description
0x0	UPDI Guard Time: 128 cycles (default)
0x1	UPDI Guard Time: 64 cycles
0x2	UPDI Guard Time: 32 cycles
0x3	UPDI Guard Time: 16 cycles
0x4	UPDI Guard Time: 8 cycles
0x5	UPDI Guard Time: 4 cycles
0x6	UPDI Guard Time: 2 cycles
0x7	GT off (no extra Idle bits inserted)

31.15 ADC

Operating conditions:

- V_{DD} = 1.8 to 5.5V
- Temperature = -40°C to 125°C
- DUTYCYC = 25%
- CLK_{ADC} = 13 * f_{ADC}
- SAMPCAP is 10 pF for 0.55V reference, while it is set to 5 pF for V_{REF}≥1.1V
- Applies for all allowed combinations of V_{REF} selections and Sample Rates unless othervise noted

Table 31-22. Power Supply, Reference, and Input Range

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		1.8	-	5.5	V
V_{REF}	Reference voltage	REFSEL = Internal reference	0.55	-	V_{DD}-0.4	V
		REFSEL = V_{DD}	1.8	-	5.5	
C_{IN}	Input capacitance	SAMPCAP=5 pF	-	5	-	pF
		SAMPCAP=10 pF	-	10	-	
V_{IN}	Input voltage range		0	-	V_{REF}	V
I_{BAND}	Input bandwidth	1.1V≤V_{REF}	-	-	57.5	kHz

Table 31-23. Clock and Timing Characteristics

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
f_{ADC}	Sample rate	1.1V≤V_{REF}	15	-	115	ksps
		1.1V≤V_{REF} (8-bit resolution)	15	-	150	
		V_{REF}=0.55V (10 bits)	7.5	-	20	
CLK_{ADC}	Clock frequency	V_{REF}=0.55V (10 bits)	100	-	260	kHz
		1.1V≤V_{REF} (10 bits)	200	-	1500	
		1.1V≤V_{REF} (8-bit resolution)	200	-	2000	
Ts	Sampling time		2	2	33	CLK_{ADC} cycles
T_{CONV}	Conversion time (latency)	Sampling time = 2 CLK_{ADC}	8.7	-	50	µs
T_{START}	Start-up time	Internal V_{REF}	-	22	-	µs

Table 31-24. Accuracy Characteristics(2)

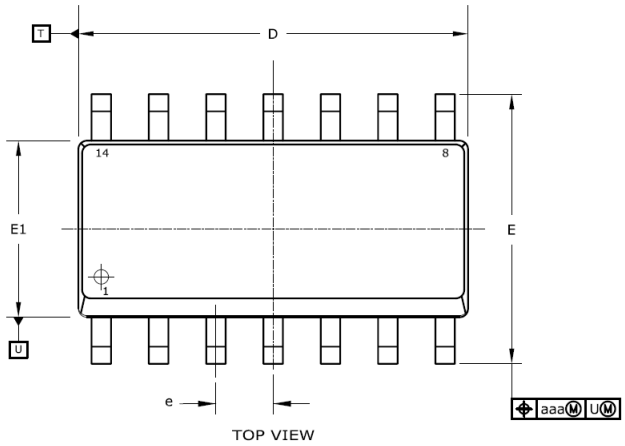
Symbol	Description	Conditions		Min.	Typ.	Max.	Unit
Res	Resolution			-	10	-	bit
INL	Integral Non-linearity	REFSEL = INTERNAL	f_{ADC}=7.7 ksps	-	1.0	-	

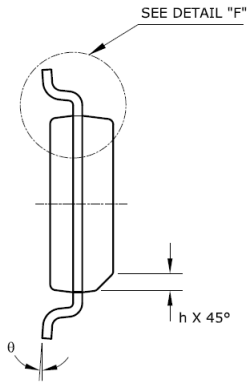
34. Package Drawings

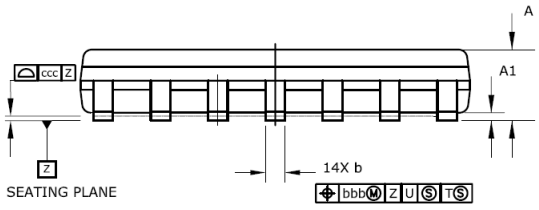
34.1 14-Pin SOIC150

For the most current package drawings, see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

DRAWINGS NOT SCALED



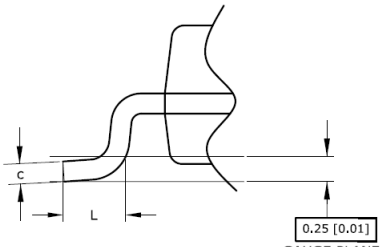




COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	1.60	1.75	
A1	0.10	----	0.25	
D	8.55	8.65	8.75	2
E	5.80	6.00	6.20	
E1	3.80	3.90	4.00	3
L	0.40	----	1.27	
b	0.33	----	0.51	4
c	0.19	-----	0.25	
e	1.27 BSC			
h	0.25	-----	0.50	
θ	0°	-----	8°	
TOLERANCES OF FORM AND POSITION				
aaa	0.25			
bbb	0.25			
ccc	0.10			
n	14			



Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MS-012, Variation AB.
2. Dimensions D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shal not exceed 0.15mm (0.006 In) per side.
3. Dimensions E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010 in) per side.
4. Dimensions b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.10mm total In excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.

01/31/2014

Atmel	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: **packagedrawings@atmel.com**	TU, 14 Lds - 1.27mm Pitch, 8.65X3.90x1.60mm Body Size Plastic Small Outline Package (SOIC)	SVQ	TU	D

38. Acronyms and Abbreviations

The table below contains acronyms and abbreviations used in this document.

Table 38-1. Acronyms and Abbreviations

Abbreviation	Description
AC	Analog Comparator
ACK	Acknowledge
ADC	Analog-to-Digital Converter
ADDR	Address
AES	Advanced Encryption Standard
ALU	Arithmetic Logic Unit
AREF	Analog reference voltage, also VREFA
BLB	Boot Lock Bit
BOD	Brown-out Detector
CAL	Calibration
CCMP	Compare/Capture
CCL	Configurable Custom Logic
CCP	Configuration Change Protection
CLK	Clock
CLKCTRL	Clock Controller
CRC	Cyclic Redundancy Check
CTRL	Control
DAC	Digital-to-Analog Converter
DFLL	Digital Frequency Locked Loop
DMAC	DMA (Direct Memory Access) Controller
DNL	Differential Nonlinearity (ADC characteristics)
EEPROM	Electrically Erasable Programmable Read-Only Memory
EVSYS	Event System
GND	Ground
GPIO	General Purpose Input/Output
I^2C	Inter-Integrated Circuit
IF	Interrupt flag
INL	Integral Nonlinearity (ADC characteristics)