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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, Serial Port
Peripherals	POR, PWM, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78erd2a40fl

1. GENERAL DESCRIPTION

The W78ERD2 is an 8-bit microcontroller which is pin- and instruction-set-compatible with the standard 80C52. The W78ERD2 contains a 64-KB Flash EPROM whose contents may be updated in-system by a loader program stored in an auxiliary, 4-KB Flash EPROM. Once the contents are confirmed, it can be protected for security.

The W78ERD2 also contains 256 bytes of on-chip RAM; 1 KB of auxiliary RAM; four 8-bit, bi-directional and bit-addressable I/O ports; an additional 4-bit port P4; three 16-bit timer/counters; and a serial port. These peripherals are all supported by nine interrupt sources with 4 levels of priority.

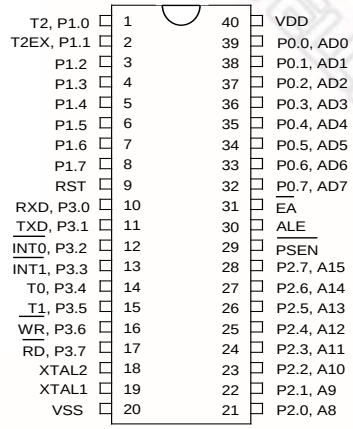
The W78ERD2 has two power-reduction modes: idle mode and power-down mode, both of which are software-selectable. Idle mode turns off the processor clock but allows peripherals to continue operating, while power-down mode stops the crystal oscillator for minimum power consumption. Power-down mode can be activated at any time and in any state without affecting the processor.

2. FEATURES

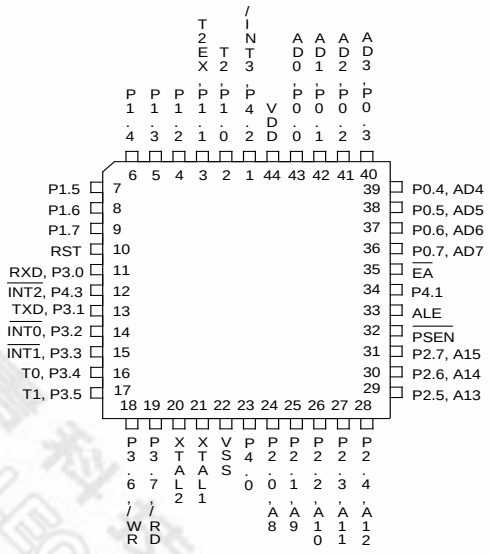
- 8-bit CMOS microcontroller
- Pin-compatible with standard 80C52
- Instruction-set compatible with 80C52
- Four 8-bit I/O ports; Port 0 has internal pull-up resisters enabled by software.
- One extra 4-bit I/O port with interrupt and chip-select functions
- Three 16-bit timers
- Programmable clock out
- Programmable Counter Array (PCA) with PWM, Capture, Compare and Watchdog functions
- 9 interrupt sources with 4 levels of priority
- Full-duplex serial port with framing-error detection and automatic address recognition
- 64-KB, in-system-programmable, Flash EPROM (AP Flash EPRAOM)
- 4-KB auxiliary Flash EPROM for loader program (LD Flash EPROM)
- 256-byte on-chip RAM
- 1-KB auxiliary RAM, software-selectable
- Software Reset
- 12 clocks per machine cycle operation (default). Speed up to 40 MHz.
- 6 clocks per machine cycle operation set by the writer. Speed up to 20 MHz.
- 2 DPTR registers
- Low EMI (inhibit ALE)
- Built-in power management with idle mode and power down mode
- Code protection
- Packages:
  - Lead Free (RoHS) DIP 40: W78ERD2A40DL
  - Lead Free (RoHS) PLCC 44: W78ERD2A40PL
  - Lead Free (RoHS) PQFP 44: W78ERD2A40FL

3. PIN CONFIGURATIONS

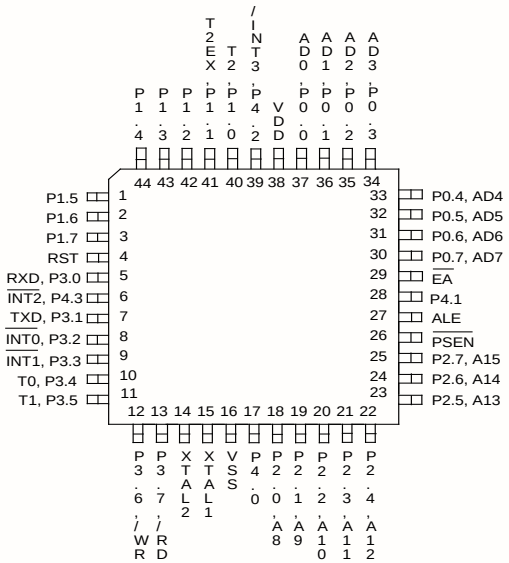
40-Pin DIP



44-Pin PLCC



44-Pin QFP



5. FUNCTIONAL DESCRIPTION

The W78ERD2 architecture consists of a core processor that supports 111 different op-codes and references 64 KB of program space and 64 KB of data space. It is surrounded by various registers; four general-purpose I/O ports; one special-purpose, programmable, 4-bit I/O port; 256 bytes of RAM; 1 KB of auxiliary RAM (AUX-RAM); three timer/counters; a serial port; and an internal 74373 latch and 74244 buffer which can be switched to port 2.

This section introduces the RAM, Timers/Counters, Clock, Power Management, Reduce EMI Emission, and Reset.

5.1 RAM

The W78ERD2 has two banks of RAM: 256 bytes of RAM and 1 KB of AUX-RAM. AUX-RAM is enabled by clearing bit 1 in the AUXR register, and it is enabled after reset. Different addresses in RAM are addressed in different ways.

- RAM 00H – 7FH can be addressed directly or indirectly, as in the 8051. The address pointers are R0 and R1 of the selected bank.
- RAM 80H – FFH can only be addressed indirectly, as in the 8051. The address pointers are R0 and R1 of the selected bank.
- AUX-RAM 00H –3FFH is addressed indirectly in the same way external data memory is accessed with the MOVX instruction. The address pointers are R0 and R1 of the selected bank and the DPTR register.
- Addresses higher than 3FFH are stored in external memory and are accessed indirectly with the MOVX instruction, as in the 8051.

When AUX-RAM is enabled, the instruction "MOVX @Ri" always accesses AUX-RAM. When the W78ERD2 is executing instructions from internal program memory, accessing AUX-RAM does not affect ports P0, P2, $\overline{WR}$ or $\overline{RD}$.

For example,

```
ANL   AUXR,#11111101B  ; Enable AUX-RAM
MOV   DPTR,#1234H
MOV   A,#56H
MOVX  @DPTR,A          ; Write 56h to address 1234H in external memory
MOV   XRAMAH,#02H      ; Only 2 LSB effective
MOV   R0,#34H
MOV   A,@R0            ; Read AUX-RAM data at address 0234H
```

5.2 Timers/Counters

The W78ERD2 has three timers/counters called Timer 0, Timer 1, and Timer 2. Each timer/counter consists of two 8-bit data registers: TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2.

The operations of Timer 0 and Timer 1 are similar to those in the W78C52, and these timers are controlled by the TCON and TMOD registers.

BIT	NAME	FUNCTION
7	TF1	Timer 1 overflow flag: This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. It can also be set or cleared by software.
6	TR1	1: Turn on Timer 1. 0: Turn off Timer 1.
5	TF0	Timer 0 overflow flag: This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. It can also be set or cleared by software.
4	TR0	1: Turn on Timer 0. 0: Turn off Timer 0.
3	IE1	Interrupt 1 Edge Detect: This bit is set by the hardware when a falling-edge / low-level is detected on $\overline{INT1}$. If $\overline{INT1}$ is edge-triggered, this bit is cleared by the hardware when the interrupt service routine begins. Otherwise, it follows the pin.
2	IT1	Interrupt 1 type control 1: Interrupt 1 is triggered by a falling-edge on $\overline{INT1}$. 0: Interrupt 1 is triggered by a low-level on $\overline{INT1}$.
1	IE0	Interrupt 0 Edge Detect: This bit is set by the hardware when a falling-edge / low-level is detected on $\overline{INT0}$. If $\overline{INT0}$ is edge-triggered, this bit is cleared by the hardware when the interrupt service routine begins. Otherwise, it follows the pin.
0	IT0	Interrupt 0 type control 1: Interrupt 0 is triggered by a falling-edge on $\overline{INT0}$. 0: Interrupt 0 is triggered by a low-level on $\overline{INT0}$.

Timer Mode Control

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/Counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 is set.
6	C/$\overline{T}$	Timer or Counter Select: When cleared, Timer 1 is incremented by the internal clock. When set, Timer 1 counts falling edges on the T1 pin.
5	M1	Timer 1 Mode Select bits: See below.
4	M0	Timer 1 Mode Select bits: See below.

Timer 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

TH1.7-0: Timer 1 High byte

Auxiliary Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	EXTRAM	ALEOFF

Mnemonic: AUXR Address: 8Eh

BIT	NAME	FUNCTION
7~2	-	Reserve
1	EXTRAM	0 = Enable AUX-RAM 1 = Disable AUX-RAM
0	ALEOFF	0: ALE expression is enabled. 1: ALE expression is disabled.

Port 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7-0: General-purpose input/output port. Port-read instructions read the port pins, while read-modify-write instructions read the port latch.

Port 4.1 Low Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P41AL.7	P41AL.6	P41AL.5	P41AL.4	P41AL.3	P41AL.2	P41AL.1	P41AL.0

Mnemonic: P41AL Address: 94h

Port 4.1 High Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P41AH.7	P41AH.6	P41AH.5	P41AH.4	P41AH.3	P41AH.2	P41AH.1	P41AH.0

Mnemonic: P41AH Address: 95h

BIT	NAME	FUNCTION
7	W: SWRESET R: REBOOT	When FBOOTSL and FPROGEN are set to 1, set this bit to 1 to force the microcontroller to reset to the initial condition, just like power-on reset. This action re-boots the microcontroller and starts normal operation. Read this bit to determine whether or not a hardware reboot is in progress.
6 – 2	-	Reserved
1	FBOOTSL	Program Location Selection. This bit should be set before entering ISP mode. 0: The Loader Program is in the 64-KB AP Flash EPROM. The 4-KB LD Flash EPROM is the destination for re-programming. 1: The Loader Program is in the 4-KB memory bank. The 64-KB AP Flash EPROM is the destination for re-programming.
0	FPROGEN	FLASH EPROM Programming Enable. 1: Enable in-system programming mode. In this mode, erase, program and read operations are achieved during device enters idle state. 0: Disable in-system programming mode. The on-chip flash memory is read-only.

CHPCON has an unrestricted read access, however, the write access is protected by timed-access protection. See the section of timed-access protection for more information.

External Interrupt Control

Bit:	7	6	5	4	3	2	1	0
	PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

Mnemonic: XICON Address: C0h

BIT	NAME	FUNCTION
7	PX3	1: Set the priority of external interrupt $\overline{INT3}$ one level higher.
6	EX3	1: Enable external interrupt $\overline{INT3}$.
5	IE3	Interrupt $\overline{INT3}$ flag. This bit is set and cleared automatically by the hardware when the interrupt is detected and processed.
4	IT3	1: $\overline{INT3}$ is falling-edge triggered 0: $\overline{INT3}$ is low-level triggered
3	PX2	1: Set the priority of external interrupt $\overline{INT2}$ one level higher.
2	EX2	1: Enable external interrupt $\overline{INT2}$.
1	IE2	Interrupt $\overline{INT2}$ flag. This bit is set and cleared automatically by the hardware when the interrupt is detected and processed.
0	IT2	1: $\overline{INT2}$ is falling-edge triggered 0: $\overline{INT2}$ is low-level triggered

External Interrupt High Control

Bit:	7	6	5	4	3	2	1	0
	PXH3	-	-	-	PXH2	-	-	-

Mnemonic: XICONH Address: C1h

BIT	NAME	FUNCTION
7	PXH3	1: Set the priority of external interrupt $\overline{INT3}$ to the highest level.
6 - 4	-	Reserved
3	PXH2	1: Set the priority of external interrupt $\overline{INT2}$ to the highest level.
2 - 0	-	Reserved

Port 4 Control Register A

Bit:	7	6	5	4	3	2	1	0
	P41FUN1	P41FUN0	P41CMP1	P41CMP0	P40FUN1	P40FUN0	P40CMP1	P40CMP0

Mnemonic: P4CONA Address: C2h

BIT	NAME	FUNCTION
7, 6	P41FUN1 P41FUN0	P4.1 function control bits, similar to P43FUN1 and P43FUN0 below.
5, 4	P41CMP1 P41CMP0	P4.1 address-comparator length control bits, similar to P43CMP1 and P43CMP0 below.
3, 2	P40FUN1 P40FUN0	P4.0 function control bits, similar to P43FUN1 and P43FUN0 below.
1, 0	P40CMP1 P40CMP0	P4.0 address-comparator length control bits, similar to P43CMP1 and P43CMP0 below.

Port 4 Control Register B

Bit:	7	6	5	4	3	2	1	0
	P43FUN1	P43FUN0	P43CMP1	P43CMP0	P42FUN1	P42FUN0	P42CMP1	P42CMP0

Mnemonic: P4CONB Address: C3h

```
MOV  P40AH, #12H
MOV  P40AL, #34H            ; Base I/O address 1234H for P4.0
MOV  P4CONA, #00001010B     ; P4.0 is a write-strobe signal; address lines A0 and A1 are masked.
MOV  P4CONB, #00H           ; P4.1 – P4.3 are general I/O ports
MOV  P2ECON, #10H           ; Set P40SINV to 1 to invert the P4.0 write-strobe to positive polarity.
```

Then, any instruction MOVX @DPTR, A (where DPTR is in 1234H – 1237H) generates a positive-polarity, write-strobe signal on pin P4.0, while the instruction MOV P4, #XX puts bits 3 – 1 of data #XX on pins P4.3 – P4.1.

9. PROGRAMMABLE TIMERS/COUNTERS

The W78ERD2 has three 16-bit programmable timer/counters.

Time-Base Selection

The W78ERD2 offers two speeds for the timer. The timers can count at 1/12 of the clock, the same speed they have in the standard 8051 family. Alternatively, the timers can count at 1/6 of the clock, called turbo mode. The speed is controlled by bits T0M, T1M and T2M bits in CKCON. The default value is zero, which selects 1/12 of the clock. These 3 bits, T0M, T1M and T2M, have no effect if option bit 3 is set to 1 to select 12 clocks / machine cycle.

9.1 Timer 0 and Timer 1

Timers 0 and 1 each have a 16-bit timer/counter which consists of two eight-bit registers: Timer 0 consists of TH0 (8 MSB) and TL0 (8 LSB), and Timer 1 consists of TH1 and TL1.

These timers/counters can be configured to operate either as timers, machine–cycle counters or counters based on external inputs. The "Timer" or "Counter" function itself is selected by the corresponding "$C/\overline{T}$" bit in the TMOD register: bit 2 for Timer 0 and bit 6 for Timer 1. In addition, each timer/counter can operate in one of four possible modes, which are selected by bits M0 and M1 in TMOD.

The rest of this section explains the time-base for the timers and then introduces each mode.

Mode 0

In mode 0, the timer/counter is a 13-bit counter whose eight MSB are in THx and five LSB are the five lower bits in TLx. The upper three bits in TLx are ignored. Because THx and TLx are read separately, the timer/counter acts like an eight-bit counter with a five-bit, divide-by-32 pre-scale.

Counting is enabled only when TRx is set and either GATE = 0 or $\overline{INTx}$ = 1. What the timer/counter counts depends on $C/\overline{T}$. When $C/\overline{T}$ is set to 0, the timer/counter counts the negative edges of the clock according to the time-base selected by bits TxM in CKCON. When $C/\overline{T}$ is set to 1, it counts falling edges on T0 (P3.4, for Timer 0) or T1 (P3.5, for Timer 1). When the 13-bit counter reaches 1FFFh, the next count rolls over the timer/counter to 0000h, and the timer overflow flag TFx (in TCON) is set. If enabled, an interrupt occurs.

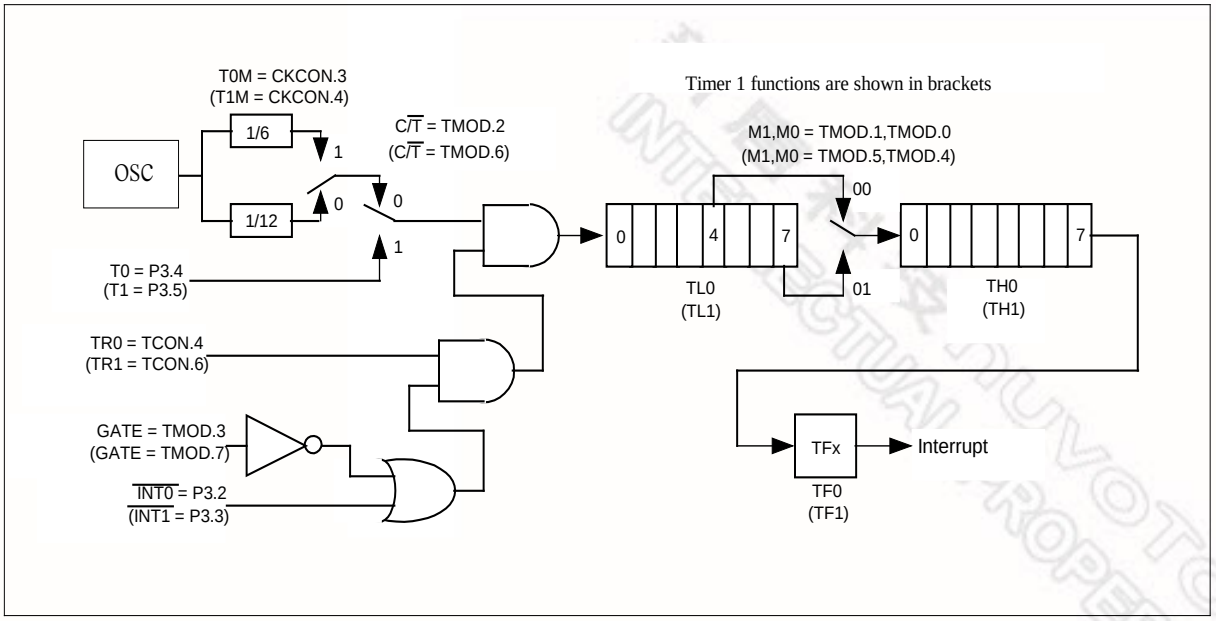


Figure 9-1 Timer/Counter Mode 0 & Mode 1

Mode 1

Mode 1 is similar to mode 0, except that the timer/counter is 16-bit counter, not a 13-bit counter. All the bits in THx and TLx are used. Roll-over occurs when the timer moves from FFFFh to 0000h.

Mode 2

Mode 2 is similar to mode 0, except that TLx acts like an eight-bit counter and THx holds the auto-reload value for TLx. When the TLx register overflows from FFh to 00h, the timer overflow flag TFx bit (in TCON) is set, TLx is reloaded with the contents of THx, and the counting process continues. The reload operation does not affect the THx register.

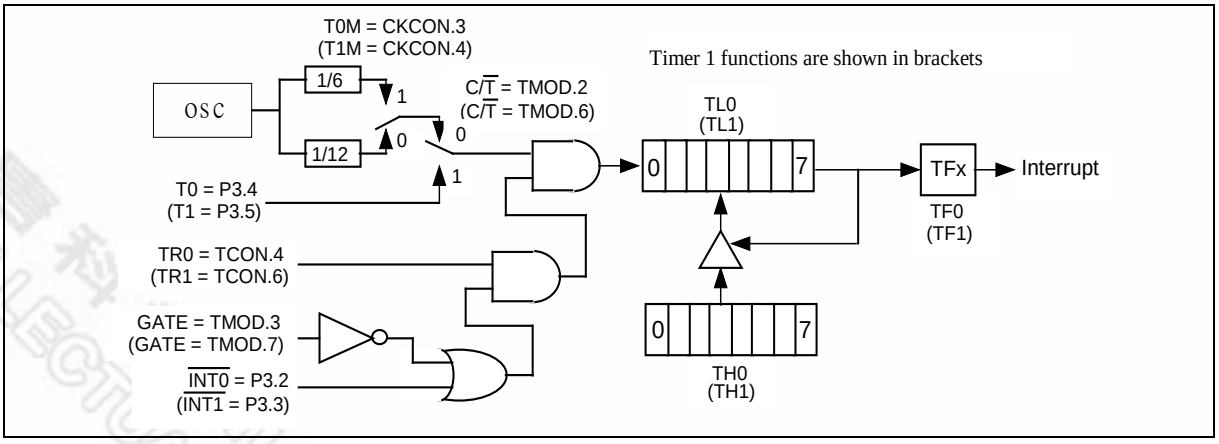


Figure 9-2 Timer/Counter Mode 2

10.5 Framing Error Detection

A frame error occurs when a valid stop bit is not detected. This could indicate incorrect serial data communication. Typically, the frame error is due to noise or contention on the serial communication line. The W78ERD2 has the ability to detect framing errors and set a flag which can be checked by software.

The frame error FE bit is located in SCON.7. This bit is normally used as SM0 in the standard 8051 family. However, in the W78ERD2 it serves a dual function and is called SM0/FE. There are actually two separate flags, one for SM0 and the other for FE. The flag that is actually accessed as SCON.7 is determined by SMOD0 (PCON.6) bit. When SMOD0 is set to 1, then the FE flag is accessed. When SMOD0 is set to 0, then the SM0 flag is accessed.

The FE bit is set to 1 by the hardware but must be cleared by software. Once FE is set, any frames received afterwards, even those without any errors, do not clear the FE flag. The flag has to be cleared by software. Note that SMOD0 must be set to 1 while reading or writing to FE.

10.6 Multi-Processor Communications

Multi-processor communication makes use of the 9th data bit in modes 2 and 3. In the W78ERD2, the RI flag is set only if the received byte corresponds to the Given or Broadcast address. This hardware feature eliminates the software overhead required in checking every received address and greatly simplifies the software programmer task.

In multi-processor communication mode, the address bytes are distinguished from the data bytes by the 9th bit, which is set high for address bytes. When the master processor wants to transmit a block of data to one of the slaves, it first sends out the address of the target slave (or slaves). All the slave processors should have their SM2 bit set high when waiting for an address byte. This ensures that they are interrupted only by the reception of an address byte. The automatic address recognition feature ensures that only the addressed slave is actually interrupted because the address comparison is done by the hardware, not the software.

The addressed slave clears the SM2 bit, thereby clearing the way to receive data bytes. With SM2 = 0, the slave is interrupted on the reception of every single complete frame of data. The unaddressed slaves are not affected, as they are still waiting for their address.

The Master processor can selectively communicate with groups of slaves by using the Given Address. All the slaves can be addressed together using the Broadcast Address. The addresses for each slave are defined in the SADDR and SADEN registers. The slave address is an eight-bit value specified in the SADDR SFR. The SADEN SFR is actually a mask for the byte value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is don't care. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR.

The following example shows how the user can define the Given Address to address different slaves.

for the modules and are set by hardware when either a match or a capture occurs. These flags can only be cleared by software.

The next five sections provide more information about each of the five modes (four modes for all registers and the watchdog timer in module 4).

11.1 PCA Capture Mode

To use one of the PCA modules in capture mode, either one or both of the CCAPM bits CAPN and CAPP for that module must be set.

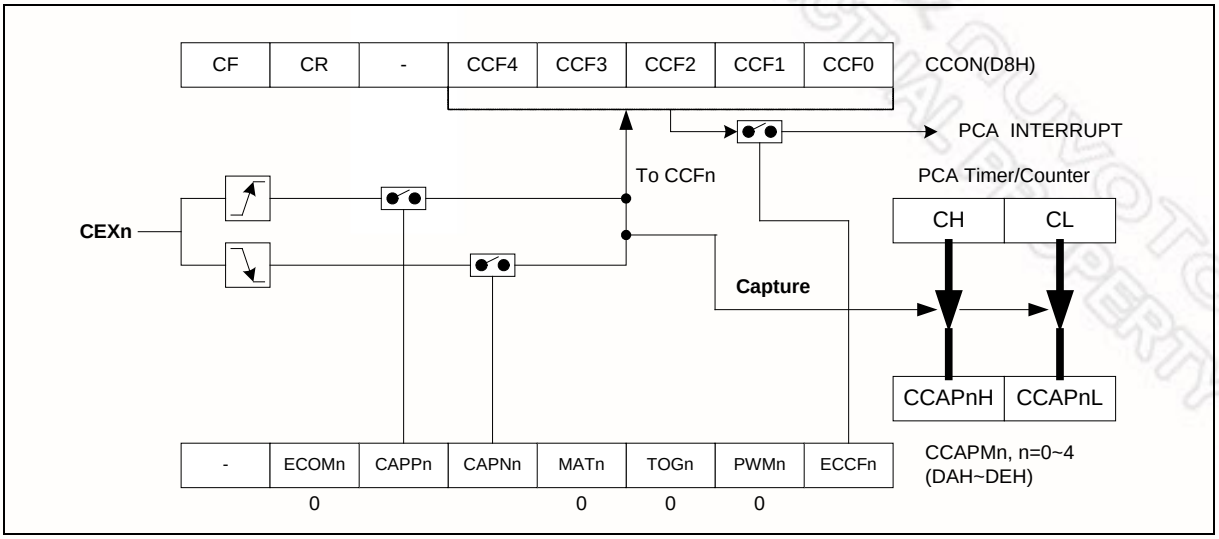


Figure 11-2 PCA Capture Mode

In capture mode, the external CEX*n* input is sampled for a transition. When a valid transition occurs, the PCA hardware loads the value of the PCA counter registers CH and CL into the module's capture registers (CCAPnH and CCAPnL). If the CCFn (CCON) and ECCFn (CCAPMn) bits are set, then an interrupt is generated.

11.2 16-bit Software Timer Comparator Mode

The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the CCAPMn register.

11.4 Pulse Width Modulator Mode

The PWM and ECOM (CCAPM) bits must be set to enable the PWM mode.

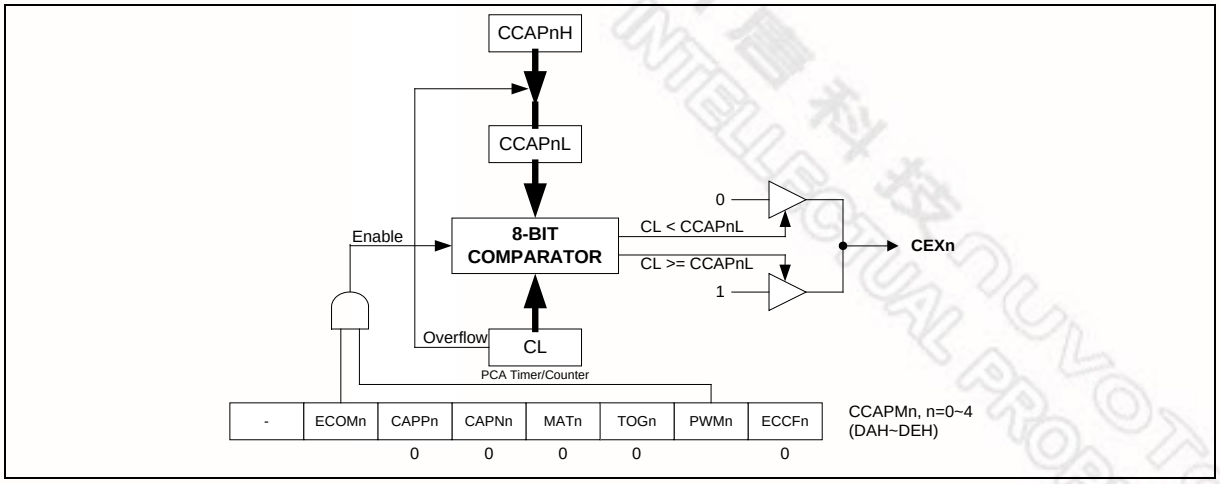


Figure 11-5 PAC PWM Mode

All of the modules have the same frequency because they share the same PCA timer. The duty cycle of each module, however, is independently controlled by the module's capture register CCAPLn. When the value of the PCA CL SFR is less than the value in CCAPLn, the output is low; when it is equal to or greater than the value in CCAPLn, the output is high. When CL overflows from FF to 00, CCAPLn is reloaded with the value in CCAPHn.

11.5 Watchdog Timer

The Watchdog Timer is a free-running timer that serves as a system monitor. It is implemented in module 4, which can still be used for other modes if the Watchdog Timer is not needed.

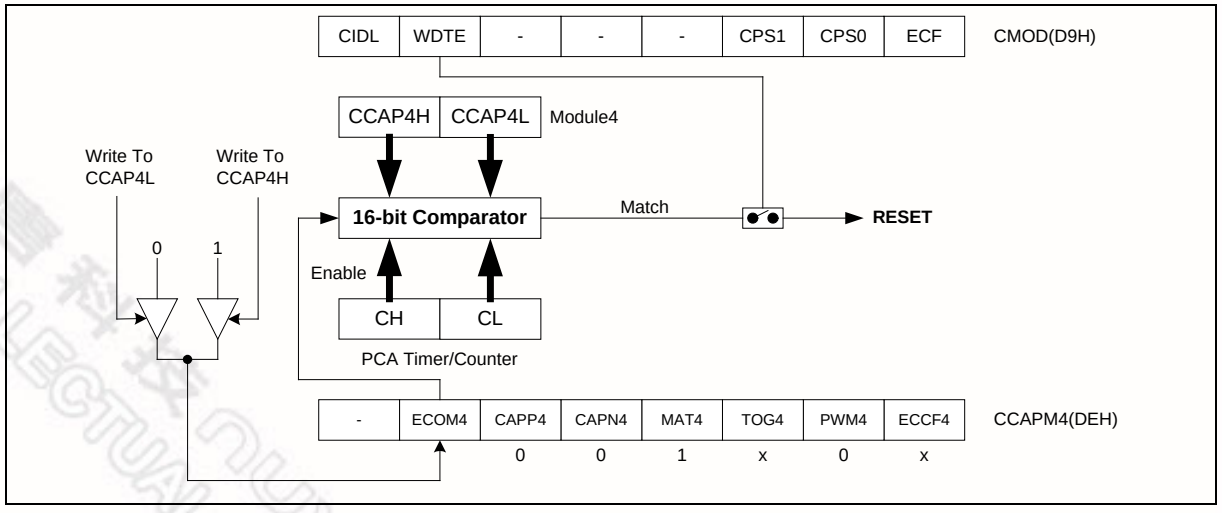


Figure 11-6 PCA Watchdog Timer Mode

The program first loads a 16-bit value into the compare registers. Then, like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match occurs, an internal reset is generated, but it does not make the RST pin go high.

14. TIMED-ACCESS PROTECTION

The W78ERD2 has features like Timer clock selecting by setting CKCON, software reset and ISP function that are crucial to the proper operation of the system. Consequently, The SFR CHPCON and CKCON, which control the functions, have restricted write access to protect CPU from errant operation. The W78ERD2 provides has a timed-access protection scheme that controls write access to critical bits.

In this scheme, protected bits have a timed write-enable window. A write is successful only if this window is active; otherwise, the write is discarded. The write-enable window is opened in two steps. First, the software writes 87h to the register CHPENR. This starts a counter, which expires in three machine cycles. Then, if the software writes 59h to CHPENR before the counter expires, the write-enable window is opened for three machine cycles. After three machine cycles, the window automatically closes, and the procedure must be repeated again to access protected bits.

The suggested code for opening the write-enable window is

```
CHPENR REG 0F6h        ; Define new register CHPENR, located at 0F6h
  MOV CHPENR, #87h
  MOV CHPENR, #59h
```

Five examples, some correct and some incorrect, of using timed-access protection are shown below.

D.C. Electrical Characteristics, continued

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Input High Voltage P0, P1, P2, P3, P4, $\overline{EA}$	V_{IH1}	2.4	V_{DD} +0.2	V	V_{DD} = 5.5V
Input High Voltage RST	V_{IH2}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
Input High Voltage XTAL1[*4]	V_{IH3}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
Output Low Voltage P1, P2, P3, P4	V_{OL1}	-	0.45	V	V_{DD} = 4.5V I_{OL} = +2 mA
Output Low Voltage P0, ALE, $\overline{PSEN}$ [*3]	V_{OL2}	-	0.45	V	V_{DD} = 4.5V I_{OL} = +4 mA
Sink Current P1, P3, P4	Isk1	4	8	mA	V_{DD} = 4.5V V_{IN} = 0.45V
Sink Current P0, P2, ALE, $\overline{PSEN}$	Isk2	10	15	mA	V_{DD} = 4.5V V_{IN} = 0.45V
Output High Voltage P1, P2, P3, P4	V_{OH1}	2.4	-	V	V_{DD} = 4.5V I_{OH} = -100 μA
Output High Voltage P0, ALE, $\overline{PSEN}$ [*3]	V_{OH2}	2.4	-	V	V_{DD} = 4.5V I_{OH} = -400 μA
Source Current P1, P2, P3, P4	Isr1	-180	-300	μA	V_{DD} = 4.5V V_{IN} = 2.4V
Source Current P0, P2, ALE, $\overline{PSEN}$	Isr2	-8	-12	mA	V_{DD} = 4.5V V_{IN} = 2.4V

Notes:

*1. RST pin is a Schmitt-trigger input.

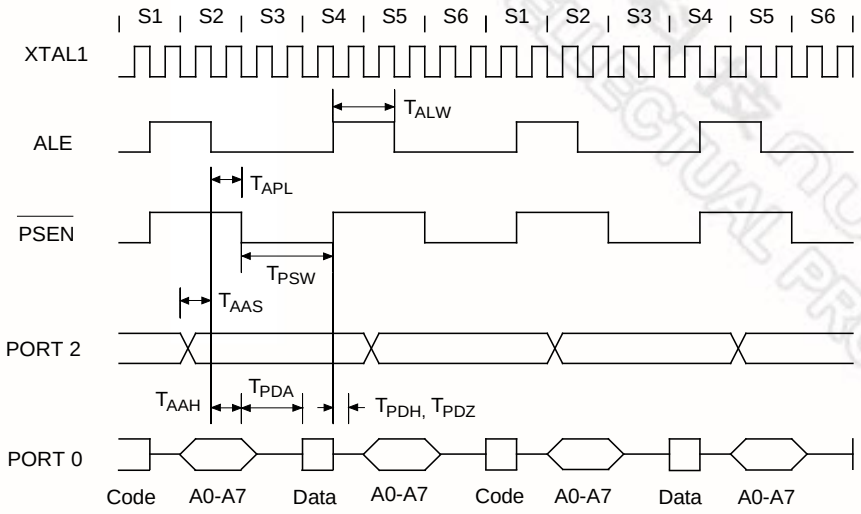
*2. P0, ALE and $\overline{PSEN}$ are tested in external-access mode.

*3. XTAL1 is a CMOS input.

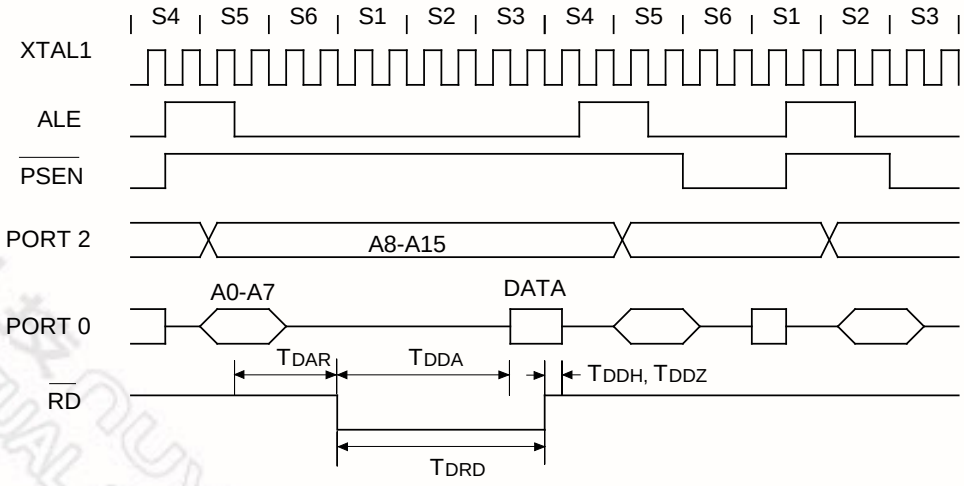
*4. Pins of P1, P2, P3 and P4 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when VIN is approximately 2V.

19. TIMING WAVEFORMS

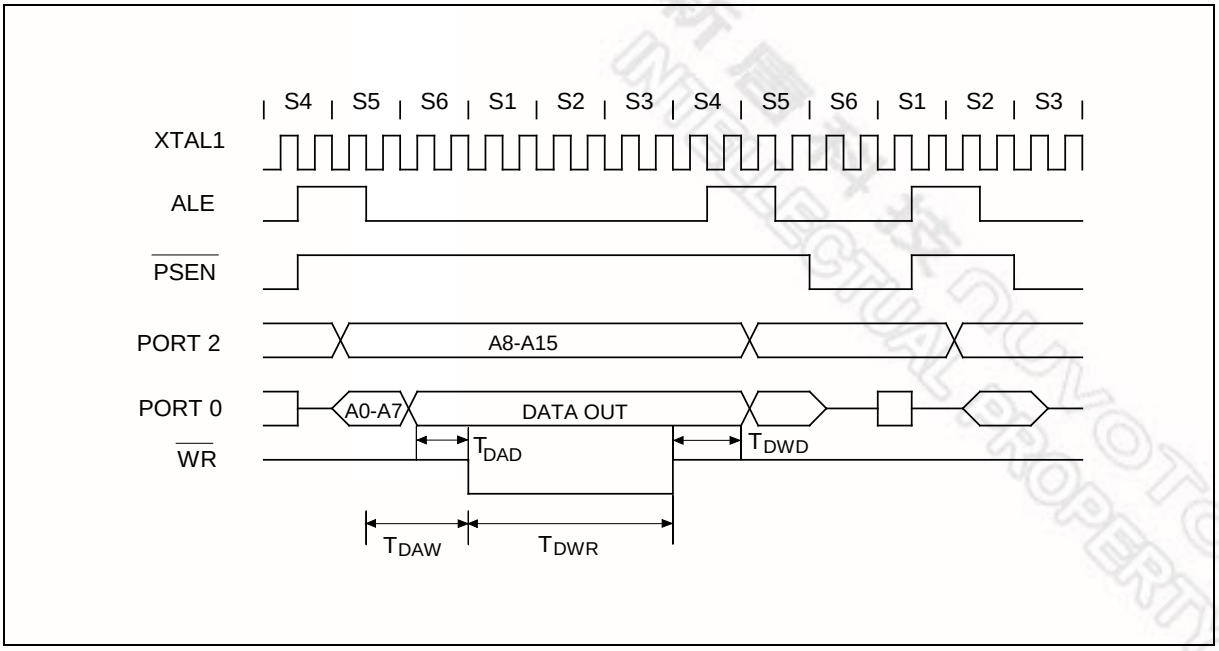
Program Fetch Cycle



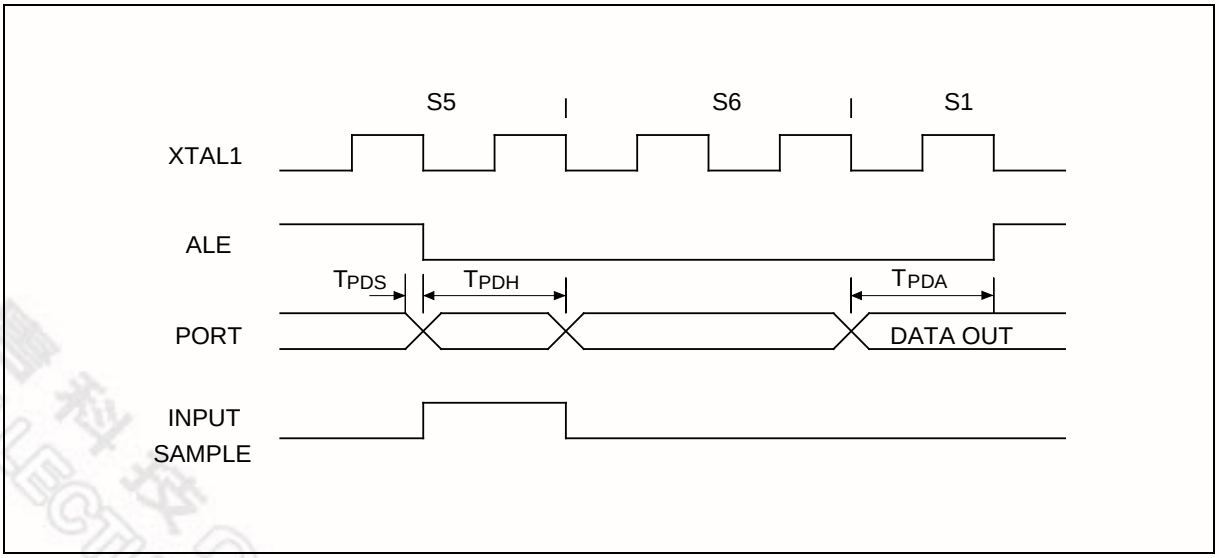
Data Read Cycle



Data Write Cycle



Port Access Cycle



```
        MOV IE, #82H                ; TIMER0 INTERRUPT ENABLE FOR WAKE-UP FROM IDLE MODE
        MOV R6, #F0H                ; TL0 = F0H
        MOV R7, #FFH                ; TH0 = FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV TMOD, #01H              ; TMOD = 01H, SET TIMER0 A 16-BIT TIMER
        MOV TCON, #10H              ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H              ; ENTER IDLE MODE FOR LAUNCHING THE IN-SYSTEM
                                    ; PROGRAMMABILITY
;*****************************************************************************
;* Normal mode 64KB AP Flash EPROM program: depending user's application
;*****************************************************************************
NORMAL_MODE:
        .                           ; User's application program
        .
        .
        .
```

EXAMPLE 2:

```
;*************************************************************************************************************************
;* Example of 4KB LD Flash EPROM program: This loader program will erase the 64KB AP Flash EPROM first,
;* then reads the new code from external SRAM and program them into 64KB AP Flash EPROM bank.
;* XTAL = 40MHz
;*************************************************************************************************************************
    .chip 8052
    .RAMCHK OFF
    .symbols

    CHPCON    EQU    BFH
    CHPENR    EQU    F6H
    SFRAL     EQU    C4H
    SFRAH     EQU    C5H
    SFRFD     EQU    C6H
    SFRCN     EQU    C7H

      ORG    000H
      LJMP   100H               ; JUMP TO MAIN PROGRAM
  ;*************************************************************************
  ;* 1. TIMER0 SERVICE VECTOR ORG = 0BH
  ;*************************************************************************
      ORG 000BH
      CLR  TR0                  ; TR0 = 0, STOP TIMER0
      MOV TL0, R6
      MOV TH0, R7
      RETI
;*************************************************************************
  ;*  4KB LD Flash EPROM MAIN PROGRAM
  ;*************************************************************************
     ORG 100H
MAIN_4K:
      MOV SP, #C0H          ; BE INITIAL SP REGISTER
```

23. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	June 2004	-	Initial Issued
A2	August 2004	38	Modify the content of PCA
		74	Add the application of PCA
A3	Sep. 30, 2004	38	Add Enhanced full duplex serial port with framing error detection and automatic address recognition
A4	April 20, 2005	72	Add Important Notice
A5	June 2, 2005	4	To add Lead Free part No. of packages.
		17	Correct GF3 to GF2 in AUXR1
		22	Correct XICONH
		38	Add Programmable Timers/Counters.
A6	Sep. 5, 2005	-	Re-organize document.
		49	Add a section of timed-access protection
A7	October 2, 2006		Remove block diagram
A8	December 4, 2006	3	Remove all Leaded package parts
A9	December 15, 2006	32	Correct the interrupt vector of INT2 & INT3.
A10	February 14, 2007	46	Correct CMOD(D8h) to CMOD(D9h)
A11	April 22, 2008	8	Update P3 reset state
A12	March 2, 2009	17	Revise P4CSIN description