What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, Serial Port
Peripherals	POR, PWM, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78erd2a40pl

5. FUNCTIONAL DESCRIPTION

The W78ERD2 architecture consists of a core processor that supports 111 different op-codes and references 64 KB of program space and 64 KB of data space. It is surrounded by various registers; four general-purpose I/O ports; one special-purpose, programmable, 4-bit I/O port; 256 bytes of RAM; 1 KB of auxiliary RAM (AUX-RAM); three timer/counters; a serial port; and an internal 74373 latch and 74244 buffer which can be switched to port 2.

This section introduces the RAM, Timers/Counters, Clock, Power Management, Reduce EMI Emission, and Reset.

5.1 RAM

The W78ERD2 has two banks of RAM: 256 bytes of RAM and 1 KB of AUX-RAM. AUX-RAM is enabled by clearing bit 1 in the AUXR register, and it is enabled after reset. Different addresses in RAM are addressed in different ways.

- RAM 00H – 7FH can be addressed directly or indirectly, as in the 8051. The address pointers are R0 and R1 of the selected bank.
- RAM 80H – FFH can only be addressed indirectly, as in the 8051. The address pointers are R0 and R1 of the selected bank.
- AUX-RAM 00H –3FFH is addressed indirectly in the same way external data memory is accessed with the MOVX instruction. The address pointers are R0 and R1 of the selected bank and the DPTR register.
- Addresses higher than 3FFH are stored in external memory and are accessed indirectly with the MOVX instruction, as in the 8051.

When AUX-RAM is enabled, the instruction "MOVX @Ri" always accesses AUX-RAM. When the W78ERD2 is executing instructions from internal program memory, accessing AUX-RAM does not affect ports P0, P2, $\overline{\text{WR}}$ or $\overline{\text{RD}}$.

For example,

```
    ANL    AUXR,#11111101B   ; Enable AUX-RAM
    MOV    DPTR,#1234H
    MOV    A,#56H
    MOVX   @DPTR,A           ; Write 56h to address 1234H in external memory
    MOV    XRAMAH,#02H       ; Only 2 LSB effective
    MOV    R0,#34H
    MOV    A,@R0             ; Read AUX-RAM data at address 0234H
```

5.2 Timers/Counters

The W78ERD2 has three timers/counters called Timer 0, Timer 1, and Timer 2. Each timer/counter consists of two 8-bit data registers: TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2.

The operations of Timer 0 and Timer 1 are similar to those in the W78C52, and these timers are controlled by the TCON and TMOD registers.

Port 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

Port 0 is an open-drain, bi-directional I/O port after chip is reset. Besides, it has internal pull-up resisters enabled by setting P0UP of POPT (86H) to high. This port also provides a multiplexed, low-order address/data bus when the W78IRD2 accesses external memory.

Stack Pointer

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

The Stack Pointer stores the RAM address (scratchpad RAM, not AUX-RAM) where the stack begins. It always points to the top of the stack.

Data Pointer Low

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

This is the low byte of the standard-8052 16-bit data pointer.

Data Pointer High

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

This is the high byte of the standard-8052 16-bit data pointer.

Port 4.0 Low-Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P40AL.7	P40AL.6	P40AL.5	P40AL.4	P40AL.3	P40AL.2	P40AL.1	P40AL.0

Mnemonic: P40AL Address: 84h

Port 4.0 High-Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P40AH.7	P40AH.6	P40AH.5	P40AH.4	P40AH.3	P40AH.2	P40AH.1	P40AH.0

Mnemonic: P40AH Address: 85h

BIT	NAME	FUNCTION
7	TF1	Timer 1 overflow flag: This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. It can also be set or cleared by software.
6	TR1	1: Turn on Timer 1. 0: Turn off Timer 1.
5	TF0	Timer 0 overflow flag: This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. It can also be set or cleared by software.
4	TR0	1: Turn on Timer 0. 0: Turn off Timer 0.
3	IE1	Interrupt 1 Edge Detect: This bit is set by the hardware when a falling-edge / low-level is detected on $\overline{\text{INT1}}$. If $\overline{\text{INT1}}$ is edge-triggered, this bit is cleared by the hardware when the interrupt service routine begins. Otherwise, it follows the pin.
2	IT1	Interrupt 1 type control 1: Interrupt 1 is triggered by a falling-edge on $\overline{\text{INT1}}$. 0: Interrupt 1 is triggered by a low-level on $\overline{\text{INT1}}$.
1	IE0	Interrupt 0 Edge Detect: This bit is set by the hardware when a falling-edge / low-level is detected on $\overline{\text{INT0}}$. If $\overline{\text{INT0}}$ is edge-triggered, this bit is cleared by the hardware when the interrupt service routine begins. Otherwise, it follows the pin.
0	IT0	Interrupt 0 type control 1: Interrupt 0 is triggered by a falling-edge on $\overline{\text{INT0}}$. 0: Interrupt 0 is triggered by a low-level on $\overline{\text{INT0}}$.

Timer Mode Control

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{\text{T}}$	M1	M0	GATE	C/$\overline{\text{T}}$	M1	M0

Mnemonic: TMOD   Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/Counter 1 is enabled only while the $\overline{\text{INT1}}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{\text{INT1}}$ pin has no effect, and Timer 1 is enabled whenever TR1 is set.
6	C/$\overline{\text{T}}$	Timer or Counter Select: When cleared, Timer 1 is incremented by the internal clock. When set, Timer 1 counts falling edges on the T1 pin.
5	M1	Timer 1 Mode Select bits: See below.
4	M0	Timer 1 Mode Select bits: See below.

PCA Module 4 Register

Bit:	7	6	5	4	3	2	1	0
	-	ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4

Mnemonic: CCAPM4 Address: DEh

Clock Control Register

Bit:	7	6	5	4	3	2	1	0
	-	-	T2M	T1M	T0M	-	-	MD

Mnemonic: CKCON Address: DFh

BIT	NAME	FUNCTION
7	-	Reserved
6	-	Reserved
5	T2M	Timer 2 clock select: 0 = Divide-by-6 clock 1 = Divide-by-12 clock This bit has no effect if option bit 3 is set to 1 to select 12 clocks / machine cycle.
4	T1M	Timer 1 clock select: 0 = Divide-by-6 clock 1 = Divide-by-12 clock This bit has no effect if option bit 3 is set to 1 to select 12 clocks / machine cycle.
3	T0M	Timer 0 clock select: 0 = Divide-by-6 clock 1 = Divide-by-12 clock This bit has no effect if option bit 3 is set to 1 to select 12 clocks / machine cycle.
2	-	Reserved
1	-	Reserved
0	MD	Stretch MOVX select bits: This bit is used to select the stretch value for the MOVX instruction, which enables the microcontroller to access slower memory devices or peripherals transparently and without the need for external circuits. The RD or WR strobe and all internal timings are stretched by the selected interval. The default value is 1 cycle. For faster access, set the value to 0.

CKCON has an unrestricted read access, however, the write access is protected by timed-access protection. See the section of timed-access protection for more information.

```
MOV  P40AH, #12H
MOV  P40AL, #34H                 ; Base I/O address 1234H for P4.0
MOV  P4CONA, #00001010B          ; P4.0 is a write-strobe signal; address lines A0 and A1 are masked.
MOV  P4CONB, #00H                ; P4.1 – P4.3 are general I/O ports
MOV  P2ECON, #10H                ; Set P40SINV to 1 to invert the P4.0 write-strobe to positive polarity.
```

Then, any instruction MOVX @DPTR, A (where DPTR is in 1234H – 1237H) generates a positive-polarity, write-strobe signal on pin P4.0, while the instruction MOV P4, #XX puts bits 3 – 1 of data #XX on pins P4.3 – P4.1.

Mode 3

Mode 3 is used when an extra eight-bit timer is needed, and it has different effects on Timer 0 and Timer 1.

Timer 0 separates TL0 and TH0 into two separate eight-bit count registers. TL0 uses the Timer 0 control bits $C/\overline{T}$, GATE, TR0, $\overline{INT0}$ and TF0 and can count clock cycles (clock / 12 or clock / 6) or falling edges on pin T0. Meanwhile, TH0 takes over TR1 and TF1 from Timer 1 and can count clock cycles (clock / 12 or clock / 6).

Mode 3 simply freezes Timer 1, which provides a way to turn it on and off. When Timer 0 is in mode 3, Timer 1 can still be used in modes 0, 1 and 2, but its flexibility is limited. Timer 1 can still be used as a timer / counter (or a baud-rate generator for the serial port) and retains the use of GATE and INT1 pin, but it no longer has control over the overflow flag TF1 and enable bit TR1.

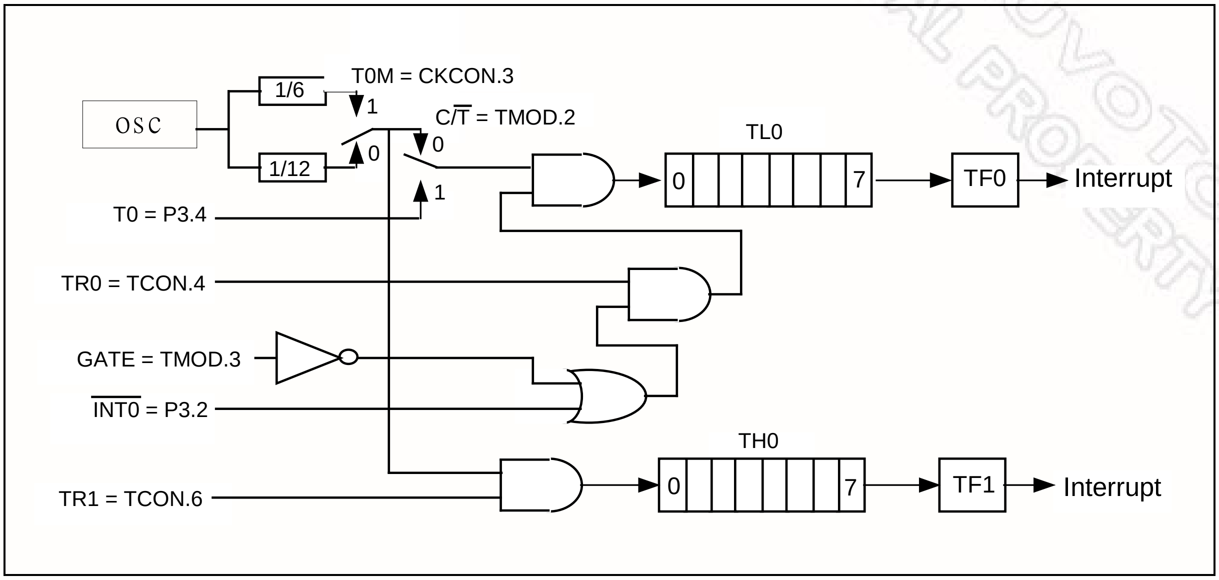


Figure 9-3 Timer/Counter 0 Mode 3

9.2 Timer/Counter 2

Timer 2 is a 16-bit up/down counter equipped with a capture/reload capability. It is configured by the T2MOD register and controlled by the T2CON register. As with Timers 0 and 1, Timer 2 can count clock cycles (fosc / 12 or fosc / 6) or the external T2 pin, as selected by $C/\overline{T2}$, and there are four operating modes, each discussed below.

Capture Mode

Capture mode is enabled by setting the $CP/\overline{RL2}$ bit in the T2CON register. In capture mode, Timer 2 serves as a 16-bit up-counter. When the counter rolls over from FFFFh to 0000h, the TF2 bit is set, and, if enabled, an interrupt is generated.

If the EXEN2 bit is set, then a negative transition on the T2EX pin captures the value in TL2 and TH2 registers in the RCAP2L and RCAP2H registers. This action also causes the EXF2 bit in T2CON to be set, which may also generate an interrupt.

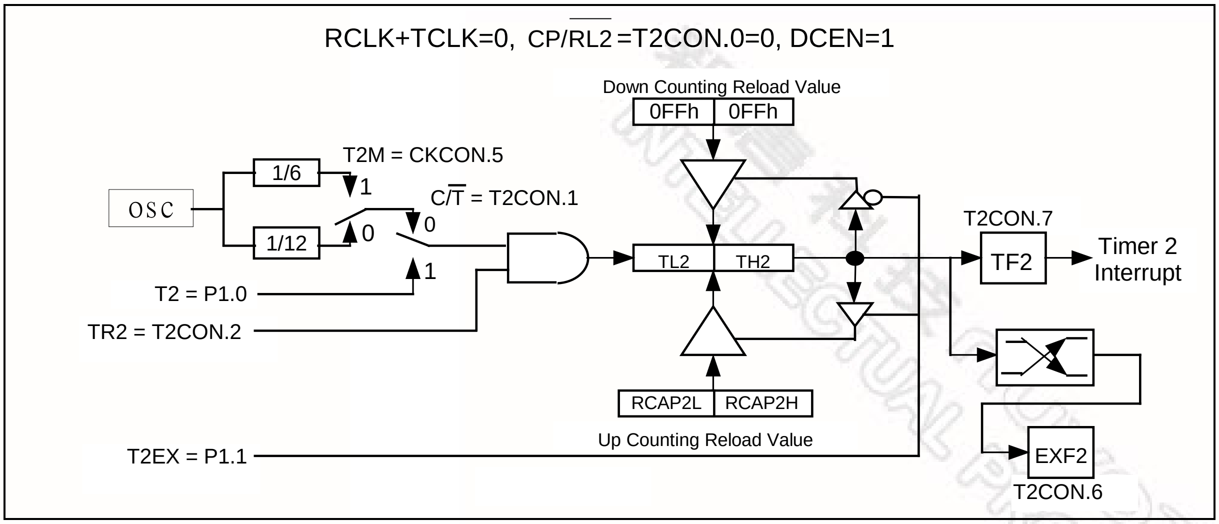


Figure 9-6 16-Bit Auto-reload Up/Down Counter

Baud Rate Generator Mode

Baud-rate generator mode is enabled by setting either the RCLK or TCLK bits in T2CON register. In baud-rate generator mode, Timer 2 is a 16-bit up-counter that automatically reloads when it overflows, but this overflow does not set the timer overflow bit TF2. If EXEN2 is set, then a negative transition on the T2EX pin sets EXF2 bit in T2CON and, if enabled, generates an interrupt request.

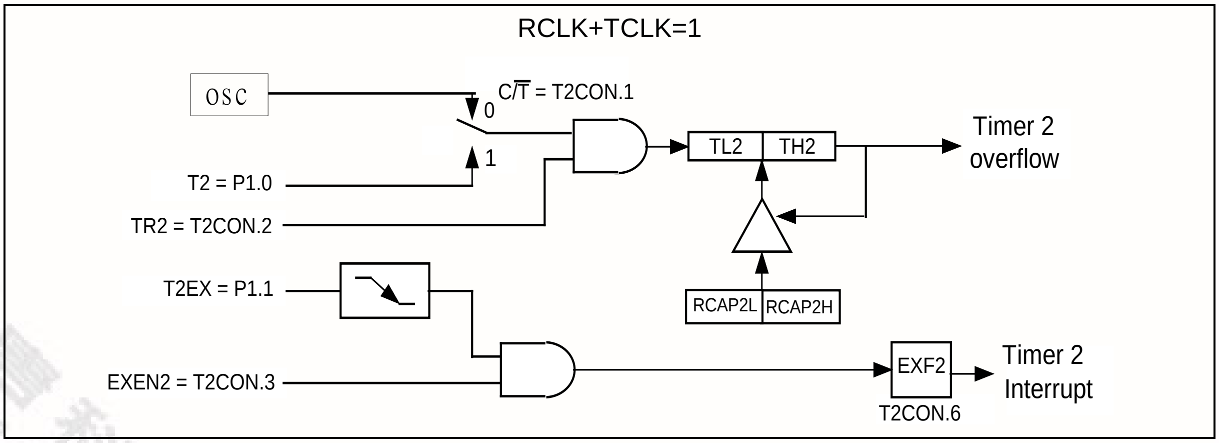


Figure 9-7 Baud Rate Generator Mode

As mentioned before, data enters and leaves the serial port on RxD. TxD line provides the shift clock, which shifts data into and out of the W78ERD2 and the device at the other end of the line. Any instruction that writes to SBUF starts the transmission. The shift clock is activated, and the data is shifted out on the RxD pin until all eight bits are transmitted. If SM2 is set to 1, the data appears on RxD one clock period before the falling edge on TxD, and the TxD clock then remains low for two clock periods before going high again. If SM2 is set to 0, the data appears on RxD three clock periods before the falling edge on TxD, and the TxD clock then remains low for six clock periods before going high again. This ensures that the receiving device can clock RxD data on the rising edge of TxD or when the TxD clock is low. Finally, the TI flag is set high in C1 once the last bit has been transmitted.

The serial port receives data when REN is 1 and RI is zero. The TxD clock is activated, and the serial port latches data on the rising edge of the shift clock. As a result, the external device should present data on the falling edge of TxD. This process continues until all eight bits have been received. Then, after the last rising edge on TxD, the RI flag is set high in C1, which stops reception until RI is cleared by the software.

10.2 MODE 1

Mode 1 is a full–duplex, asynchronous mode. Serial communication frames are made up of ten bits transmitted on TXD and received on RXD. The ten bits consist of a start bit (0), eight data bits (LSB first), and a stop bit (1). When the W78ERD2 receives data, the stop bit goes into RB8 in SCON. The baud rate is either 1/16 or 1/32 of the Timer 1 overflow, which can be set to a variety of reload values. (The 1/16 or 1/32 factor is determined by the SMOD bit in PCON SFR.) The functional diagram is shown below.

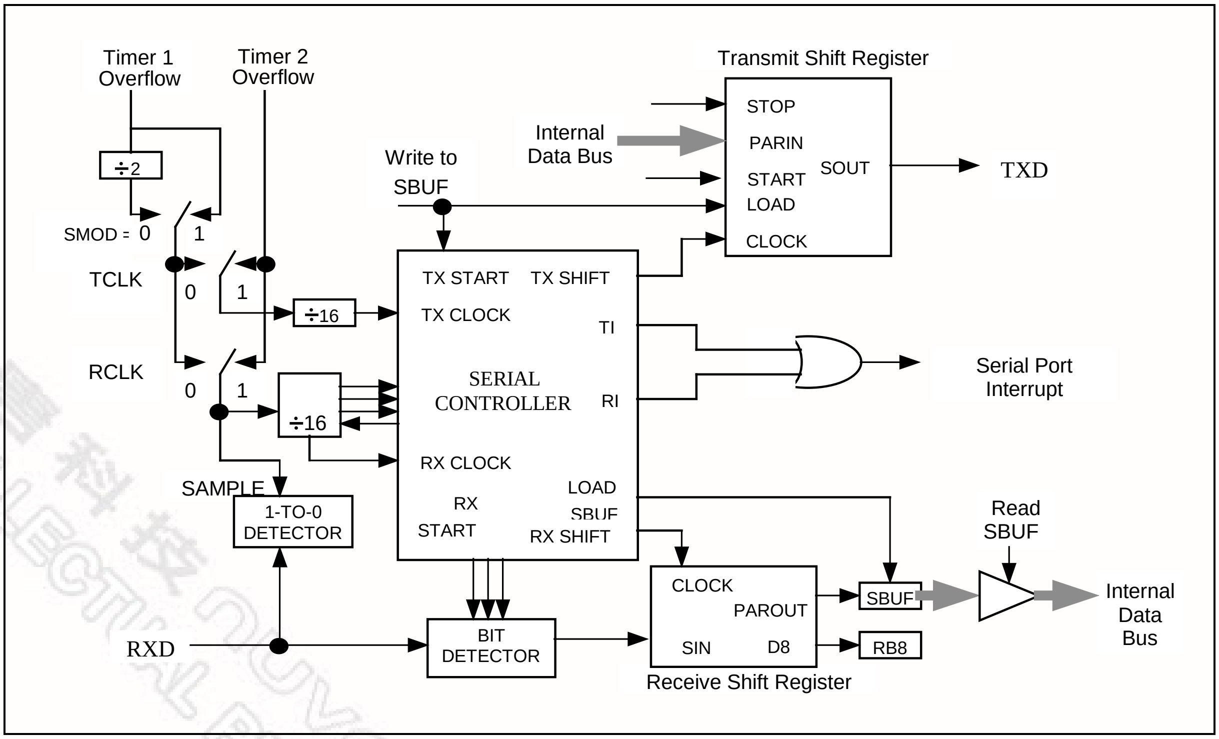


Figure 10-2 Serial Port Mode 1

Transmission begins when data is written to SBUF but is synchronized with the roll-over of Timer 1 (divided by 16 or 32, as configured) and not the write signal. The W78ERD2 waits until the next roll-over of Timer 1 (divided by 16 or 32) before the data is put on TxD. The next bit is placed on TxD after the next rollover. After all eight bits of data are transmitted, the stop bit is transmitted. Finally, the TI flag is set, at the tenth rollover after the write signal.

Reception is enabled only if REN is high. The W78ERD2 samples the RxD line at a rate of 16 times the selected baud rate, looking for a falling edge. When a falling edge is detected on the RxD pin, Timer 1 (divided by 16 or 32) is immediately reset to align the bit boundaries better, and the serial port starts receiving data. The 16 states of the counter effectively divide the time into 16 slices, and bit detection is done on a best-of-three basis using the eighth, ninth and tenth states. If the start bit is invalid (1), reception is aborted, and the serial port resumes looking for a falling edge on RxD. If the start bit is valid, the eight data bits are shifted in. Then, if

(1) RI = 0 and

(2) SM2 = 0 or the stop bit = 1,

the stop bit is put into RB8, the data is put in SBUF, and RI is set. Otherwise, the received frame may be lost. In the middle of the stop bit, the W78ERD2 resumes looking for falling edges on RxD.

10.3 MODE 2

Mode 2 is a full-duplex, asynchronous mode. Serial communication frames are made up of eleven bits transmitted on TXD and received on RXD. The eleven bits consist of a start bit (0), eight data bits (LSB first), a programmable ninth bit (TB8) and a stop bit (1). The ninth bit is read into and transmitted from RB8. The baud rate is either 1/32 or 1/64 of the oscillator frequency, and the 1/32 or 1/64 factor is determined by the SMOD bit in PCON SFR. The functional diagram is shown below.

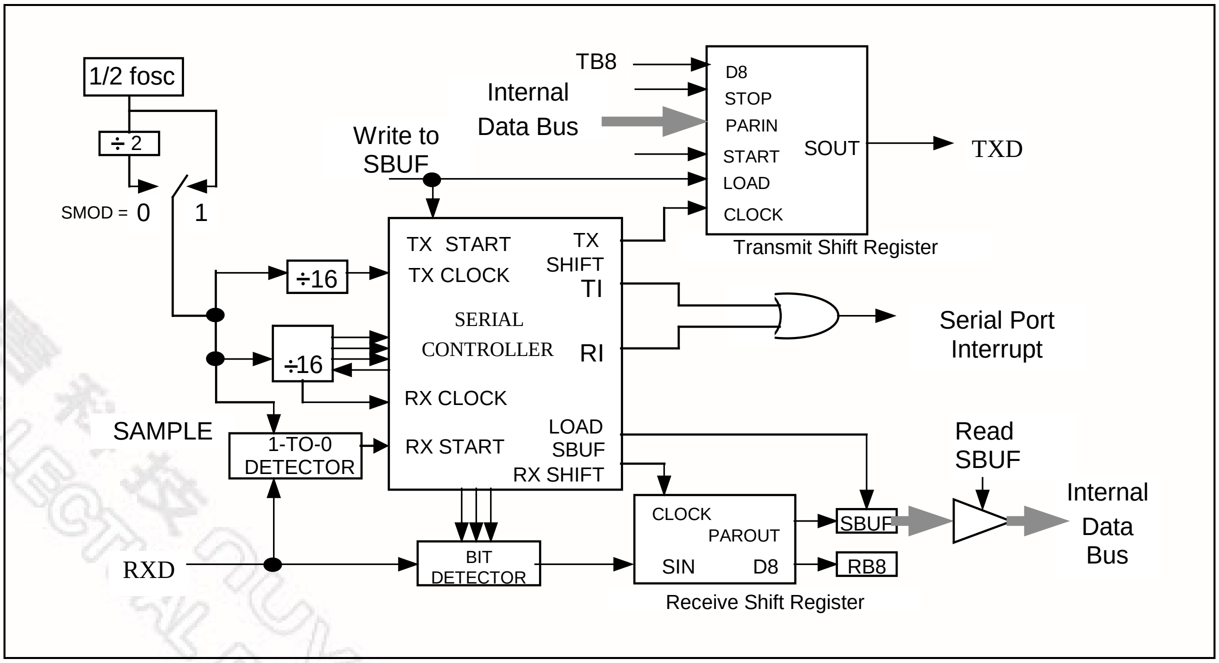


Figure 10-3 Serial Port Mode 2

Transmission begins when data is written to SBUF but is synchronized with the roll-over of the counter (divided by 32 or 64, as configured) and not the write signal. The W78ERD2 waits until the next roll-over of the counter (divided by 32 or 64) before the data is put on TxD. The next bit is placed on TxD after the next rollover. After all nine bits of data are transmitted, the stop bit is transmitted. Finally, the TI flag is set, at the eleventh rollover after the write signal.

Reception is enabled only if REN is high. The W78ERD2 samples the RxD line at a rate of 16 times the selected baud rate, looking for a falling edge. When a falling edge is detected on the RxD pin, the counter (divided by 32 or 64) is immediately reset to align the bit boundaries better, and the serial port starts receiving data. The 16 states of the counter effectively divide the time into 16 slices, and bit detection is done on a best-of-three basis using the eighth, ninth and tenth states. If the start bit is invalid (1), reception is aborted, and the serial port resumes looking for a falling edge on RxD. If the start bit is valid, the rest of the bits are shifted in. Then, if

(1) RI = 0 and

(2) Either SM2 = 0 or the received 9th bit = 1,

the ninth bit is put into RB8, the data is put in SBUF, and RI is set. Otherwise, the received frame may be lost. In the middle of the stop bit, the W78ERD2 resumes looking for falling edges on RxD.

10.4 MODE 3

Mode 3 is similar to mode 2 in all respects, except that the baud rate is programmable the same way it is programmable in mode 1. The functional diagram is shown below.

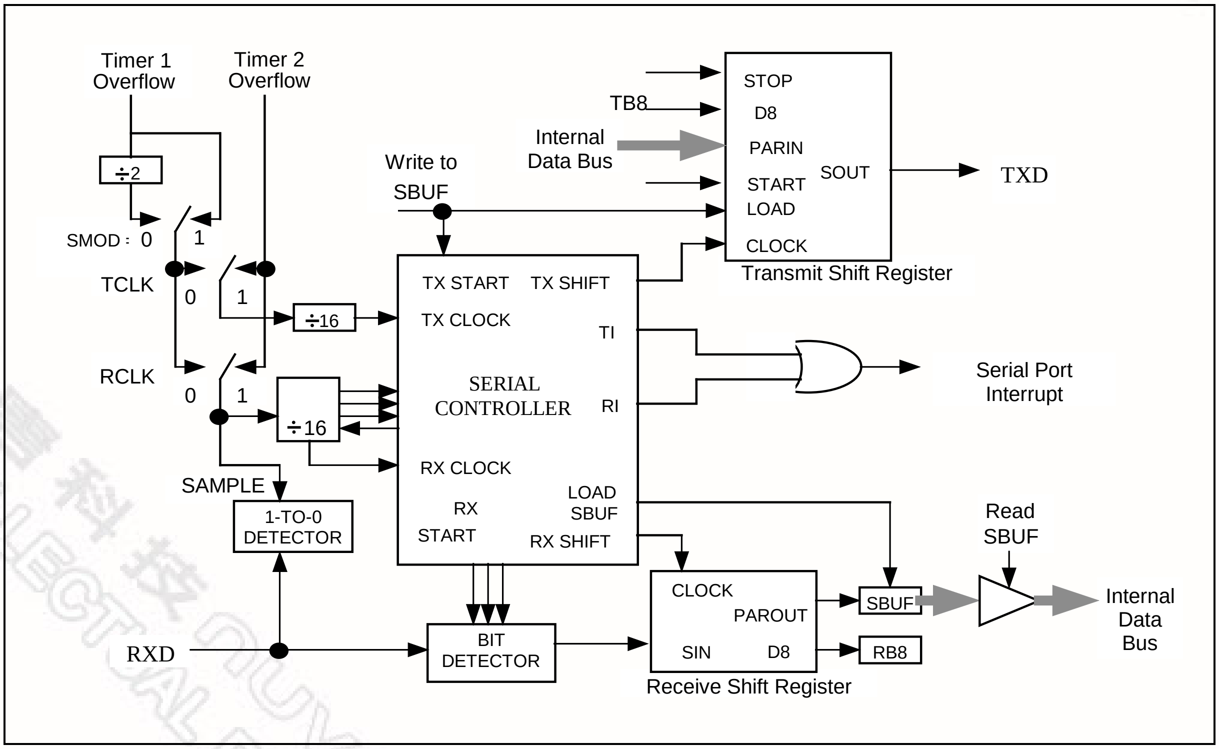


Figure 10-4 Serial Port Mode 3

10.5 Framing Error Detection

A frame error occurs when a valid stop bit is not detected. This could indicate incorrect serial data communication. Typically, the frame error is due to noise or contention on the serial communication line. The W78ERD2 has the ability to detect framing errors and set a flag which can be checked by software.

The frame error FE bit is located in SCON.7. This bit is normally used as SM0 in the standard 8051 family. However, in the W78ERD2 it serves a dual function and is called SM0/FE. There are actually two separate flags, one for SM0 and the other for FE. The flag that is actually accessed as SCON.7 is determined by SMOD0 (PCON.6) bit. When SMOD0 is set to 1, then the FE flag is accessed. When SMOD0 is set to 0, then the SM0 flag is accessed.

The FE bit is set to 1 by the hardware but must be cleared by software. Once FE is set, any frames received afterwards, even those without any errors, do not clear the FE flag. The flag has to be cleared by software. Note that SMOD0 must be set to 1 while reading or writing to FE.

10.6 Multi-Processor Communications

Multi-processor communication makes use of the 9th data bit in modes 2 and 3. In the W78ERD2, the RI flag is set only if the received byte corresponds to the Given or Broadcast address. This hardware feature eliminates the software overhead required in checking every received address and greatly simplifies the software programmer task.

In multi-processor communication mode, the address bytes are distinguished from the data bytes by the 9th bit, which is set high for address bytes. When the master processor wants to transmit a block of data to one of the slaves, it first sends out the address of the target slave (or slaves). All the slave processors should have their SM2 bit set high when waiting for an address byte. This ensures that they are interrupted only by the reception of an address byte. The automatic address recognition feature ensures that only the addressed slave is actually interrupted because the address comparison is done by the hardware, not the software.

The addressed slave clears the SM2 bit, thereby clearing the way to receive data bytes. With SM2 = 0, the slave is interrupted on the reception of every single complete frame of data. The unaddressed slaves are not affected, as they are still waiting for their address.

The Master processor can selectively communicate with groups of slaves by using the Given Address. All the slaves can be addressed together using the Broadcast Address. The addresses for each slave are defined in the SADDR and SADEN registers. The slave address is an eight-bit value specified in the SADDR SFR. The SADEN SFR is actually a mask for the byte value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is don't care. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR.

The following example shows how the user can define the Given Address to address different slaves.

14. TIMED-ACCESS PROTECTION

The W78ERD2 has features like Timer clock selecting by setting CKCON, software reset and ISP function that are crucial to the proper operation of the system. Consequently, The SFR CHPCON and CKCON, which control the functions, have restricted write access to protect CPU from errant operation. The W78ERD2 provides has a timed-access protection scheme that controls write access to critical bits.

In this scheme, protected bits have a timed write-enable window. A write is successful only if this window is active; otherwise, the write is discarded. The write-enable window is opened in two steps. First, the software writes 87h to the register CHPENR. This starts a counter, which expires in three machine cycles. Then, if the software writes 59h to CHPENR before the counter expires, the write-enable window is opened for three machine cycles. After three machine cycles, the window automatically closes, and the procedure must be repeated again to access protected bits.

The suggested code for opening the write-enable window is

```
CHPENR REG  0F6h          ; Define new register CHPENR, located at 0F6h
    MOV CHPENR, #87h
    MOV CHPENR, #59h
```

Five examples, some correct and some incorrect, of using timed-access protection are shown below.

Example 1: Valid access

```
MOV CHPENR, #87h     ;3 M/C, Note: M/C = Machine Cycles
MOV CHPENR, #59h     ;3 M/C
MOV CKCON, #00h      ;3 M/C
```

Example 2: Valid access

```
MOV CHPENR, #87h     ;3 M/C
MOV CHPENR, #59h     ;3 M/C
NOP                  ;1 M/C
SETB   EWT           ;2 M/C
```

Example 3: Valid access

```
MOV CHPENR, #87h     ;3 M/C
MOV CHPENR, #59h     ;3 M/C
ORL  CKCON, #01h     ;3M/C
```

Example 4: Invalid access

```
MOV CHPENR, #87h     ;3 M/C
MOV CHPENR, #59h     ;3 M/C
NOP                  ;1 M/C
NOP                  ;1 M/C
CLR  MD              ;2 M/C
```

Example 5: Invalid Access

```
MOV CHPENR, #87h     ;3 M/C
NOP                  ;1 M/C
MOV CHPENR, #59h     ;3 M/C
SETB   MD            ;2 M/C
```

In the first three examples, the protected bits are written before the window closes. In Example 4, however, the write occurs after the window has closed, so there is no change in the protected bit. In Example 5, the second write to CHPENR occurs four machine cycles after the first write, so the timed access window in not opened at all, and the write to the protected bit fails.

16. H/W REBOOT MODE (BOOT FROM LDROM)

By default, the W78ERD2 boots up from the AP Flash EPROM after a power-on reset. Sometimes, this is not desirable. H/W REBOOT mode forces the W78ERD2 to use the LD Flash EPROM instead and execute in-system programming procedures. Enter H/W REBOOT mode using these settings.

H/W REBOOT MODE

P4.3	P2.7	P2.6	OPTION BIT	MODE
X	L	L	Bit4 = L	H/W REBOOT
L	X	X	Bit5 = L	H/W REBOOT

This might be implemented by connecting pins P2.6 and P2.7 to switches or jumpers. For example, in a CD-ROM system, P2.6 and P2.7 might be connected to the PLAY and EJECT buttons on the panel. If the user wants to enter H/W REBOOT mode, the user can press these two buttons at the same time and then turn on the power to force the W78ERD2 to enter H/W REBOOT mode. After the power-on, releasing both buttons finishes the in-system programming procedure.

This mode can be accidentally activated, so **be careful with the values of pins P2, P3, ALE,** $\overline{\text{EA}}$ **and** $\overline{\text{PSEN}}$ **at reset**.

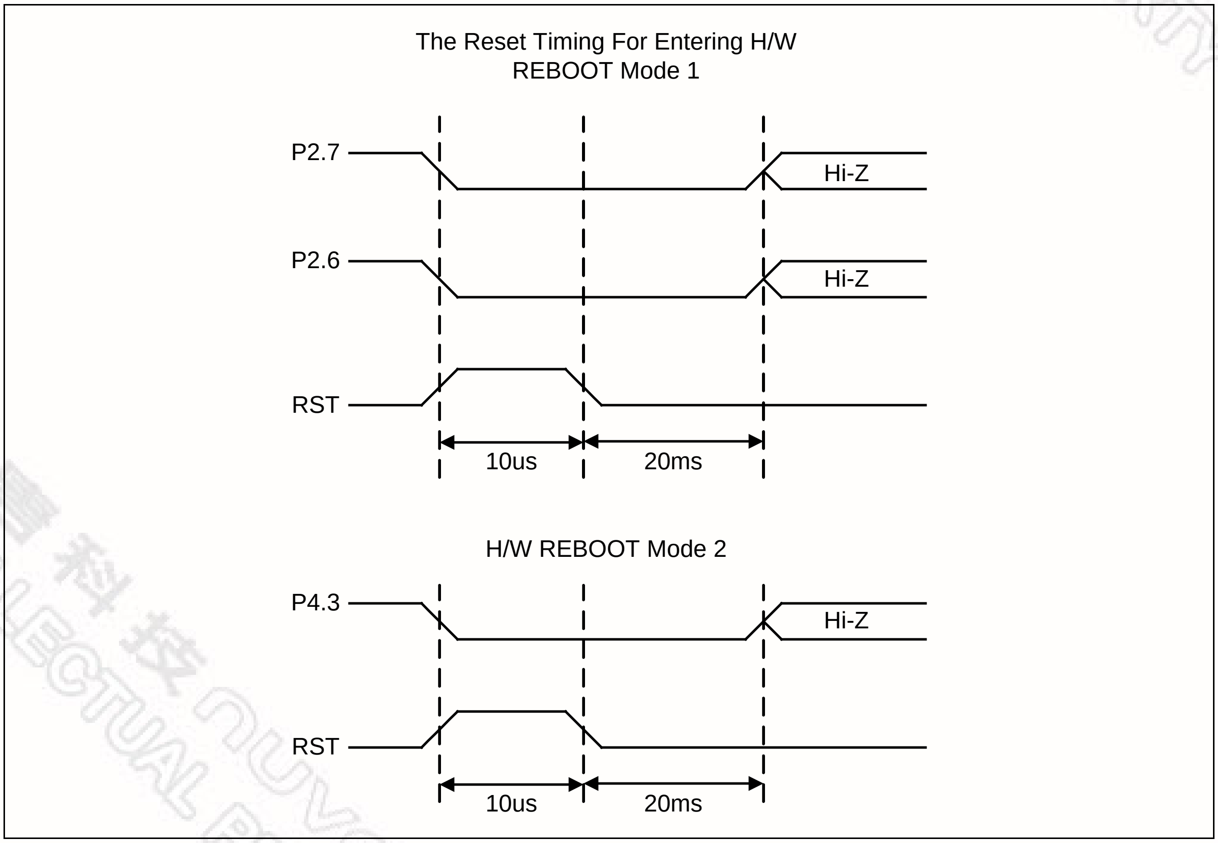


Figure 16-1

17. OPTION BITS REGISTER

In the on-chip Flash EPROM writer programming mode mode, the flash EPROM can be programmed and verified repeatedly. Until the code is ready, it can be protected by properly setting option bits. Option bits control the initial configuration of W78ERD2, including code protection, system clock mode selection (6T/12T), H/W reboot mode selection and oscillator control.

D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3	B2	B1	B0

B0: Lock bit, Logic 0 is active

B1: MOVC Inhibit, Logic 0 is active

B2: Encryption bit, Logic 0 is active

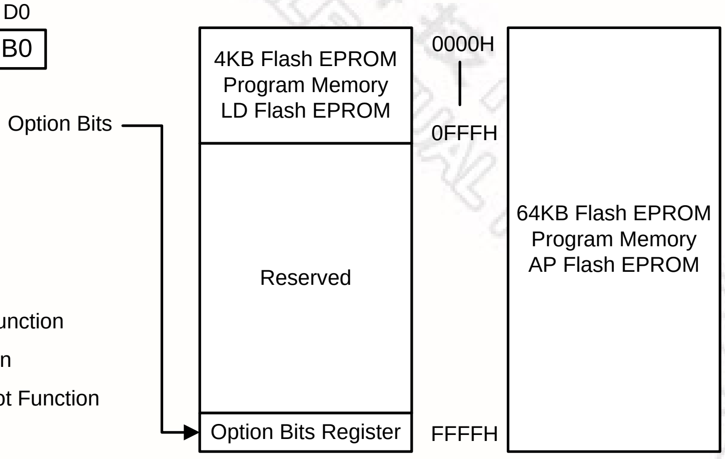
B3: logic 1 is 12 clock per machine cycle
logic 0 is 6 clock per machine cycle

B4: Enable P2.7 and P2.6 as H/W Reboot Function
logic 1: P2.7 and P2.6 are as I/O Function
logic 0: P2.7 and P2.6 are as H/W Reboot Function

B5: Enable P4.3 as H/W Reboot Function
logic 1: P4.3 is as I/O Function
logic 0: P4.3 is as H/W Reboot Function

B6: Reserved (0)

B7: Logic 1: The Crystal Frequency is above 25MHz
Logic 0: The Crystal Frequency is under 25MHz



Default 1 is for all Security Bits.
The Reserved bit must be kept in logic 1.

Option Bits Register

Lock bit

This bit is used to protect the code in the W78ERD2. It may be set after the programmer finishes programming and verifies the sequence. Once this bit is set to logic-0, both the Flash EPROM data and Option Bits Register cannot be accessed again.

MOVC Inhibit

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent a MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic-0, a MOVC instruction in external program memory space can only access code in external memory, not in internal memory. A MOVC instruction in internal program memory can always access both internal and external memory. If this bit is logic-1, there are no restrictions on MOVC.

Encryption

This bit is used to enable and disable the encryption logic for code protection. Once encryption is enabled, the data presented on port 0 is encoded via encryption logic. This bit can be reset only by erasing the whole chip.

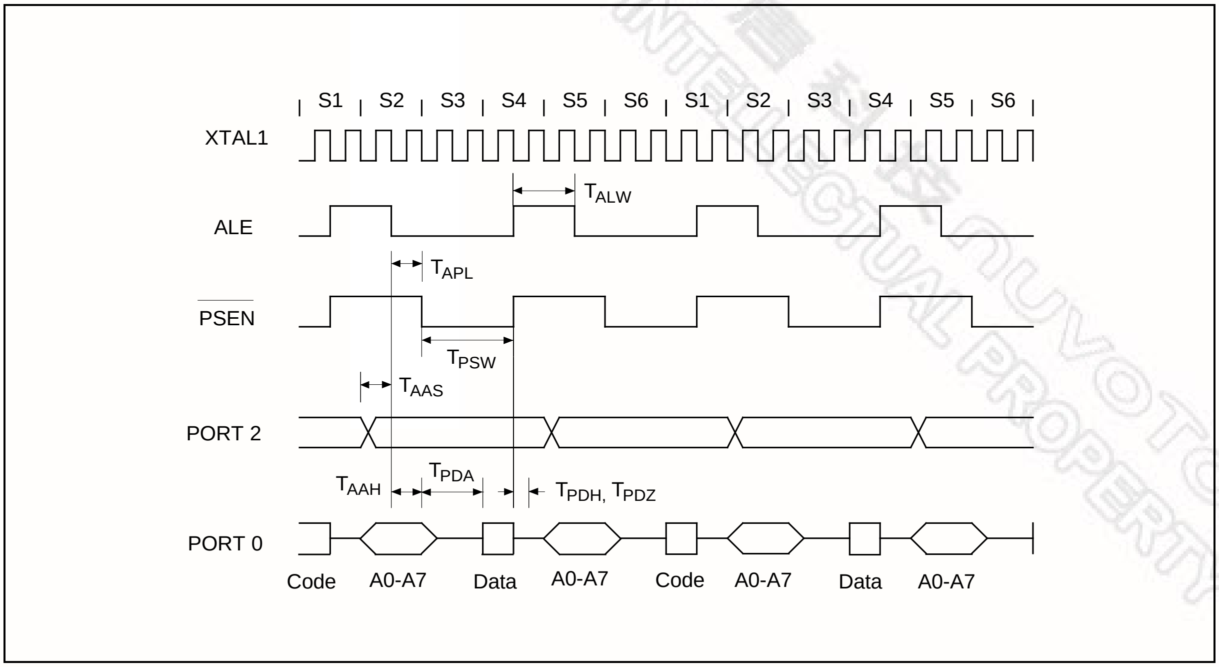
Oscillator Control

The gain of the on-chip oscillator amplifier can be reduced by bit B7 in the option bits register. If bit 7 is set to zero, the gain is cut in half.

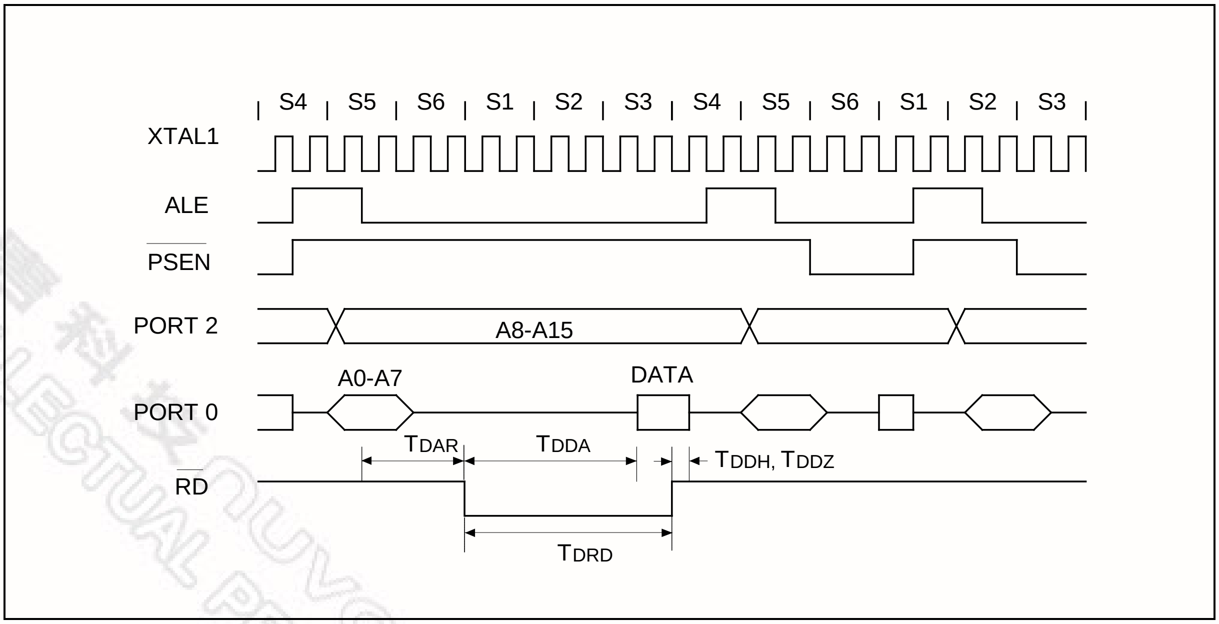
According the circuit in Figure 20-1, the values of R, C1 and C2 may need some adjustment when running at lower gain. Furthermore, reducing the gain by one-half may improperly affect an external crystal running at frequencies above 25 MHz.

19. TIMING WAVEFORMS

Program Fetch Cycle

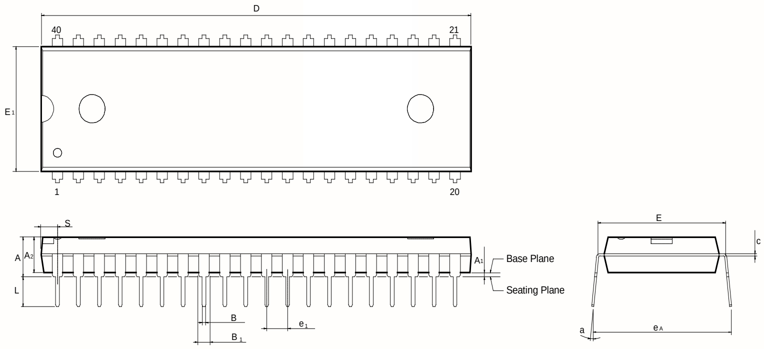


Data Read Cycle



21. PACKAGE DIMENSIONS

40-pin DIP

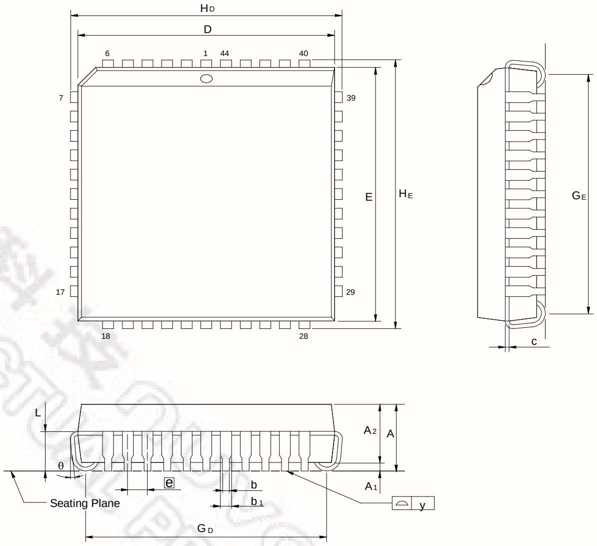


Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.334
A_1	0.010	—	—	0.254	—	—
A_2	0.150	0.155	0.160	3.81	3.937	4.064
B	0.016	0.018	0.022	0.406	0.457	0.559
B_1	0.048	0.050	0.054	1.219	1.27	1.372
c	0.008	0.010	0.014	0.203	0.254	0.356
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.986	15.24	15.494
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.286	2.54	2.794
L	0.120	0.130	0.140	3.048	3.302	3.556
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.01
S	—	—	0.090	—	—	2.286

Notes:

1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

44-pin PLCC

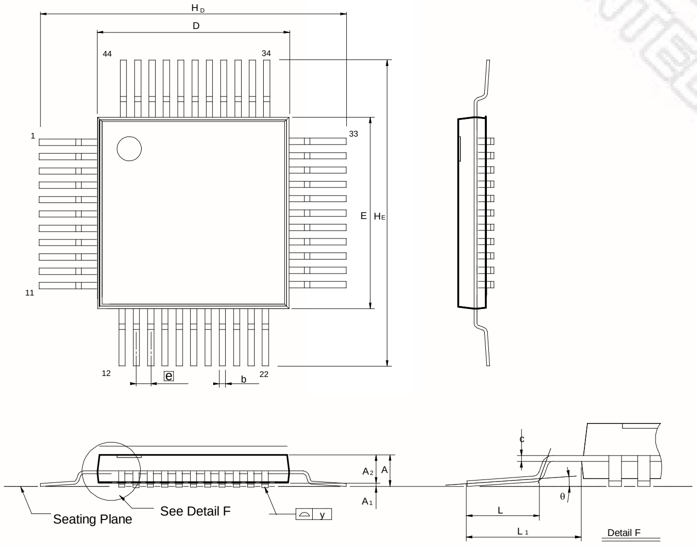


Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
$\boxed{e}$	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.296	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

44-pin PQFP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	---	---	---	---
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
$\boxed{e}$	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.510	0.520	0.530	12.95	13.2	13.45
H_E	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

```
          MOV PCON, #01H
          INC R2
          MOVX A, @DPTR
          INC DPTR
          CJNE A, SFRFD, ERROR_64K
          CJNE R2, #0H, READ_VERIFY_64K
          INC R1
          MOV SFRAH, R1
          CJNE R1, #0H, READ_VERIFY_64K

;********************************************************************************
;* PROGRAMMING COMPLETLY, SOFTWARE RESET CPU
;********************************************************************************
          MOV CHPENR, #87H        ; CHPENR = 87H
          MOV CHPENR, #59H        ; CHPENR = 59H
          MOV CHPCON, #83H        ; CHPCON = 83H, SOFTWARE RESET.

ERROR_64K:
          DJNZ R4, UPDATE_64K     ; IF ERROR OCCURS, REPEAT 3 TIMES.
          .                       ; IN-SYSTEM PROGRAMMING FAIL, USER'S PROCESS TO DEAL WITH IT.
          .
          .
          .
```

22.2 How to Use Programmable Counter Array

Please go to Nuvoton’s website at http://www.Nuvoton.com.tw fort the application note.