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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

E·XF

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f818t-i-sstsl

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NOTES:





#### 2.2.2.2 OPTION\_REG Register

The OPTION\_REG register is a readable and writable register that contains various control bits to configure the TMR0 prescaler/WDT postscaler (single assignable register known also as the prescaler), the external INT interrupt, TMR0 and the weak pull-ups on PORTB.

**Note:** To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer.

#### **REGISTER 2-2: OPTION\_REG: OPTION REGISTER (ADDRESS 81h, 181h)**

	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1				
	RBPU	INTEDG	T0CS	TOSE	PSA	PS2	PS1	PS0				
	bit 7	·		·				bit 0				
bit 7	<b>RBPU</b> : PO 1 = PORT 0 = PORT	<b>RBPU</b> : PORTB Pull-up Enable bit1 = PORTB pull-ups are disabled0 = PORTB pull-ups are enabled by individual port latch values										
bit 6	<b>INTEDG:</b> I 1 = Interru 0 = Interru	INTEDG: Interrupt Edge Select bit 1 = Interrupt on rising edge of RB0/INT pin 0 = Interrupt on falling edge of RB0/INT pin										
bit 5	<b>TOCS:</b> TM 1 = Transi 0 = Interna	<b>TOCS:</b> TMR0 Clock Source Select bit 1 = Transition on T0CKI pin 0 = Internal instruction cycle clock (CLKO)										
bit 4	<b>TOSE:</b> TMR0 Source Edge Select bit 1 = Increment on high-to-low transition on T0CKI pin 0 = Increment on low-to-bigh transition on T0CKI pin											
bit 3	<b>PSA:</b> Pres 1 = Presca 0 = Presca	<b>PSA:</b> Prescaler Assignment bit 1 = Prescaler is assigned to the WDT 0 = Prescaler is assigned to the Timer() module										
bit 2-0	Bit Value       TMR0 Rate       WDT Rate         000       1:2       1:1         001       1:4       1:2         010       1:8       1:4         011       1:16       1:8         100       1:32       1:16         101       1:64       1:32         110       1:128       1:64         111       1:256       1:128											
	Legend:											
	R = Reada -n = Value	able bit at POR	W = Wr '1' = Bit	ritable bit t is set	U = Unimp '0' = Bit is	cleared	bit, read as x = Bit is ι	'0' unknown				

#### 2.2.2.3 INTCON Register

The INTCON register is a readable and writable register that contains various enable and flag bits for the TMR0 register overflow, RB port change and external RB0/INT pin interrupts. Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the Global Interrupt Enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

#### REGISTER 2-3: INTCON: INTERRUPT CONTROL REGISTER (ADDRESS 0Bh, 8Bh, 10Bh, 18Bh)

	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x			
	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF			
	bit 7							bit 0			
oit 7	<b>GIE:</b> Globa 1 = Enable 0 = Disabl	GIE: Global Interrupt Enable bit 1 = Enables all unmasked interrupts 0 = Disables all interrupts									
oit 6	<ul> <li>PEIE: Peripheral Interrupt Enable bit</li> <li>1 = Enables all unmasked peripheral interrupts</li> <li>0 = Disables all peripheral interrupts</li> </ul>										
oit 5	<b>TMROIE:</b> T 1 = Enable 0 = Disabl	<b>TMR0IE:</b> TMR0 Overflow Interrupt Enable bit 1 = Enables the TMR0 interrupt 0 = Disables the TMR0 interrupt									
oit 4	INTE: RB0 1 = Enable 0 = Disabl	INTE: RB0/INT External Interrupt Enable bit 1 = Enables the RB0/INT external interrupt 0 = Disables the RB0/INT external interrupt									
oit 3	<b>RBIE:</b> RB 1 = Enable 0 = Disabl	<b>RBIE:</b> RB Port Change Interrupt Enable bit 1 = Enables the RB port change interrupt 0 = Disables the RB port change interrupt									
oit 2	<b>TMROIF:</b> T 1 = TMRO 0 = TMRO	MR0 Overflov register has register did r	w Interrupt Fl overflowed (r not overflow	lag bit nust be clea	red in softw	vare)					
oit 1	<b>INTF:</b> RB0 1 = The R 0 = The R	/INT External B0/INT exterr B0/INT exterr	Interrupt Fla nal interrupt o nal interrupt o	ig bit occurred (mi did not occu	ust be clear	ed in softwa	are)				
oit O	<ul> <li>RBIF: RB Port Change Interrupt Flag bit</li> <li>A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.</li> <li>1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)</li> <li>0 = None of the RB7:RB4 pins have changed state</li> </ul>										
	<b>Legend:</b> R = Reada	able bit	W = Wr	itable bit	U = Unim	plemented	bit, read as	·0'			

'1' = Bit is set

'0' = Bit is cleared

-n = Value at POR

x = Bit is unknown

#### FIGURE 2-6: DIRECT/INDIRECT ADDRESSING



### 3.7 Writing to Flash Program Memory

Flash program memory may only be written to if the destination address is in a segment of memory that is not write-protected, as defined in bits WRT1:WRT0 of the device Configuration Word (Register 12-1). Flash program memory must be written in four-word blocks. A block consists of four words with sequential addresses, with a lower boundary defined by an address, where EEADR<1:0> = 00. At the same time, all block writes to program memory are done as write-only operations. The program memory must first be erased. The write operation is edge-aligned and cannot occur across boundaries.

To write to the program memory, the data must first be loaded into the buffer registers. There are four 14-bit buffer registers and they are addressed by the low 2 bits of EEADR.

The following sequence of events illustrate how to perform a write to program memory:

- Set the EEPGD and WREN bits in the EECON1 register
- Clear the FREE bit in EECON1
- Write address to EEADRH:EEADR
- Write data to EEDATH:EEDATA
- Write 55 to EECON2
- Write AA to EECON2
- Set WR bit in EECON 1

The user must follow the same specific sequence to initiate the write for each word in the program block by writing each program word in sequence (00, 01, 10, 11).

There are 4 buffer register words and all four locations **MUST** be written to with correct data.

After the "BSF EECON1, WR" instruction, if EEADR  $\neq$  xxxxx11, then a short write will occur. This short write-only transfers the data to the buffer register. The WR bit will be cleared in hardware after one cycle.

After the "BSF EECON1, WR" instruction, if EEADR = xxxxx11, then a long write will occur. This will simultaneously transfer the data from EEDATH:EEDATA to the buffer registers and begin the write of all four words. The processor will execute the next instruction and then ignore the subsequent instruction. The user should place NOP instructions into the second words. The processor will then halt internal operations for typically 2 msec in which the write takes place. This is not a Sleep mode, as the clocks and peripherals will continue to run. After the write cycle, the processor will resume operation with the 3rd instruction after the EECON1 write instruction.

After each long write, the 4 buffer registers will be reset to 3FFF.



#### FIGURE 3-1: BLOCK WRITES TO FLASH PROGRAM MEMORY

### 5.2 PORTB and the TRISB Register

PORTB is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin).

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit RBPU (OPTION\_REG<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Four of PORTB's pins, RB7:RB4, have an interrupt-onchange feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupton-change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are ORed together to generate the RB Port Change Interrupt with Flag bit, RBIF (INTCON<0>).

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

- a) Any read or write of PORTB. This will end the mismatch condition.
- b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

RB0/INT is an external interrupt input pin and is configured using the INTEDG bit (OPTION\_REG<6>).

PORTB is multiplexed with several peripheral functions (see Table 5-3). PORTB pins have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTB pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modifywrite instructions (BSF, BCF, XORWF) with TRISB as the destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

TABLE 5-3:	PORTB FUNCTIONS
TABLE 5-3:	PURID FUNCTIONS

Name	Bit#	Buffer	Function
RB0/INT	bit 0	TTL/ST <sup>(1)</sup>	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1/SDI/SDA	bit 1	TTL/ST <sup>(5)</sup>	Input/output pin, SPI data input pin or I <sup>2</sup> C™ data I/O pin. Internal software programmable weak pull-up.
RB2/SDO/CCP1	bit 2	TTL/ST <sup>(4)</sup>	Input/output pin, SPI data output pin or Capture input/Compare output/PWM output pin. Internal software programmable weak pull-up.
RB3/CCP1/PGM <sup>(3)</sup>	bit 3	TTL/ST <sup>(2)</sup>	Input/output pin, Capture input/Compare output/PWM output pin or programming in LVP mode. Internal software programmable weak pull-up.
RB4/SCK/SCL	bit 4	TTL/ST <sup>(5)</sup>	Input/output pin or SPI and I <sup>2</sup> C clock pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB5/SS	bit 5	TTL	Input/output pin or SPI slave select pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB6/T1OSO/T1CKI/ PGC	bit 6	TTL/ST <sup>(2)</sup>	Input/output pin, Timer1 oscillator output pin, Timer1 clock input pin or serial programming clock (with interrupt-on-change). Internal software programmable weak pull-up.
RB7/T1OSI/PGD	bit 7	TTL/ST <sup>(2)</sup>	Input/output pin, Timer1 oscillator input pin or serial programming data (with interrupt-on-change). Internal software programmable weak pull-up.

**Legend:** TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

3: Low-Voltage ICSP<sup>™</sup> Programming (LVP) is enabled by default which disables the RB3 I/O function. LVP must be disabled to enable RB3 as an I/O pin and allow maximum compatibility to the other 18-pin mid-range devices.

- 4: This buffer is a Schmitt Trigger input when configured for CCP or SSP mode.
- **5:** This buffer is a Schmitt Trigger input when configured for SPI or I<sup>2</sup>C mode.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
06h, 106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
86h, 186h	TRISB	PORTB	ORTB Data Direction Register							1111 1111	1111 1111
81h, 181h	OPTION_REG	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

**Legend:** x = unknown, u = unchanged. Shaded cells are not used by PORTB.

#### FIGURE 5-9: BLOCK DIAGRAM OF RB1 PIN



# 7.0 TIMER1 MODULE

The Timer1 module is a 16-bit timer/counter consisting of two 8-bit registers (TMR1H and TMR1L) which are readable and writable. The TMR1 register pair (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The TMR1 interrupt, if enabled, is generated on overflow which is latched in interrupt flag bit, TMR1IF (PIR1<0>). This interrupt can be enabled/disabled by setting/clearing TMR1 Interrupt Enable bit, TMR1IE (PIE1<0>).

Timer1 can also be used to provide Real-Time Clock (RTC) functionality to applications with only a minimal addition of external components and code overhead.

### 7.1 Timer1 Operation

Timer1 can operate in one of three modes:

- as a timer
- as a synchronous counter
- · as an asynchronous counter

The operating mode is determined by the clock select bit, TMR1CS (T1CON<1>).

In Timer mode, Timer1 increments every instruction cycle. In Counter mode, it increments on every rising edge of the external clock input.

Timer1 can be enabled/disabled by setting/clearing control bit, TMR1ON (T1CON<0>).

Timer1 also has an internal "Reset input". This Reset can be generated by the CCP1 module as the special event trigger (see **Section 9.1** "**Capture Mode**"). Register 7-1 shows the Timer1 Control register.

When the Timer1 oscillator is enabled (T1OSCEN is set), the RB6/T1OSO/T1CKI/PGC and RB7/T1OSI/ PGD pins become inputs. That is, the TRISB<7:6> value is ignored and these pins read as '0'.

Additional information on timer modules is available in the "*PIC*<sup>®</sup> *Mid-Range MCU Family Reference Manual*" (DS33023).

#### REGISTER 7-1: T1CON: TIMER1 CONTROL REGISTER (ADDRESS 10h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_		T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N
bit 7							bit 0

bit 7-6	Unimplemented: Read	<b>as</b> '0'									
bit 5-4	T1CKPS1:T1CKPS0: Ti	mer1 Input Clock Presc	ale Select bits								
	11 = 1:8 Prescale value	11 = 1:8 Prescale value									
	10 = 1:4 Prescale value										
	01 = 1:2 Prescale value										
<b>L</b> H 0	00 = 111  Prescale value										
DILS		INALOF ENABLE CONTROL DIL									
	1 = Oscillator is enabled 0 = Oscillator is shut-off	(the oscillator inverter is	s turned off to eliminate power drain)								
hit 2	TISYNC: Timer1 Extern	al Clock Input Synchror	nization Control bit								
5112	TMR1CS = $1^{\circ}$										
	1 = Do not synchronize external clock input										
	0 = Synchronize externa	I clock input									
	<u>TMR1CS = 0:</u>										
	This bit is ignored. Time	r1 uses the internal cloc	k when TMR1CS = 0.								
bit 1	TMR1CS: Timer1 Clock Source Select bit										
	1 = External clock from 0 = Internal clock (Eosc	pin RB6/T1OSO/T1CKI	/PGC (on the rising edge)								
bit 0	TMR10N: Timer1 On bit	t i									
	1 = Enables Timer1										
	0 = Stops Timer1										
	Legend:										
	R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'								

R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

EXAMPLE 7-3:	IMPLEMENTING A REAL-TIME CLOCK USING A TIMER1 INTERRUPT SERVICE
-	

RTCinit	BANKSEL	TMR1H		
	MOVLW	0x80	;	Preload TMR1 register pair
	MOVWF	TMR1H	;	for 1 second overflow
	CLRF	TMR1L		
	MOVLW	b'00001111'	;	Configure for external clock,
	MOVWF	T1CON	;	Asynchronous operation, external oscillator
	CLRF	secs	;	Initialize timekeeping registers
	CLRF	mins		
	MOVLW	.12		
	MOVWF	hours		
	BANKSEL	PIE1		
	BSF	PIE1, TMR1IE	;	Enable Timer1 interrupt
	RETURN			
RTCisr	BANKSEL	TMR1H		
	BSF	TMR1H, 7	;	Preload for 1 sec overflow
	BCF	PIR1, TMR1IF	;	Clear interrupt flag
	INCF	secs, F	;	Increment seconds
	MOVF	secs, w		
	SUBLW	.60		
	BTFSS	STATUS, Z	;	60 seconds elapsed?
	RETURN	_	;	No, done
	CLRF	seconds	;	Clear seconds
	INCF	mins, f	;	Increment minutes
	MOVF	mins, w		
	SUBLW	.60		
	BTFSS	STATUS, Z	;	60 seconds elapsed?
	RETURN		;	No, done
	CLRF	mins	;	Clear minutes
	INCF	hours, f	;	Increment hours
	MOVE	hours, w		
	SUBLW	.24		
	BIFSS	STATUS, Z	;	24 nours elapsed?
	RETURN	h	;	No, done
	CLKF	nours	;	Clear nours
	RETURN		;	Doue

#### TABLE 7-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Valu POR,	e on BOR	Valu all c Res	e on other sets
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000	000x	0000	000u
0Ch	PIR1	_	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	- 0	0000	- 0	0000
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	- 0	0000	- 0	0000
0Eh	TMR1L	Holding	g Regist	er for the Le	east Signific	ant Byte of t	he 16-bit T	MR1 Regi	ster	xxxx	xxxx	uuuu	uuuu
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register						xxxx	xxxx	uuuu	uuuu		
10h	T1CON	_	_	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00	0000	uu	uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

### 11.1 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 11-2. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD), see Figure 11-2. The maximum recommended impedance for analog sources is 2.5 k\Omega. As the impedance is decreased, the acquisition time may be decreased.

After the analog input channel is selected (changed), this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 11-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

To calculate the minimum acquisition time, TACQ, see the "*PIC*<sup>®</sup> *Mid-Range MCU Family Reference Manual*" (DS33023).

#### EQUATION 11-1: ACQUISITION TIME

TACQ = Amplifier Settling Time + Hold Capacitor Charging Time + Temperature Coefficient = TAMP + TC + TCOFF  $= 2 \mu s + TC + [(Temperature - 25^{\circ}C)(0.05 \mu s/^{\circ}C)]$  TC = CHOLD (RIC + Rss + Rs) In(1/2047)  $= -120 pF (1 k\Omega + 7 k\Omega + 10 k\Omega) In(0.0004885)$   $= 16.47 \mu s$   $TACQ = 2 \mu s + 16.47 \mu s + [(50^{\circ}C - 25^{\circ}C)(0.05 \mu s/^{\circ}C)]$   $= 19.72 \mu s$ 

Note 1: The reference voltage (VREF) has no effect on the equation since it cancels itself out.

- **2:** The charge holding capacitor (CHOLD) is not discharged after each conversion.
- **3:** The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.
- **4:** After a conversion has completed, a 2.0 TAD delay must complete before acquisition can begin again. During this time, the holding capacitor is not connected to the selected A/D input channel.

#### FIGURE 11-2: ANALOG INPUT MODEL



NOTES:

## 12.0 SPECIAL FEATURES OF THE CPU

These devices have a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power-saving operating modes and offer code protection:

- Reset
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- Sleep
- Code Protection
- ID Locations
- In-Circuit Serial Programming

There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT) which provides a fixed delay of 72 ms (nominal) on power-up only. It is designed to keep the part in Reset while the power supply stabilizes and is enabled or disabled using a configuration bit. With these two timers on-chip, most applications need no external Reset circuitry. Sleep mode is designed to offer a very low-current power-down mode. The user can wake-up from Sleep through external Reset, Watchdog Timer wake-up or through an interrupt.

Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. Configuration bits are used to select the desired oscillator mode.

Additional information on special features is available in the "PIC<sup>®</sup> Mid-Range MCU Family Reference Manual" (DS33023).

### 12.1 Configuration Bits

The configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space which can be accessed only during programming.

#### 12.9 Power Control/Status Register (PCON)

The Power Control/Status register, PCON, has two bits to indicate the type of Reset that last occurred.

Bit 0 is Brown-out Reset Status bit,  $\overline{\text{BOR}}$ . Bit  $\overline{\text{BOR}}$  is unknown on a Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if

# bit BOR cleared, indicating a Brown-out Reset occurred. When the Brown-out Reset is disabled, the state of the BOR bit is unpredictable.

Bit 1 is Power-on Reset Status bit,  $\overline{\text{POR}}$ . It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

### TABLE 12-1: TIME-OUT IN VARIOUS SITUATIONS

Oscillator	Power-u	p	Brown-out R	Brown-out Reset			
Configuration	PWRTE = 0	PWRTE = 1	PWRTE = 0	PWRTE = 1	from Sleep		
XT, HS, LP	TPWRT + 1024 • TOSC	1024 • Tosc	TPWRT + 1024 • TOSC	1024 • Tosc	1024 • Tosc		
EXTRC, EXTCLK, INTRC	TPWRT	5-10 μs <b>(1)</b>	Tpwrt	5-10 μs <sup>(1)</sup>	5-10 μs <b>(1)</b>		

**Note 1:** CPU start-up is always invoked on POR, BOR and wake-up from Sleep.

#### TABLE 12-2: STATUS BITS AND THEIR SIGNIFICANCE

POR	BOR	ТО	PD	
0	x	1	1	Power-on Reset
0	x	0	x	Illegal, TO is set on POR
0	x	x	0	Illegal, PD is set on POR
1	0	1	1	Brown-out Reset
1	1	0	1	WDT Reset
1	1	0	0	WDT wake-up
1	1	u	u	MCLR Reset during normal operation
1	1	1	0	MCLR Reset during Sleep or interrupt wake-up from Sleep

**Legend:** u = unchanged, x = unknown

#### TABLE 12-3: RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	Status Register	PCON Register
Power-on Reset	000h	0001 1xxx	0x
MCLR Reset during normal operation	000h	000u uuuu	uu
MCLR Reset during Sleep	000h	0001 Ouuu	uu
WDT Reset	000h	0000 luuu	uu
WDT wake-up	PC + 1	uuu0 0uuu	uu
Brown-out Reset	000h	0001 luuu	u0
Interrupt wake-up from Sleep	PC + 1 <sup>(1)</sup>	uuul Ouuu	uu

**Legend:** u = unchanged, x = unknown, - = unimplemented bit, read as '0'

**Note 1:** When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

# 14.0 DEVELOPMENT SUPPORT

The PIC<sup>®</sup> microcontrollers and dsPIC<sup>®</sup> digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
- MPLAB<sup>®</sup> IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB C Compiler for Various Device Families
  - HI-TECH C<sup>®</sup> for Various Device Families
  - MPASM<sup>™</sup> Assembler
  - MPLINK<sup>™</sup> Object Linker/ MPLIB<sup>™</sup> Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
  - MPLAB ICD 3
  - PICkit<sup>™</sup> 3 Debug Express
- Device Programmers
  - PICkit<sup>™</sup> 2 Programmer
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

### 14.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows<sup>®</sup> operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - In-Circuit Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- · A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (C or assembly)
  - Mixed C and assembly
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

### 15.2 DC Characteristics: Power-Down and Supply Current PIC16F818/819 (Industrial, Extended) PIC16LF818/819 (Industrial)

PIC16LF (Indus	Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial								
PIC16F8 <sup>,</sup> (Indus	Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended								
Param No.	Тур	Max	Units		Conditions				
	Power-Down Current (IPD)	(1)							
	PIC16LF818/819	0.1	0.4	μΑ	-40°C				
		0.1	0.4	μΑ	+25°C	VDD = 2.0V			
		0.4	1.5	μΑ	+85°C				
	PIC16LF818/819	0.3	0.5	μΑ	-40°C				
		0.3	0.5	μΑ	+25°C	VDD = 3.0V			
		0.7	1.7	μΑ	+85°C				
	All devices Extended devices		1.0	μΑ	-40°C				
			1.0	μA	+25°C				
			5.0	μA	+85°C	VDD = 5.0V			
			28	μA	+125°C				

Legend: Shading of rows is to assist in readability of the table.

**Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSs and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

- OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
- MCLR = VDD; WDT enabled/disabled as specified.
- **3:** For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.



#### TABLE 15-1: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
	Fosc	External CLKI Frequency (Note 1)	DC		1	MHz	XT and RC Oscillator mode
			DC	—	20	MHz	HS Oscillator mode
			DC	_	32	kHz	LP Oscillator mode
		Oscillator Frequency (Note 1)	DC		4	MHz	RC Oscillator mode
			0.1	—	4	MHz	XT Oscillator mode
			4	—	20	MHz	HS Oscillator mode
			5	_	200	kHz	LP Oscillator mode
1	Tosc	External CLKI Period (Note 1)	1000	—	_	ns	XT and RC Oscillator mode
			50	—	_	ns	HS Oscillator mode
			5	_		ms	LP Oscillator mode
		Oscillator Period (Note 1)	250		_	ns	RC Oscillator mode
			250	—	10,000	ns	XT Oscillator mode
			50	—	250	ns	HS Oscillator mode
			5	_	—	ms	LP Oscillator mode
2	Тсү	Instruction Cycle Time (Note 1)	200	Тсү	DC	ns	TCY = 4/FOSC
3	TosL,	External Clock in (OSC1) High	500	_	_	ns	XT Oscillator
	TosH	or Low Time	2.5	—	—	ms	LP Oscillator
			15	—	—	ns	HS Oscillator
4	TosR,	External Clock in (OSC1) Rise or	—	_	25	ns	XT Oscillator
	TosF	Fall Time	—	—	50	ns	LP Oscillator
			—	—	15	ns	HS Oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type, under standard operating conditions, with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin. When an external clock input is used, the "max." cycle time limit is "DC" (no clock) for all devices.



# FIGURE 15-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

### FIGURE 15-7: BROWN-OUT RESET TIMING



# TABLE 15-3:RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER<br/>AND BROWN-OUT RESET REQUIREMENTS

Param No.	Symbol	Characteristic		Тур†	Max	Units	Conditions
30	TMCL	MCLR Pulse Width (Low)	2			μS	VDD = 5V, -40°C to +85°C
31*	Twdt	Watchdog Timer Time-out Period (no prescaler)	13.6	16	18.4	ms	VDD = 5V, -40°C to +85°C
32	Tost	Oscillation Start-up Timer Period	_	1024 Tosc	_	_	Tosc = OSC1 period
33*	TPWRT	Power-up Timer Period	61.2	72	82.8	ms	VDD = 5V, -40°C to +85°C
34	Tioz	I/O High-Impedance from MCLR Low or Watchdog Timer Reset		—	2.1	μS	
35	TBOR	Brown-out Reset Pulse Width	100	—	—	μS	$VDD \leq VBOR$ (D005)

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.





Param No.	Symbol	Characte	Min	Тур†	Max	Units	Conditions	
130	TAD	A/D Clock Period PIC16F818/819		1.6	—	_	μS	Tosc based, VREF $\ge 3.0V$
			PIC16LF818/819	3.0	_		μs	Tosc based, VREF $\ge 2.0V$
			PIC16F818/819	2.0	4.0	6.0	μs	A/D RC mode
			PIC16LF818/819	3.0	6.0	9.0	μs	A/D RC mode
131	TCNV	Conversion Time (not i (Note 1)		—	12	TAD		
132	TACQ	Acquisition Time		(Note 2)	40	—	μS	
				10*	_	_	μs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1 LSb (i.e., 5.0 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD).
134	TGO	Q4 to A/D Clock Start		_	Tosc/2 §	_	—	If the A/D clock source is selected as RC, a time of Tcy is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

#### TABLE 15-10: A/D CONVERSION REQUIREMENTS

These parameters are characterized but not tested.

Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are t not tested.

§ This specification ensured by design.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 11.1 "A/D Acquisition Requirements" for minimum conditions.