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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f819-i-mltsl

Table of Contents

1.0	Device Overview	5
2.0	Memory Organization	9
3.0	Data EEPROM and Flash Program Memory	25
4.0	Oscillator Configurations	33
5.0	I/O Ports	39
6.0	Timer0 Module	53
7.0	Timer1 Module	57
8.0	Timer2 Module	63
9.0	Capture/Compare/PWM (CCP) Module	65
10.0	Synchronous Serial Port (SSP) Module	71
11.0	Analog-to-Digital Converter (A/D) Module	81
12.0	Special Features of the CPU	89
13.0	Instruction Set Summary	103
14.0	Development Support	111
15.0	Electrical Characteristics	115
16.0	DC and AC Characteristics Graphs and Tables	141
17.0	Packaging Information	155
	Appendix A: Revision History	165
	Appendix B: Device Differences	165
	INDEX	167
	The Microchip Web Site	173
	Customer Change Notification Service	173
	Customer Support	173
	Reader Response	174
	PIC16F818/819 Product Identification System	175

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PIC16F818/819

TABLE 1-2: PIC16F818/819 PINOUT DESCRIPTIONS (CONTINUED)

Pin Name	PDIP/ SOIC Pin#	SSOP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
RB0/INT RB0 INT	6	7	7	I/O I	TTL ST ⁽¹⁾	PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs. Bidirectional I/O pin. External interrupt pin.
RB1/SDI/SDA RB1 SDI SDA	7	8	8	I/O I I/O	TTL ST ST	Bidirectional I/O pin. SPI data in. I ² C™ data.
RB2/SDO/CCP1 RB2 SDO CCP1	8	9	9	I/O O I/O	TTL ST ST	Bidirectional I/O pin. SPI data out. Capture input, Compare output, PWM output.
RB3/CCP1/PGM RB3 CCP1 PGM	9	10	10	I/O I/O I	TTL ST ST	Bidirectional I/O pin. Capture input, Compare output, PWM output. Low-Voltage ICSP™ Programming enable pin.
RB4/SCK/SCL RB4 SCK SCL	10	11	12	I/O I/O I	TTL ST ST	Bidirectional I/O pin. Interrupt-on-change pin. Synchronous serial clock input/output for SPI. Synchronous serial clock input for I ² C.
RB5/ \overline{SS} RB5 \overline{SS}	11	12	13	I/O I	TTL TTL	Bidirectional I/O pin. Interrupt-on-change pin. Slave select for SPI in Slave mode.
RB6/T1OSO/T1CKI/PGC RB6 T1OSO T1CKI PGC	12	13	15	I/O O I I	TTL ST ST ST ⁽²⁾	Interrupt-on-change pin. Timer1 Oscillator output. Timer1 clock input. In-circuit debugger and ICSP programming clock pin.
RB7/T1OSI/PGD RB7 T1OSI PGD	13	14	16	I/O I I	TTL ST ST ⁽²⁾	Interrupt-on-change pin. Timer1 oscillator input. In-circuit debugger and ICSP programming data pin.
Vss	5	5, 6	3, 5	P	–	Ground reference for logic and I/O pins.
VDD	14	15, 16	17, 19	P	–	Positive supply for logic and I/O pins.

Legend: I = Input O = Output I/O = Input/Output P = Power
– = Not used TTL = TTL Input ST = Schmitt Trigger Input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

PIC16F818/819

2.2.2.3 INTCON Register

The INTCON register is a readable and writable register that contains various enable and flag bits for the TMR0 register overflow, RB port change and external RB0/INT pin interrupts.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the Global Interrupt Enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTCON: INTERRUPT CONTROL REGISTER (ADDRESS 0Bh, 8Bh, 10Bh, 18Bh)

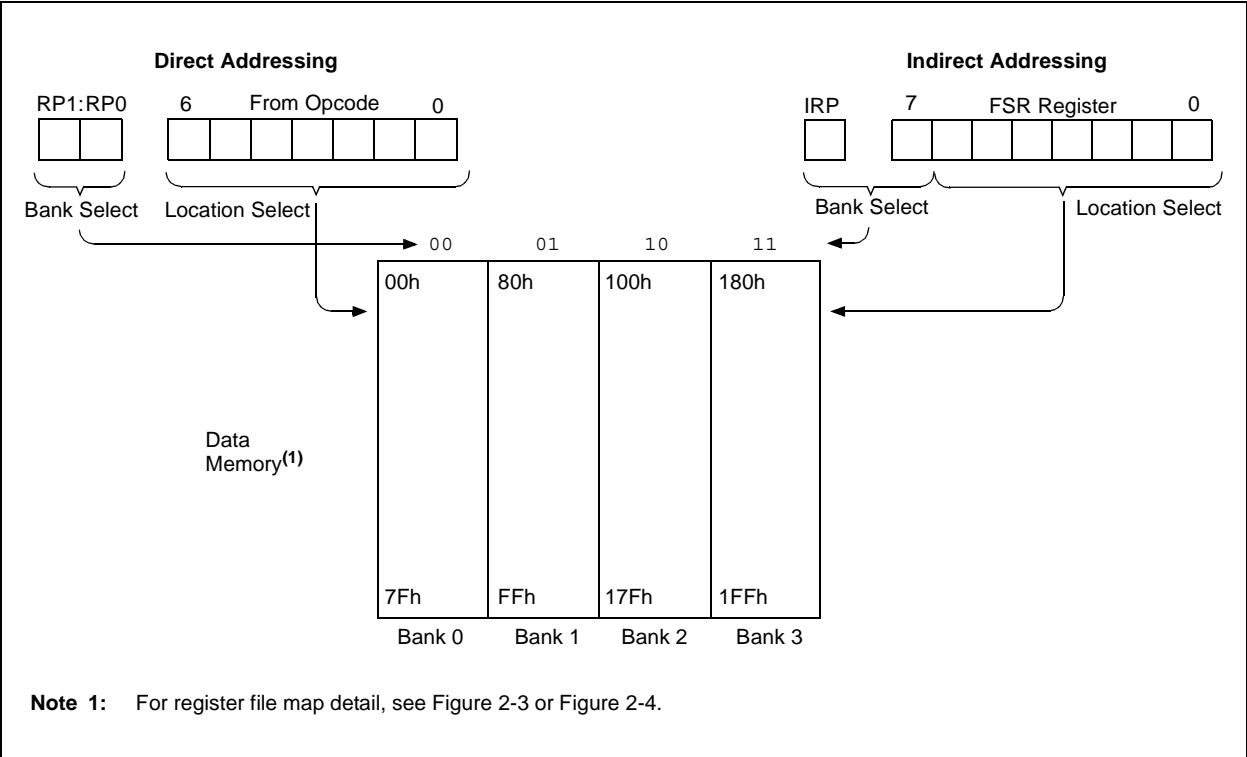
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF
bit 7							bit 0

- bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts
- bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts
- bit 5 **TMR0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt
- bit 4 **INTE:** RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt
- bit 3 **RBIE:** RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt
- bit 2 **TMR0IF:** TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow
- bit 1 **INTF:** RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur
- bit 0 **RBIF:** RB Port Change Interrupt Flag bit
A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.
1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

FIGURE 2-6: DIRECT/INDIRECT ADDRESSING



An example of the complete four-word write sequence is shown in Example 3-5. The initial address is loaded into the EEADRH:EEADR register pair; the four words of data are loaded using indirect addressing, assuming that a row erase sequence has already been performed.

EXAMPLE 3-5: WRITING TO FLASH PROGRAM MEMORY

```
; This write routine assumes the following:

; 1. The 32 words in the erase block have already been erased.
; 2. A valid starting address (the least significant bits = '00') is loaded into EEADRH:EEADR
; 3. This example is starting at 0x100, this is an application dependent setting.
; 4. The 8 bytes (4 words) of data are loaded, starting at an address in RAM called ARRAY.
; 5. This is an example only, location of data to program is application dependent.
; 6. word_block is located in data memory.

        BANKSEL EECON1           ;prepare for WRITE procedure
        BSF      EECON1, EEPGD    ;point to program memory
        BSF      EECON1, WREN     ;allow write cycles
        BCF      EECON1, FREE     ;perform write only

        BANKSEL word_block
        MOVLW    .4
        MOVWF    word_block      ;prepare for 4 words to be written

        BANKSEL EEADRH           ;Start writing at 0x100
        MOVLW    0x01
        MOVWF    EEADRH          ;load HIGH address
        MOVLW    0x00
        MOVWF    EEADR           ;load LOW address
        BANKSEL ARRAY
        MOVLW    ARRAY           ;initialize FSR to start of data
        MOVWF    FSR

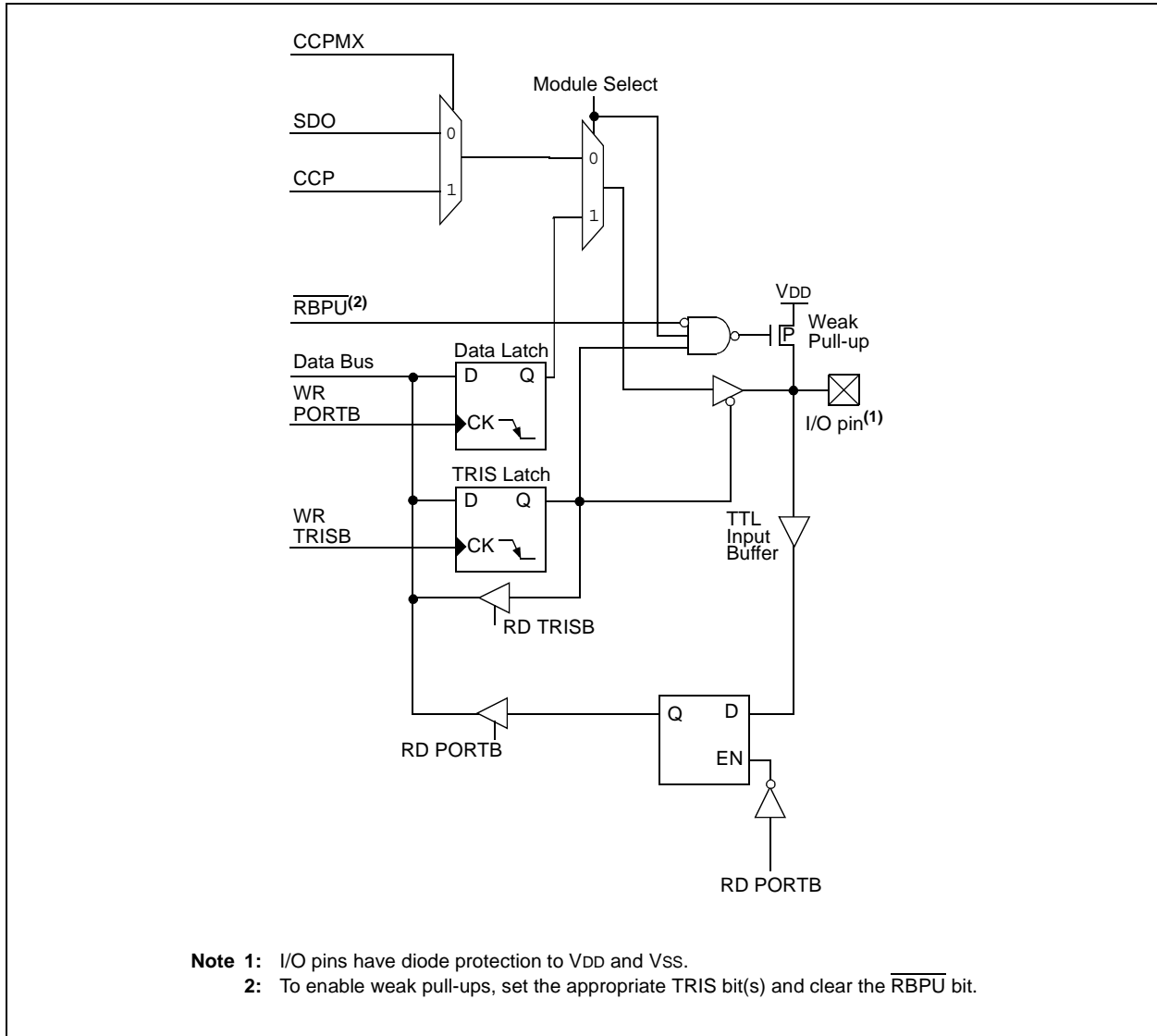
LOOP
        BANKSEL EEDATA
        MOVF     INDF, W          ;indirectly load EEDATA
        MOVWF    EEDATA
        INCF     FSR, F           ;increment data pointer
        MOVF     INDF, W          ;indirectly load EEDATH
        MOVWF    EEDATH
        INCF     FSR, F           ;increment data pointer

        BANKSEL EECON1
        MOVLW    0x55             ;required sequence
        MOVWF    EECON2
        MOVLW    0xAA
        MOVWF    EECON2
        BSF      EECON1, WR       ;set WR bit to begin write
        NOP      ;instructions here are ignored as processor
        NOP

        BANKSEL EEADR
        INCF     EEADR, f         ;load next word address
        BANKSEL word_block
        DECFSZ   word_block, f    ;have 4 words been written?
        GOTO     loop            ;NO, continue with writing

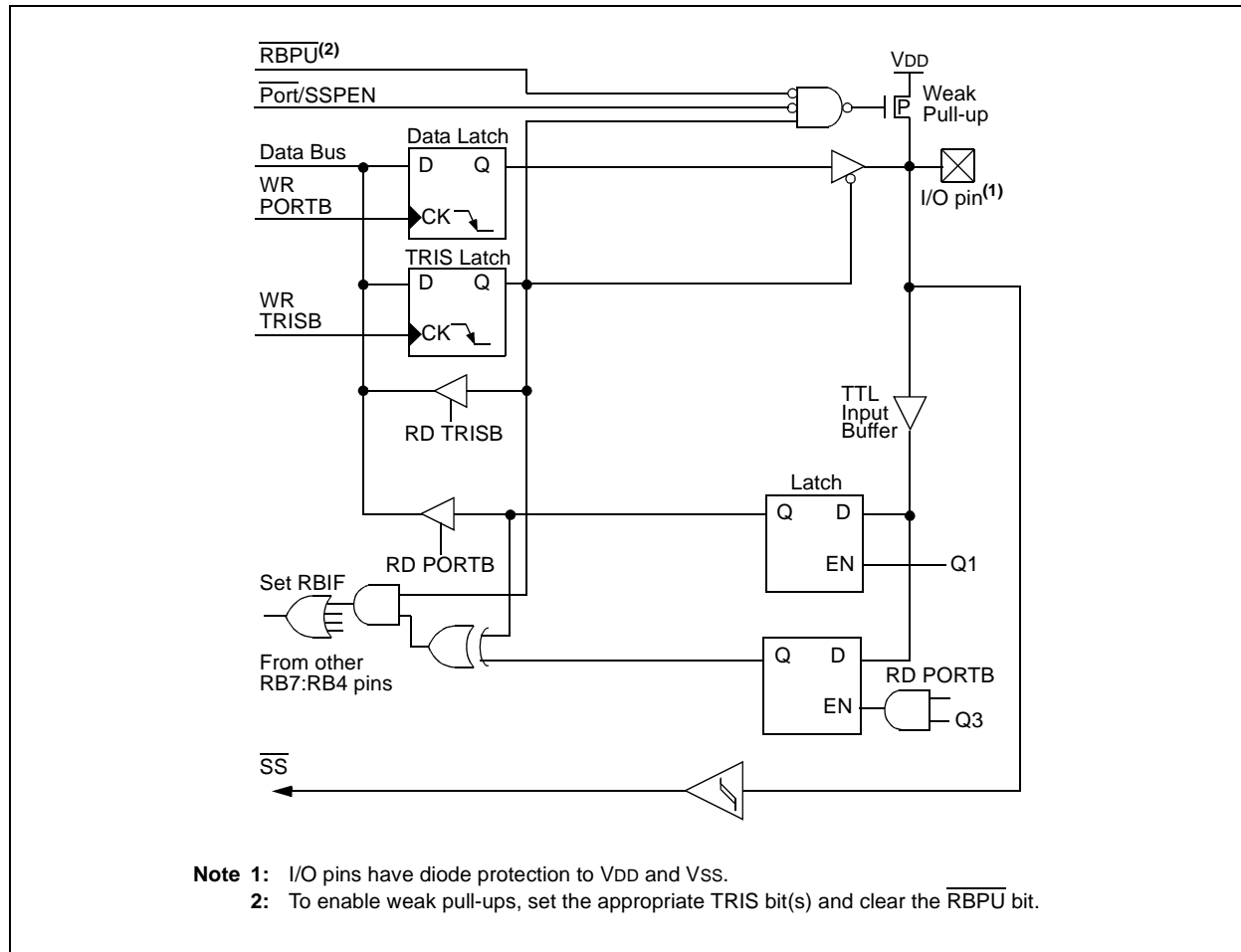
        BANKSEL EECON1
        BCF      EECON1, WREN     ;YES, 4 words complete, disable writes
        BSF      INTCON, GIE      ;enable interrupts
```

FIGURE 5-10: BLOCK DIAGRAM OF RB2 PIN



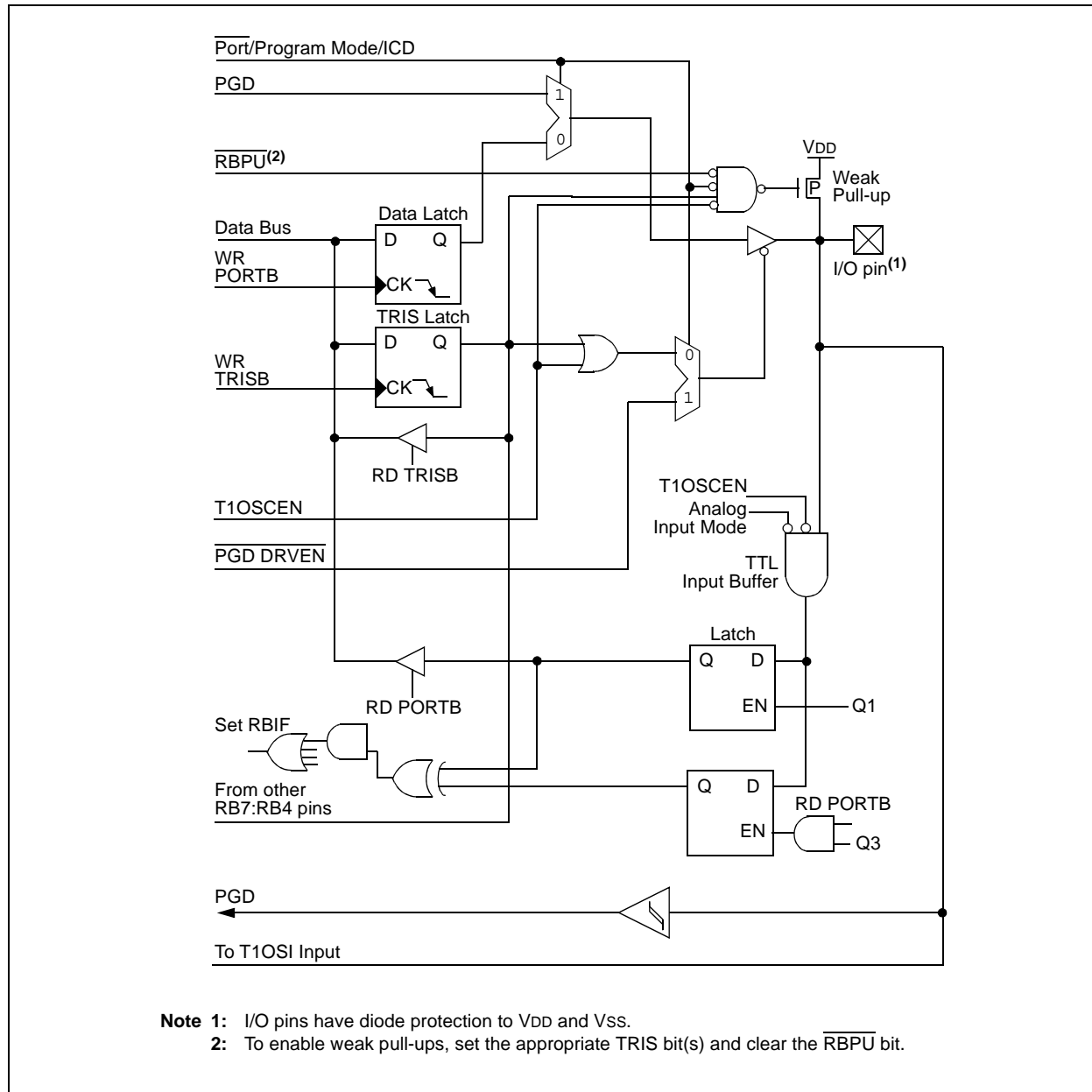
PIC16F818/819

FIGURE 5-13: BLOCK DIAGRAM OF RB5 PIN



PIC16F818/819

FIGURE 5-15: BLOCK DIAGRAM OF RB7 PIN



PIC16F818/819

6.3 Using Timer0 with an External Clock

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least 2 TOSC (and a small RC delay of 20 ns) and low for at least 2 TOSC (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

6.4 Prescaler

There is only one prescaler available which is mutually exclusively shared between the Timer0 module and the Watchdog Timer. A prescaler assignment for the

Timer0 module means that there is no prescaler for the Watchdog Timer and vice versa. This prescaler is not readable or writable (see Figure 6-1).

The PSA and PS2:PS0 bits (OPTION_REG<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1, x....etc.) will clear the prescaler. When assigned to WDT, a CLRWDI instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.

Note: Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count but will not change the prescaler assignment.

REGISTER 6-1: OPTION_REG: OPTION REGISTER (ADDRESS 81h, 181h)

	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	RBPUP	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
	bit 7							bit 0
bit 7	RBPUP: PORTB Pull-up Enable bit 1 = PORTB pull-ups are disabled 0 = PORTB pull-ups are enabled by individual port latch values							
bit 6	INTEDG: Interrupt Edge Select bit 1 = Interrupt on rising edge of RB0/INT pin 0 = Interrupt on falling edge of RB0/INT pin							
bit 5	T0CS: TMR0 Clock Source Select bit 1 = Transition on T0CKI pin 0 = Internal instruction cycle clock (CLKO)							
bit 4	T0SE: TMR0 Source Edge Select bit 1 = Increment on high-to-low transition on T0CKI pin 0 = Increment on low-to-high transition on T0CKI pin							
bit 3	PSA: Prescaler Assignment bit 1 = Prescaler is assigned to the WDT 0 = Prescaler is assigned to the Timer0 module							
bit 2-0	PS2:PS0: Prescaler Rate Select bits							
	Bit Value	TMR0 Rate	WDT Rate					
	000	1 : 2	1 : 1					
	001	1 : 4	1 : 2					
	010	1 : 8	1 : 4					
	011	1 : 16	1 : 8					
	100	1 : 32	1 : 16					
	101	1 : 64	1 : 32					
	110	1 : 128	1 : 64					
	111	1 : 256	1 : 128					

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

Note: To avoid an unintended device Reset, the instruction sequence shown in the "PIC® Mid-Range MCU Family Reference Manual" (DS33023) must be executed when changing the prescaler assignment from Timer0 to the WDT. This sequence must be followed even if the WDT is disabled.

7.0 TIMER1 MODULE

The Timer1 module is a 16-bit timer/counter consisting of two 8-bit registers (TMR1H and TMR1L) which are readable and writable. The TMR1 register pair (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The TMR1 interrupt, if enabled, is generated on overflow which is latched in interrupt flag bit, TMR1IF (PIR1<0>). This interrupt can be enabled/disabled by setting/clearing TMR1 Interrupt Enable bit, TMR1IE (PIE1<0>).

Timer1 can also be used to provide Real-Time Clock (RTC) functionality to applications with only a minimal addition of external components and code overhead.

7.1 Timer1 Operation

Timer1 can operate in one of three modes:

- as a timer
- as a synchronous counter
- as an asynchronous counter

The operating mode is determined by the clock select bit, TMR1CS (T1CON<1>).

In Timer mode, Timer1 increments every instruction cycle. In Counter mode, it increments on every rising edge of the external clock input.

Timer1 can be enabled/disabled by setting/clearing control bit, TMR1ON (T1CON<0>).

Timer1 also has an internal "Reset input". This Reset can be generated by the CCP1 module as the special event trigger (see **Section 9.1 "Capture Mode"**). Register 7-1 shows the Timer1 Control register.

When the Timer1 oscillator is enabled (T1OSCEN is set), the RB6/T1OSO/T1CKI/PGC and RB7/T1OSI/PGD pins become inputs. That is, the TRISB<7:6> value is ignored and these pins read as '0'.

Additional information on timer modules is available in the "PIC® Mid-Range MCU Family Reference Manual" (DS33023).

REGISTER 7-1: T1CON: TIMER1 CONTROL REGISTER (ADDRESS 10h)

	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNCR	TMR1CS	TMR1ON
bit 7								bit 0
bit 7-6	Unimplemented: Read as '0'							
bit 5-4	T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits							
	11 = 1:8 Prescale value							
	10 = 1:4 Prescale value							
	01 = 1:2 Prescale value							
	00 = 1:1 Prescale value							
bit 3	T1OSCEN: Timer1 Oscillator Enable Control bit							
	1 = Oscillator is enabled							
	0 = Oscillator is shut-off (the oscillator inverter is turned off to eliminate power drain)							
bit 2	T1SYNCR: Timer1 External Clock Input Synchronization Control bit							
	<u>TMR1CS = 1:</u>							
	1 = Do not synchronize external clock input							
	0 = Synchronize external clock input							
	<u>TMR1CS = 0:</u>							
	This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.							
bit 1	TMR1CS: Timer1 Clock Source Select bit							
	1 = External clock from pin RB6/T1OSO/T1CKI/PGC (on the rising edge)							
	0 = Internal clock (FOSC/4)							
bit 0	TMR1ON: Timer1 On bit							
	1 = Enables Timer1							
	0 = Stops Timer1							

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

PIC16F818/819

EXAMPLE 7-3: IMPLEMENTING A REAL-TIME CLOCK USING A TIMER1 INTERRUPT SERVICE

```

RTCinit    BANKSEL    TMR1H
           MOVLW      0x80          ; Preload TMR1 register pair
           MOVWF      TMR1H        ; for 1 second overflow
           CLRF       TMR1L
           MOVLW      b'00001111'  ; Configure for external clock,
           MOVWF      T1CON        ; Asynchronous operation, external oscillator
           CLRF       secs         ; Initialize timekeeping registers
           CLRF       mins
           MOVLW      .12
           MOVWF      hours
           BANKSEL    PIE1
           BSF        PIE1, TMR1IE ; Enable Timer1 interrupt
           RETURN

RTCisr     BANKSEL    TMR1H
           BSF        TMR1H, 7      ; Preload for 1 sec overflow
           BCF        PIR1, TMR1IF  ; Clear interrupt flag
           INCF       secs, F       ; Increment seconds
           MOVF       secs, w
           SUBLW      .60
           BTFS      STATUS, Z      ; 60 seconds elapsed?
           RETURN          ; No, done
           CLRF       seconds       ; Clear seconds
           INCF       mins, f       ; Increment minutes
           MOVF       mins, w
           SUBLW      .60
           BTFS      STATUS, Z      ; 60 seconds elapsed?
           RETURN          ; No, done
           CLRF       mins         ; Clear minutes
           INCF       hours, f      ; Increment hours
           MOVF       hours, w
           SUBLW      .24
           BTFS      STATUS, Z      ; 24 hours elapsed?
           RETURN          ; No, done
           CLRF       hours        ; Clear hours
           RETURN          ; Done
    
```

TABLE 7-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Bh,8Bh,10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0-- 0000	-0-- 0000
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0-- 0000	-0-- 0000
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	--00 0000	--uu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

PIC16F818/819

NOTES:

12.17 In-Circuit Serial Programming

PIC16F818/819 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data and three other lines for power, ground and the programming voltage (see Figure 12-10 for an example). This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

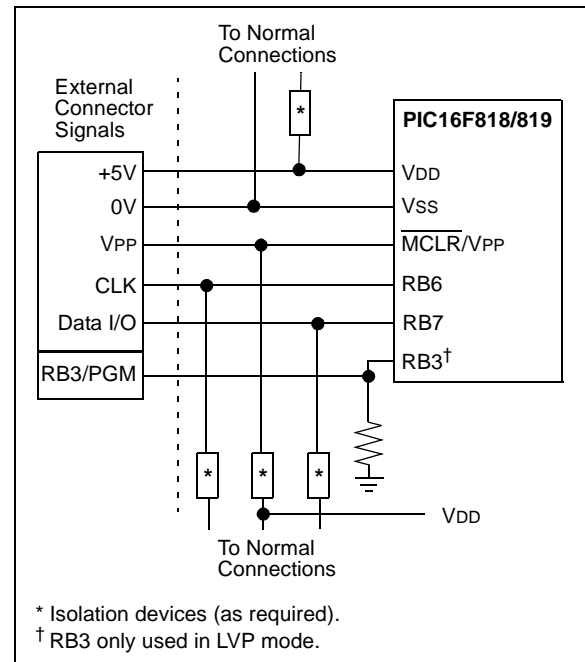
For more information on serial programming, please refer to the "PIC16F818/819 Flash Memory Programming Specification" (DS39603).

Note: The Timer1 oscillator shares the T1OSI and T1OSO pins with the PGD and PGC pins used for programming and debugging.

When using the Timer1 oscillator, In-Circuit Serial Programming™ (ICSP™) may not function correctly (high voltage or low voltage) or the In-Circuit Debugger (ICD) may not communicate with the controller. As a result of using either ICSP or ICD, the Timer1 crystal may be damaged.

If ICSP or ICD operations are required, the crystal should be disconnected from the circuit (disconnect either lead) or installed after programming. The oscillator loading capacitors may remain in-circuit during ICSP or ICD operation.

FIGURE 12-10: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



COMF	Complement f
Syntax:	[<i>label</i>] COMF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) \rightarrow (\text{destination})$
Status Affected:	Z
Description:	The contents of register 'f' are complemented. If 'd' = 0, the result is stored in W. If 'd' = 1, the result is stored back in register 'f'.

GOTO	Unconditional Branch
Syntax:	[<i>label</i>] GOTO k
Operands:	$0 \leq k \leq 2047$
Operation:	$k \rightarrow \text{PC}<10:0>$ $\text{PCLATH}<4:3> \rightarrow \text{PC}<12:11>$
Status Affected:	None
Description:	GOTO is an unconditional branch. The eleven-bit immediate value is loaded into PC bits<10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.

DECf	Decrement f
Syntax:	[<i>label</i>] DECf f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) - 1 \rightarrow (\text{destination})$
Status Affected:	Z
Description:	Decrement register 'f'. If 'd' = 0, the result is stored in the W register. If 'd' = 1, the result is stored back in register 'f'.

INCF	Increment f
Syntax:	[<i>label</i>] INCF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) + 1 \rightarrow (\text{destination})$
Status Affected:	Z
Description:	The contents of register 'f' are incremented. If 'd' = 0, the result is placed in the W register. If 'd' = 1, the result is placed back in register 'f'.

DECFSZ	Decrement f, Skip if 0
Syntax:	[<i>label</i>] DECFSZ f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) - 1 \rightarrow (\text{destination});$ skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are decremented. If 'd' = 0, the result is placed in the W register. If 'd' = 1, the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', then a NOP is executed instead, making it a 2 Tcy instruction.

INCFSZ	Increment f, Skip if 0
Syntax:	[<i>label</i>] INCFSZ f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) + 1 \rightarrow (\text{destination});$ skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are incremented. If 'd' = 0, the result is placed in the W register. If 'd' = 1, the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a 2 Tcy instruction.

15.4 DC Characteristics: PIC16F818/819 (Industrial, Extended) PIC16LF818/819 (Industrial) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended Operating voltage VDD range as described in Section 15.1 “DC Characteristics: Supply Voltage” .				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D080	VOL	Output Low Voltage					
		I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +125°C
D083		OSC2/CLKO (RC oscillator config)	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +125°C
D090	VOH	Output High Voltage					
		I/O ports (Note 3)	VDD – 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +125°C
D092		OSC2/CLKO (RC oscillator config)	VDD – 0.7	—	—	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +125°C
D100	Cosc2	Capacitive Loading Specs on Output Pins					
		OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101	CIO	All I/O pins and OSC2 (in RC mode)	—	—	50	pF	
D102	CB	SCL, SDA in I ² C™ mode	—	—	400	pF	
D120	ED	Data EEPROM Memory					
		Endurance	100K 10K	1M 100K	— —	E/W E/W	-40°C to +85°C +85°C to +125°C
D121	VDRW	VDD for read/write	VMIN	—	5.5	V	Using EECON to read/write, VMIN = min. operating voltage
D122	TDEW	Erase/write cycle time	—	4	8	ms	
D130	EP	Program Flash Memory					
		Endurance	10K 1K	100K 10K	— —	E/W E/W	-40°C to +85°C +85°C to +125°C
	VPR	VDD for read	VMIN	—	5.5	V	Using EECON to read/write, VMIN = min. operating voltage
		VDD for erase/write	VMIN	—	5.5	V	
	TPE	Erase cycle time	—	2	4	ms	
	D134	TPW	Write cycle time	—	2	4	ms

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** In RC oscillator configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PIC16F818/819 be driven with external clock in RC mode.
- 2:** The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3:** Negative current is defined as current sourced by the pin.

PIC16F818/819

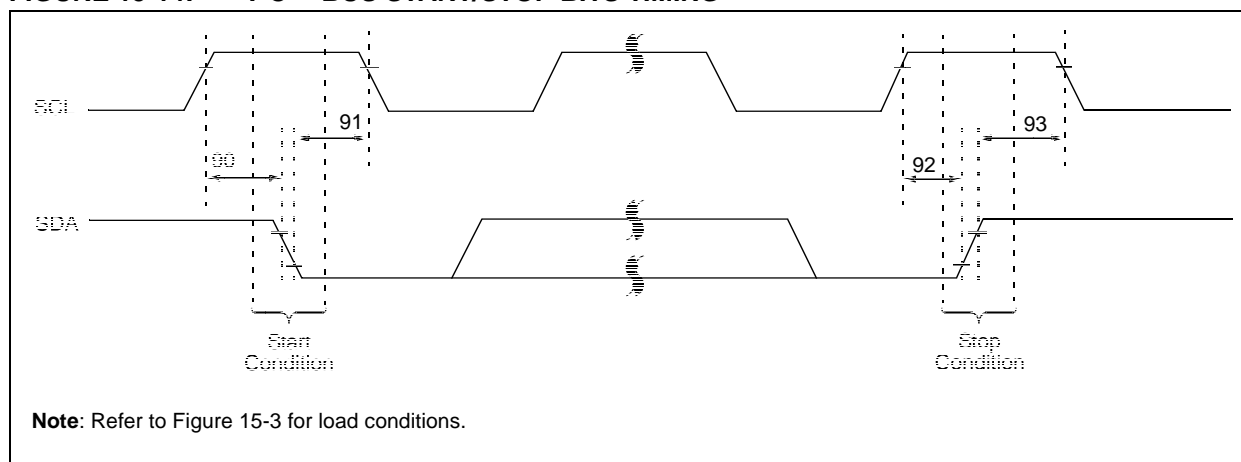
TABLE 15-6: SPI MODE REQUIREMENTS

Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
70*	TssL2sclH, TssL2sclL	\overline{SS} ↓ to SCK ↓ or SCK ↑ Input	T _{cy}	—	—	ns	
71*	Tsch	SCK Input High Time (Slave mode)	T _{cy} + 20	—	—	ns	
72*	Tscl	SCK Input Low Time (Slave mode)	T _{cy} + 20	—	—	ns	
73*	TdiV2sch, TdiV2scl	Setup Time of SDI Data Input to SCK Edge	100	—	—	ns	
74*	Tsch2diL, Tscl2diL	Hold Time of SDI Data Input to SCK Edge	100	—	—	ns	
75*	TdoR	SDO Data Output Rise Time	PIC16F818/819 — PIC16LF818/819	10 25	25 50	ns ns	
76*	TdoF	SDO Data Output Fall Time	—	10	25	ns	
77*	TssH2doZ	\overline{SS} ↑ to SDO Output High-Impedance	10	—	50	ns	
78*	Tscr	SCK Output Rise Time (Master mode)	PIC16F818/819 — PIC16LF818/819	10 25	25 50	ns ns	
79*	Tscf	SCK Output Fall Time (Master mode)	—	10	25	ns	
80*	Tsch2doV, Tscl2doV	SDO Data Output Valid after SCK Edge	PIC16F818/819 — PIC16LF818/819	— —	50 145	ns ns	
81*	TdoV2sch, TdoV2scl	SDO Data Output Setup to SCK Edge	T _{cy}	—	—	ns	
82*	Tssl2doV	SDO Data Output Valid after \overline{SS} ↓ Edge	—	—	50	ns	
83*	Tsch2ssH, Tscl2ssH	\overline{SS} ↑ after SCK Edge	1.5 T _{cy} + 40	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 15-14: I²C™ BUS START/STOP BITS TIMING



16.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

“Typical” represents the mean of the distribution at 25°C. “Maximum” or “minimum” represents (mean + 3 σ) or (mean – 3 σ) respectively, where σ is a standard deviation, over the whole temperature range.

FIGURE 16-1: TYPICAL I_{DD} vs. F_{osc} OVER V_{DD} (HS MODE)

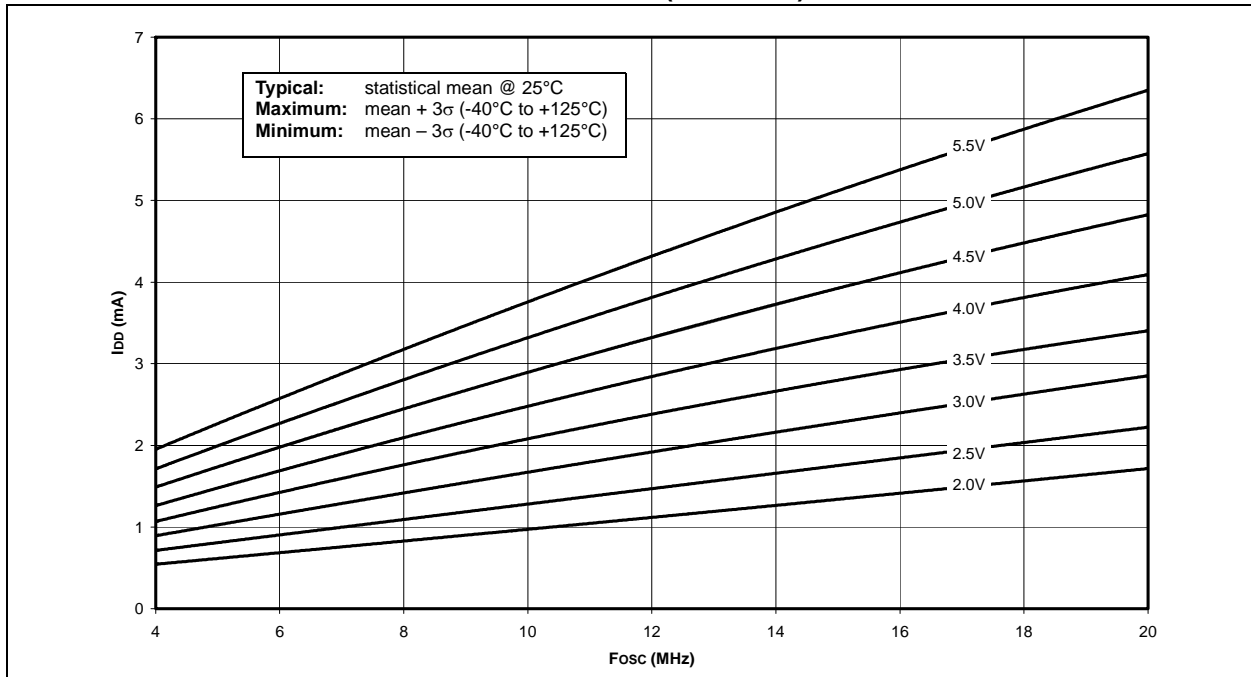


FIGURE 16-2: MAXIMUM I_{DD} vs. F_{osc} OVER V_{DD} (HS MODE)

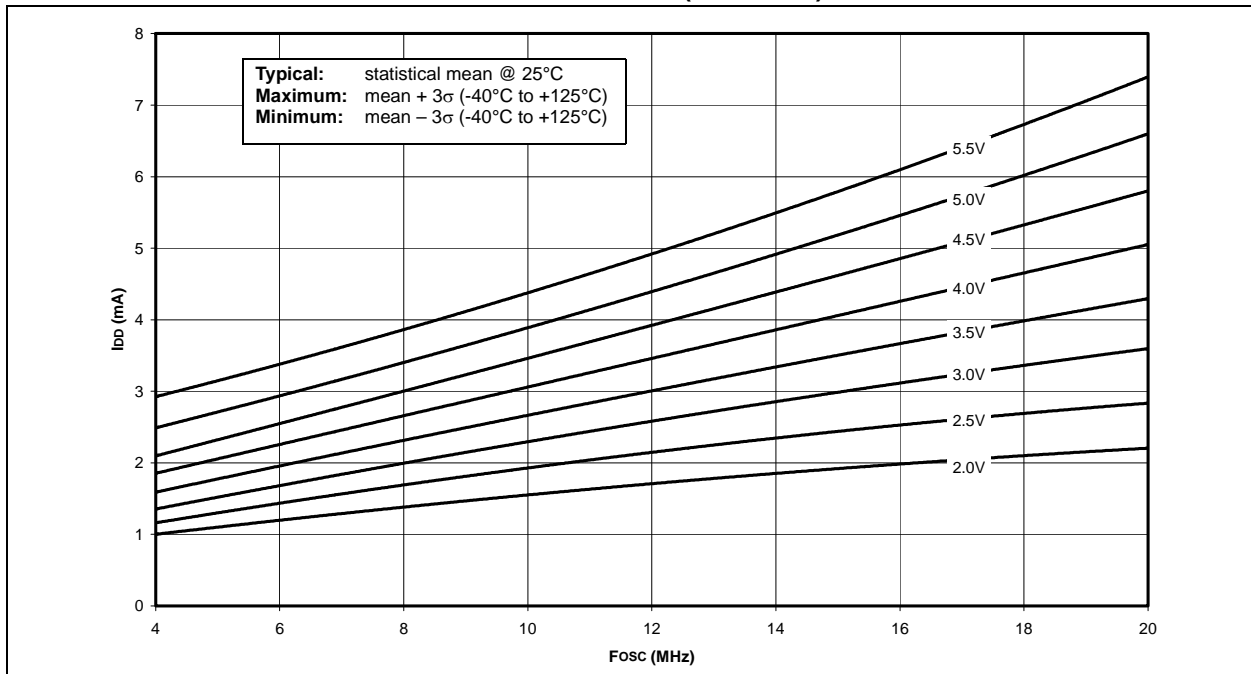
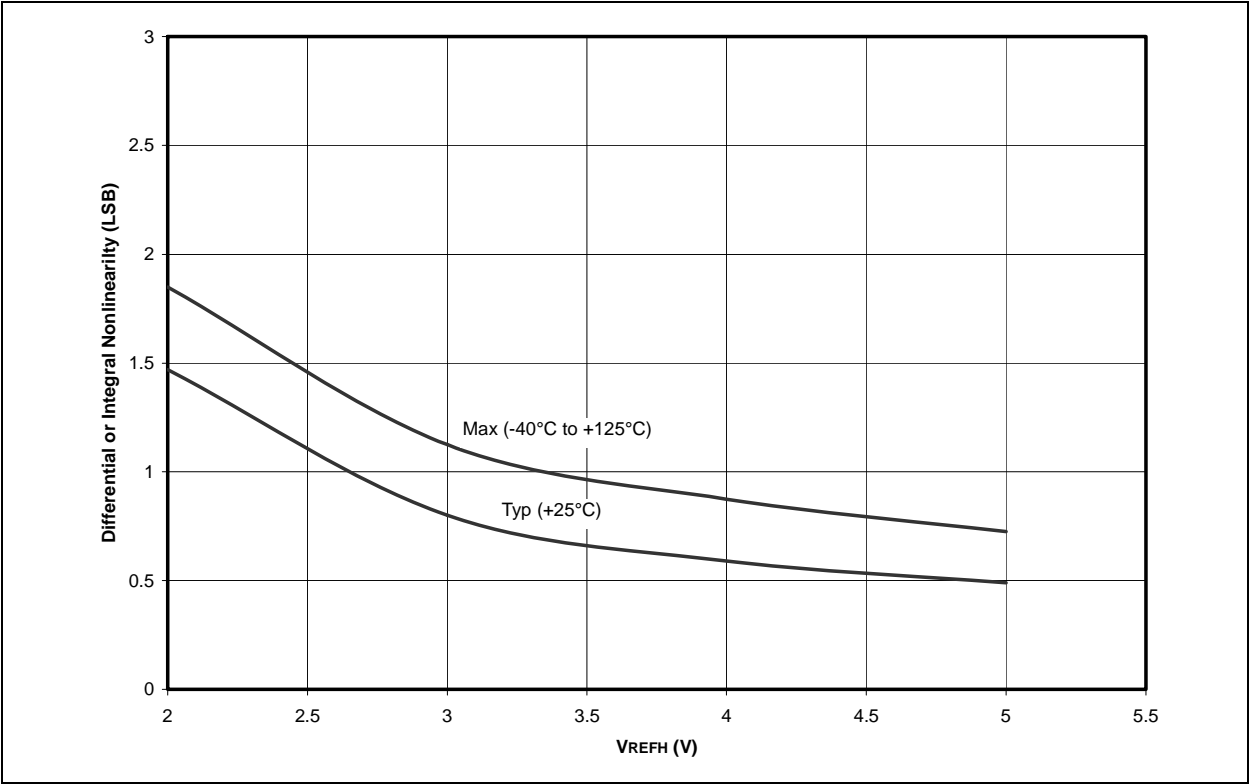
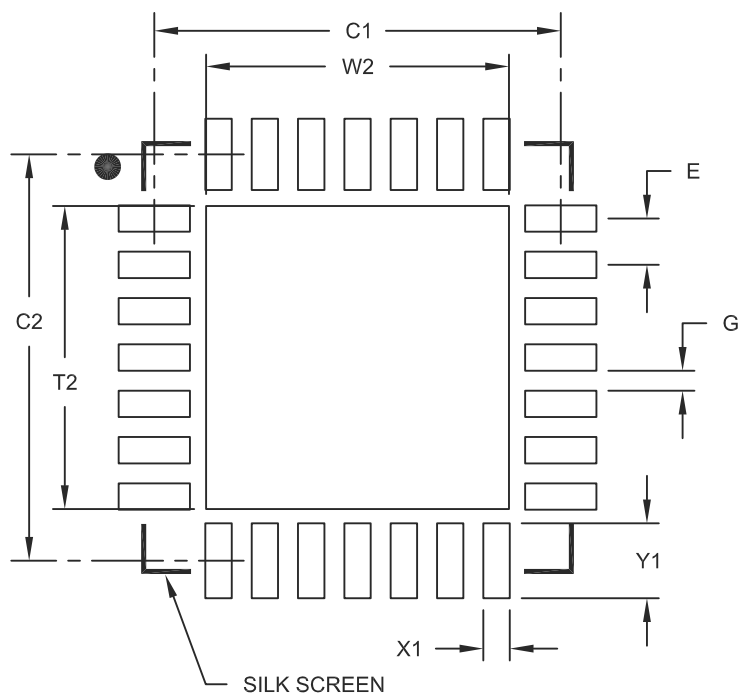


FIGURE 16-25: A/D NONLINEARITY vs. VREFH (VDD = 5V, -40°C TO +125°C)



28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

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