

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f819-i-sotsl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.0 DEVICE OVERVIEW

This document contains device specific information for the operation of the PIC16F818/819 devices. Additional information may be found in the "PIC[®] Mid-Range MCU Family Reference Manual" (DS33023) which may be downloaded from the Microchip web site. The Reference Manual should be considered a complementary document to this data sheet and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

The PIC16F818/819 belongs to the Mid-Range family of the PIC[®] devices. The devices differ from each other in the amount of Flash program memory, data memory and data EEPROM (see Table 1-1). A block diagram of the devices is shown in Figure 1-1. These devices contain features that are new to the PIC16 product line:

- Internal RC oscillator with eight selectable frequencies, including 31.25 kHz, 125 kHz, 250 kHz, 500 kHz, 1 MHz, 2 MHz, 4 MHz and 8 MHz. The INTRC can be configured as the system clock via the configuration bits. Refer to Section 4.5 "Internal Oscillator Block" and Section 12.1 "Configuration Bits" for further details.
- The Timer1 module current consumption has been greatly reduced from 20 μA (previous PIC16 devices) to 1.8 μA typical (32 kHz at 2V), which is ideal for real-time clock applications. Refer to Section 6.0 "Timer0 Module" for further details.
- The amount of oscillator selections has increased. The RC and INTRC modes can be selected with an I/O pin configured as an I/O or a clock output (Fosc/4). An external clock can be configured with an I/O pin. Refer to **Section 4.0 "Oscillator Configurations"** for further details.

TABLE 1-1:AVAILABLE MEMORY INPIC16F818/819 DEVICES

Device	Device Program Flash		Data EEPROM
PIC16F818	1K x 14	128 x 8	128 x 8

Device	Device Program Flash		Data EEPROM
PIC16F819	2K x14	256 x 8	256 x 8

There are 16 I/O pins that are user configurable on a pin-to-pin basis. Some pins are multiplexed with other device functions. These functions include:

- External Interrupt
- Change on PORTB Interrupt
- Timer0 Clock Input
- Low-Power Timer1 Clock/Oscillator
- Capture/Compare/PWM
- 10-bit, 5-channel Analog-to-Digital Converter
- SPI/I²C
- MCLR (RA5) can be configured as an Input

Table 1-2 details the pinout of the devices with descriptions and details for each pin.

FIGURE 2-4: PIC16F819 REGISTER FILE MAP

ŀ	File Address		File Address	ļ	File Address	А	Fi dd
Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	18
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	18
PCL	02h	PCL	82h	PCL	102h	PCL	1
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	1
FSR	04h	FSR	84h	FSR	104h	FSR	1
PORTA	05h	TRISA	85h		105h		1
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	1
	07h		87h		107h		1
	08h		88h		108h		18
	09h		89h		109h		18
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18
PIR1	0Ch	PIE1	8Ch	EEDATA	10Ch	EECON1	18
PIR2	0Dh	PIE2	8Dh	EEADR	10Dh	EECON2	18
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved ⁽¹⁾	18
TMR1H	0Fh	OSCCON	8Fh	EEADRH	10Fh	Reserved ⁽¹⁾	18
T1CON	10h	OSCTUNE	90h		110h		19
TMR2	11h		91h				
T2CON	12h	PR2	92h				
SSPBUE	13h	SSPADD	93h				
SSPCON	14n	SSPSTAT	94h				
	15h		95h				
	160		96h				
CCP1CON	170		97h				
	18n 10h		98h				
	1911		99n				
	1 A II 1 B b		9An ODh				
	101 10b		9BN				
			901 00b				
	1Eh	ADRESI					
	1Fh		9En 9Fh		11Fh		19
ADCONU	20h				120h		1.
	2011		AUN				
General		General		General			
Purpose		Register		Register		Accesses	
Register		80 Bytes		80 Bytes		20h-7Fh	
96 Bytes				,			
		A a a a a a a a a a a	EFh	A	16Fh		
		ACCESSES 70h-7Fh	FUN	70h-7Fh			
Bank 0	J 7Fh	Rank 1	FFh	Bank 2	17Fh	Rank 3	1
Dalik U		Dalik I		Dank Z		Dank J	





9.2 Compare Mode

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the CCP1 pin is:

- Driven high
- Driven low
- · Remains unchanged

The action on the pin is based on the value of control bits, CCP1M3:CCP1M0 (CCP1CON<3:0>). At the same time, interrupt flag bit CCP1IF is set.

FIGURE 9-2: COMPARE MODE OPERATION BLOCK DIAGRAM



9.2.1 CCP PIN CONFIGURATION

The user must configure the CCP1 pin as an output by clearing the TRISB<x> bit.

- Note 1: Clearing the CCP1CON register will force the CCP1 compare output latch to the default low level. This is not the data latch.
 - 2: The TRISB bit (2 or 3) is dependent upon the setting of configuration bit 12 (CCPMX).

9.2.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

9.2.3 SOFTWARE INTERRUPT MODE

When generate software interrupt is chosen, the CCP1 pin is not affected. Only a CCP interrupt is generated (if enabled).

9.2.4 SPECIAL EVENT TRIGGER

In this mode, an internal hardware trigger is generated that may be used to initiate an action.

The special event trigger output of CCP1 resets the TMR1 register pair and starts an A/D conversion (if the A/D module is enabled). This allows the CCPR1 register to effectively be a 16-bit programmable period register for Timer1.

Note: The special event trigger from the CCP1 module will not set interrupt flag bit, TMR1IF (PIR1<0>).

TABLE 9-2: REGISTERS ASSOCIATED WITH CAPTURE, COMPARE AND TIMER1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value POR,	e on BOR	Valu all o Res	e on ther sets
0Bh,8Bh 10BH,18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000	000x	0000	000u
0Ch	PIR1		ADIF	_	_	SSPIF	CCP1IF	TMR2IF	TMR1IF	- 0	0000	- 0	0000
8Ch	PIE1		ADIE	_		SSPIE	CCP1IE	TMR2IE	TMR1IE	- 0	0000	- 0	0000
86h	TRISB	PORTE	3 Data Dir	ection Reg	ister					1111	1111	1111	1111
0Eh	TMR1L	Holding	g Register	r for the Lea	ast Significa	ant Byte of t	he 16-bit T	MR1 Regi	ster	xxxx	xxxx	uuuu	uuuu
0Fh	TMR1H	Holding	g Register	r for the Mo	st Significa	nt Byte of th	ne 16-bit T	MR1 Regis	ster	xxxx	xxxx	uuuu	uuuu
10h	T1CON		_	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00	0000	uu	uuuu
15h	CCPR1L	Capture	Capture/Compare/PWM Register 1 (LSB)									uuuu	uuuu
16h	CCPR1H	Capture	Capture/Compare/PWM Register 1 (MSB)									uuuu	uuuu
17h	CCP1CON		_	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00	0000	00	0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by Capture and Timer1.

An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF must be cleared in software and the SSPSTAT register is used to determine the status of the byte. Flag bit SSPIF is set on the falling edge of the ninth clock pulse.

As a slave-transmitter, the \overline{ACK} pulse from the masterreceiver is latched on the rising edge of the ninth SCL input pulse. If the SDA line was high (not \overline{ACK}), then the data transfer is complete. When the \overline{ACK} is latched by the slave device, the slave logic is reset (resets SSPSTAT register) and the slave device then monitors for another occurrence of the Start bit. If the SDA line was low (\overline{ACK}), the transmit data must be loaded into the SSPBUF register which also loads the SSPSR register. Then pin RB4/SCK/SCL should be enabled by setting bit, CKP.

TABLE 10-2: DATA TRANSFER RECEIVED BYTE ACTIONS	TABLE 10-2:	DATA TRANSFER RECEIVED BYTE ACTIONS
---	-------------	-------------------------------------

Status Bits as Data Transfer is Received		$SSPSR \rightarrow SSPBUF$	Generate ACK Pulse	Set bit SSPIF
BF	SSPOV			
0	0	Yes	Yes	Yes
1	0	No	No	Yes
1	1	No	No	Yes
0	1	No	No	Yes

Note 1: Shaded cells show the conditions where the user software did not properly clear the overflow condition.

FIGURE 10-6: I²C[™] WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)



FIGURE 10-7: I²C[™] WAVEFORMS FOR TRANSMISSION (7-BIT ADDRESS)



11.4 A/D Conversions

Clearing the GO/DONE bit during a conversion will abort the current conversion. The A/D Result register pair will NOT be updated with the partially completed A/D conversion sample. That is, the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers). After the A/D conversion is aborted, a 2-TAD wait is required before the next acquisition is started. After this 2-TAD wait, acquisition on the selected channel is automatically started. The GO/DONE bit can then be set to start the conversion.

In Figure 11-3, after the GO bit is set, the first time segment has a minimum of TCY and a maximum of TAD.

Note: The GO/DONE bit should NOT be set in the same instruction that turns on the A/D.

11.4.1 A/D RESULT REGISTERS

The ADRESH:ADRESL register pair is the location where the 10-bit A/D result is loaded at the completion of the A/D conversion. This register pair is 16 bits wide. The A/D module gives the flexibility to left or right justify the 10-bit result in the 16-bit result register. The A/D Format Select bit (ADFM) controls this justification. Figure 11-4 shows the operation of the A/D result justification. The extra bits are loaded with '0's. When an A/D result will not overwrite these locations (A/D disable), these registers may be used as two general purpose 8-bit registers.

FIGURE 11-3: A/D CONVERSION TAD CYCLES



FIGURE 11-4: A/D RESULT JUSTIFICATION



12.10.1 INT INTERRUPT

External interrupt on the RB0/INT pin is edge triggered, either rising if bit INTEDG (OPTION_REG<6>) is set, or falling if the INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, flag bit, INTF (INTCON<1>), is set. This interrupt can be disabled by clearing enable bit, INTE (INTCON<4>). Flag bit INTF must be cleared in software in the Interrupt Service Routine before re-enabling this interrupt. The INT interrupt can wake-up the processor from Sleep if bit INTE was set prior to going into Sleep. The status of Global Interrupt Enable bit, GIE, decides whether or not the processor branches to the interrupt vector following wake-up. See **Section 12.13 "Power-Down Mode** (**Sleep**)" for details on Sleep mode.

12.10.2 TMR0 INTERRUPT

An overflow (FFh \rightarrow 00h) in the TMR0 register will set flag bit, TMR0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit, TMR0IE (INTCON<5>) (see **Section 6.0 "Timer0 Module"**).

12.10.3 PORTB INTCON CHANGE

An input change on PORTB<7:4> sets flag bit, RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit, RBIE (INTCON<3>). See Section 3.2 "EECON1 and EECON2 Registers".

12.11 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (i.e., W, Status registers). This will have to be implemented in software as shown in Example 12-1.

For PIC16F818 devices, the upper 64 bytes of each bank are common. Temporary holding registers, W_TEMP and STATUS_TEMP, should be placed here. These 64 locations do not require banking and therefore, make it easier for context save and restore.

For PIC16F819 devices, the upper 16 bytes of each bank are common.

EXAMPLE 12-1: SAVING STATUS AND W REGISTERS IN RAM

MOVWF	W_TEMP	;Copy W to TEMP register
SWAPF	STATUS, W	;Swap status to be saved into W
CLRF	STATUS	;bank 0, regardless of current bank, Clears IRP,RP1,RP0
MOVWF	STATUS_TEMP	;Save status to bank zero STATUS_TEMP register
:		
:(ISR)		;Insert user code here
:		
SWAPF	STATUS_TEMP, W	;Swap STATUS_TEMP register into W
		;(sets bank to original state)
MOVWF	STATUS	;Move W into STATUS register
SWAPF	W_TEMP, F	;Swap W_TEMP
SWAPF	W_TEMP, W	;Swap W_TEMP into W

12.13 Power-Down Mode (Sleep)

Power-Down mode is entered by executing a $\ensuremath{\mathtt{SLEEP}}$ instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the \overline{PD} bit (Status<3>) is cleared, the \overline{TO} (Status<4>) bit is set and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, low or high-impedance).

For lowest current consumption in this mode, place all I/O pins at either VDD or VSS, ensure no external circuitry is drawing current from the I/O pin, power-down the A/D and disable external clocks. Pull all I/O pins that are high-impedance inputs, high or low externally, to avoid switching currents caused by floating inputs. The TOCKI input should also be at VDD or VSS for lowest current consumption. The contribution from on-chip pull-ups on PORTB should also be considered.

The MCLR pin must be at a logic high level (VIHMC).

12.13.1 WAKE-UP FROM SLEEP

The device can wake-up from Sleep through one of the following events:

- 1. External Reset input on $\overline{\text{MCLR}}$ pin.
- 2. Watchdog Timer wake-up (if WDT was enabled).
- 3. Interrupt from INT pin, RB port change or a peripheral interrupt.

External MCLR Reset will cause a device Reset. All other events are considered a continuation of program execution and cause a "wake-up". The TO and PD bits in the Status register can be used to determine the cause of the device Reset. The PD bit, which is set on power-up, is cleared when Sleep is invoked. The TO bit is cleared if a WDT time-out occurred and caused wake-up.

The following peripheral interrupts can wake the device from Sleep:

- 1. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
- 2. CCP Capture mode interrupt.
- 3. Special event trigger (Timer1 in Asynchronous mode using an external clock).
- 4. SSP (Start/Stop) bit detect interrupt.
- 5. SSP transmit or receive in Slave mode (SPI/I²C).
- 6. A/D conversion (when A/D clock source is RC).
- 7. EEPROM write operation completion.

Other peripherals cannot generate interrupts since during Sleep, no on-chip clocks are present.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is prefetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up occurs regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

12.13.2 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs before the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT postscaler will not be cleared, the TO bit will not be set and PD bit will not be cleared.
- If the interrupt occurs during or after the execution of a SLEEP instruction, the device will immediately wake-up from Sleep. The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT postscaler will be cleared, the TO bit will be set and the PD bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the PD bit. If the PD bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction.

15.2 DC Characteristics: Power-Down and Supply Current PIC16F818/819 (Industrial, Extended) PIC16LF818/819 (Industrial)

PIC16LF (Indus	Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial								
PIC16F8 [,] (Indus	Standa Operati	itandard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended							
Param No.	Тур	Max	Units		Condi	tions			
	Power-Down Current (IPD)	(1)							
	PIC16LF818/819	0.1	0.4	μΑ	-40°C				
		0.1	0.4	μΑ	+25°C	VDD = 2.0V			
		0.4	1.5	μΑ	+85°C				
	PIC16LF818/819	0.3	0.5	μA	-40°C				
		0.3	0.5	μΑ	+25°C	VDD = 3.0V			
		0.7	1.7	μΑ	+85°C				
	All devices	0.6	1.0	μΑ	-40°C				
		0.6	1.0	μA	+25°C				
		1.2	5.0	μA	+85°C	VDD = 5.0V			
	Extended devices	devices 6.0 28 μA +12		+125°C					

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSs and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

- OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
- MCLR = VDD; WDT enabled/disabled as specified.
- **3:** For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.

15.4 DC Characteristics: PIC16F818/819 (Industrial, Extended) PIC16LF818/819 (Industrial) (Continued)

DC CHA	ARACTI	ERISTICS	$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions		
	Vol	Output Low Voltage							
D080		I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +125°C		
D083		OSC2/CLKO (RC oscillator config)	—	-	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +125°C		
	Vон	Output High Voltage							
D090		I/O ports (Note 3)	Vdd - 0.7	-	—	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +125°C		
D092		OSC2/CLKO (RC oscillator config)	Vdd - 0.7	-	—	V	IOH = -1.3 mA, VDD = 4.5V, -40°С to +125°С		
		Capacitive Loading Specs on	Output Pins						
D100	COSC2	OSC2 pin	—	-	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1		
D101	Сю	All I/O pins and OSC2 (in RC mode)	—	-	50	pF			
D102	Св	SCL, SDA in I ² C™ mode	—	—	400	pF			
		Data EEPROM Memory							
D120	ED	Endurance	100K	1M	_	E/W	-40°C to +85°C		
			10K	100K	_	E/W	+85°C to +125°C		
D121	Vdrw	VDD for read/write	Vmin	-	5.5	V	Using EECON to read/write, VMIN = min. operating voltage		
D122	TDEW	Erase/write cycle time		4	8	ms			
		Program Flash Memory							
D130	Ер	Endurance	10K	100K	—	E/W	-40°C to +85°C		
			1K	10K	—	E/W	+85°C to +125°C		
D131	Vpr	VDD for read	Vmin	—	5.5	V			
D132A		VDD for erase/write	VMIN	-	5.5	V	Using EECON to read/write, VMIN = min. operating voltage		
D133	TPE	Erase cycle time	—	2	4	ms			
D134	TPW	Write cycle time	—	2	4	ms			

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PIC16F818/819 be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.



TABLE 15-1: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
	Fosc	External CLKI Frequency (Note 1)	DC	_	1	MHz	XT and RC Oscillator mode
			DC	—	20	MHz	HS Oscillator mode
				—	32	kHz	LP Oscillator mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC Oscillator mode
			0.1	—	4	MHz	XT Oscillator mode
			4	—	20	MHz	HS Oscillator mode
			5	_	200	kHz	LP Oscillator mode
1	Tosc	External CLKI Period (Note 1)	1000	—		ns	XT and RC Oscillator mode
			50	—		ns	HS Oscillator mode
			5	_		ms	LP Oscillator mode
		Oscillator Period (Note 1)	250	—	_	ns	RC Oscillator mode
			250	—	10,000	ns	XT Oscillator mode
			50	—	250	ns	HS Oscillator mode
			5	—	—	ms	LP Oscillator mode
2	Тсү	Instruction Cycle Time (Note 1)	200	TCY	DC	ns	TCY = 4/FOSC
3	TosL,	External Clock in (OSC1) High	500	_	_	ns	XT Oscillator
	TosH	or Low Time	2.5	—	—	ms	LP Oscillator
			15	—	—	ns	HS Oscillator
4	TosR,	External Clock in (OSC1) Rise or		_	25	ns	XT Oscillator
	TosF	Fall Time	—	—	50	ns	LP Oscillator
			—		15	ns	HS Oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type, under standard operating conditions, with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin. When an external clock input is used, the "max." cycle time limit is "DC" (no clock) for all devices.

FIGURE 15-8: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS



Param No.	Symbol		Characteristic	Min	Тур†	Max	Units	Conditions		
40*	T⊤0H	T0CKI High Pulse	e Width	No Prescaler	0.5 Tcy + 20	_	_	ns	Must also meet	
		V		With Prescaler	10	_	_	ns	parameter 42	
41*	T⊤0L	T0CKI Low Pulse	Width	No Prescaler	0.5 Tcy + 20		_	ns	Must also meet	
				With Prescaler	10		_	ns	parameter 42	
42*	T⊤0P	T0CKI Period		No Prescaler	Tcy + 40		_	ns		
				With Prescaler	Greater of: 20 or <u>Tcy + 40</u> N	_	_	ns	N = prescale value (2, 4,, 256)	
45*	T⊤1H	T1CKI High	Synchronous, Pre	scaler = 1	0.5 Tcy + 20	-	_	ns	Must also meet	
		Time	Synchronous,	PIC16 F 818/819	15	_	_	ns	parameter 47	
			Prescaler = 2,4,8	PIC16LF818/819	25	_	_	ns		
			Asynchronous	PIC16 F 818/819	30	-	_	ns		
				PIC16LF818/819	50	_	_	ns		
46*	T⊤1L	T1CKI Low Time	Synchronous, Pre	0.5 Tcy + 20		_	ns	Must also meet		
			Synchronous, Prescaler = 2,4,8	PIC16 F 818/819	15	—	_	ns	parameter 47	
				PIC16LF818/819	25	_	_	ns		
			Asynchronous	PIC16 F 818/819	30	_	_	ns		
				PIC16LF818/819	50	-	_	ns		
47*	TT1P	T1CKI Input Period	Synchronous	PIC16 F 818/819	Greater of: 30 or <u>Tcy + 40</u> N	_	_	ns	N = prescale value (1, 2, 4, 8)	
				PIC16 LF 818/819	Greater of: 50 or <u>Tcy + 40</u> N				N = prescale value (1, 2, 4, 8)	
			Asynchronous	PIC16 F 818/819	60		_	ns		
				PIC16LF818/819	100		_	ns		
	FT1	Timer1 Oscillator (Oscillator enable	Input Frequency R d by setting bit T10	nput Frequency Range d by setting bit T1OSCEN)			32.768	kHz		
48	TCKEZTMR1	Delay from Extern	nal Clock Edge to T	imer Increment	2 Tosc	—	7 Tosc	—		

TABLE 15-4:	TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.











FIGURE 16-21: MINIMUM AND MAXIMUM VIN vs. VDD (TTL INPUT, -40°C TO +125°C)







17.0 **PACKAGING INFORMATION**

17.1 **Package Marking Information**

18-Lead PDIP (300 mil)



18-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES			
Dimensio	n Limits	MIN	NOM	MAX	
Number of Pins	Ν		18		
Pitch	е	.100 BSC			
Top to Seating Plane	Α	-	-	.210	
Molded Package Thickness	A2	.115	.130	.195	
Base to Seating Plane	A1	.015	-	-	
Shoulder to Shoulder Width	E	.300	.310	.325	
Molded Package Width	E1	.240	.250	.280	
Overall Length	D	.880	.900	.920	
Tip to Seating Plane	L	.115	.130	.150	
Lead Thickness	С	.008	.010	.014	
Upper Lead Width	b1	.045	.060	.070	
Lower Lead Width	b	.014	.018	.022	
Overall Row Spacing §	eB	-	-	.430	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic.

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-007B

18-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Microchip Technology Drawing C04-051C Sheet 1 of 2

18-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	С		9.40	
Contact Pad Width	Х			0.60
Contact Pad Length	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2051A

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	С		7.20	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072A