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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	10MHz
Connectivity	I ² C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf818-i-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

PIC16F818/819

Pin Name	PDIP/	SSOP	QFN	I/O/P	Buffer	Description
	Pin#	Pin#	Pin#	Туре	Туре	Description
						PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT RB0 INT	6	7	7	I/O I	TTL ST ⁽¹⁾	Bidirectional I/O pin. External interrupt pin.
RB1/SDI/SDA RB1 SDI SDA	7	8	8	I/O I I/O	TTL ST ST	Bidirectional I/O pin. SPI data in. I ² C™ data.
RB2/SDO/CCP1 RB2 SDO CCP1	8	9	9	I/O O I/O	TTL ST ST	Bidirectional I/O pin. SPI data out. Capture input, Compare output, PWM output.
RB3/CCP1/PGM RB3 CCP1 PGM	9	10	10	I/O I/O I	TTL ST ST	Bidirectional I/O pin. Capture input, Compare output, PWM output. Low-Voltage ICSP™ Programming enable pin.
RB4/SCK/SCL RB4 SCK SCL	10	11	12	I/O I/O I	TTL ST ST	Bidirectional I/O pin. Interrupt-on-change pin. Synchronous serial clock input/output for SPI. Synchronous serial clock input for I ² C.
RB5/SS RB5 SS	11	12	13	I/O I	TTL TTL	Bidirectional I/O pin. Interrupt-on-change pin. Slave select for SPI in Slave mode.
RB6/T1OSO/T1CKI/PGC RB6 T1OSO T1CKI PGC	12	13	15	I/O O I I	TTL ST ST ST ⁽²⁾	Interrupt-on-change pin. Timer1 Oscillator output. Timer1 clock input. In-circuit debugger and ICSP programming clock pin.
RB7/T1OSI/PGD RB7 T1OSI PGD	13	14	16	I/O I I	TTL ST ST ⁽²⁾	Interrupt-on-change pin. Timer1 oscillator input. In-circuit debugger and ICSP programming data pin.
Vss	5	5, 6	3, 5	Р	-	Ground reference for logic and I/O pins.
VDD	14	15, 16	17, 19	Р	_	Positive supply for logic and I/O pins.
Legend:IIInputO= OutputI/OInput/OutputPPowerNot usedTTL = TTL InputST = Schmitt Trigger Input						 Input/Output P = Power Schmitt Trigger Input

TABLE 1-2: PIC16F818/819 PINOUT DESCRIPTIONS (CONTINUED)

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

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FIGURE 2-3:
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PIC16F818 REGISTER FILE MAP

A	File ddress		File Address		File Address	۵	File ddre
Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180
TMR0	01h	OPTION REG	81h	TMR0	101h	OPTION REG	181
PCL	02h	PCI	82h	PCL	102h	PCL	182
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183
FSR	04h	FSR	84h	FSR	104h	FSR	184
PORTA	05h	TRISA	85h		105h		185
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186
	07h	ITTIOD	87h		107h		187
	08h		88h		108h		188
	09h		89h		109h		189
PCLATH	0Ah	PCI ATH	8Ah	PCLATH	10Ah	PCI ATH	184
INTCON	0Bh		8Bh	INTCON	10Bh		18F
PIR1	0Ch	PIF1	8Ch	FEDATA	10Ch	EFCON1	180
PIR2	0Dh	PIE2	8Dh	FEADR	10Dh	EECON2	180
TMR1I	0Eh	PCON	8Eh		10Eh	Reserved ⁽¹⁾	185
	0Eh	OSCCON	0EH		10Eh	Reserved(1)	100
	10h		00h		110h	Reserveu	100
	1011 11h	OSCIONE	9011 01h				190
	12h	DD2	9111 02h				
	1211 13h		9211 02h				
SSPCON	1/h		9311 04b				
	1 4 11 15h	55P5TAT	9411 05b				
	16h		9511 06b				
	17h		9011 07h				
CONTOON	18h		9711 09h				
	1011 10h		9011 00h				
	1Δh		9911 04b				
	1Rh		9AN 0Ph				
	1011 101		9011 00h				
	1011 1Dh		901 006				
	1011 1Eb		9DN				
ADCONO	1Eh		905h		11Fh		19F
ADCONU	20h	ADCON1	9711		120h		140
	2011	Purpose Register	A0h		12011		.7 (
General		32 Bytes	BFh				
Purpose			C0h	Accesses		Accesses	
Register		Accesses		20h-7Fh		20h-7Fh	
96 Bytes		40h-7Fh					
	7Fh		FFh		17Fh		1FF
Bank 0		Bank 1		Bank 2		Bank 3	
Unimple * Not a ph lote 1: These re	mented d nysical reg egisters a	ata memory locati jister. re reserved; maint	ons, read ain these	as '0'. registers clear.			

4.5.3 OSCILLATOR CONTROL REGISTER

The OSCCON register (Register 4-2) controls several aspects of the system clock's operation.

The Internal Oscillator Select bits, IRCF2:IRCF0, select the frequency output of the internal oscillator block that is used to drive the system clock. The choices are the INTRC source (31.25 kHz), the INTOSC source (8 MHz) or one of the six frequencies derived from the INTOSC postscaler (125 kHz to 4 MHz). Changing the configuration of these bits has an immediate change on the multiplexor's frequency output.

4.5.4 MODIFYING THE IRCF BITS

The IRCF bits can be modified at any time regardless of which clock source is currently being used as the system clock. The internal oscillator allows users to change the frequency during run time. This is achieved by modifying the IRCF bits in the OSCCON register. The sequence of events that occur after the IRCF bits are modified is dependent upon the initial value of the IRCF bits before they are modified. If the INTRC (31.25 kHz, IRCF<2:0> = 000) is running and the IRCF bits are modified to any other value than '000', a 4 ms (approx.) clock switch delay is turned on. Code execution continues at a higher than expected frequency while the new frequency stabilizes. Time sensitive code should wait for the IOFS bit in the OSCCON register to become set before continuing. This bit can be monitored to ensure that the frequency is stable before using the system clock in time critical applications.

If the IRCF bits are modified while the internal oscillator is running at any other frequency than INTRC (31.25 kHz, IRCF<2:0> \neq 000), there is no need for a 4 ms (approx.) clock switch delay. The new INTOSC frequency will be stable immediately after the **eight** falling edges. The IOFS bit will remain set after clock switching occurs.

Note: Caution must be taken when modifying the IRCF bits using BCF or BSF instructions. It is possible to modify the IRCF bits to a frequency that may be out of the VDD specification range; for example, VDD = 2.0V and IRCF = 111 (8 MHz).

4.5.5 CLOCK TRANSITION SEQUENCE WHEN THE IRCF BITS ARE MODIFIED

Following are three different sequences for switching the internal RC oscillator frequency.

- Clock before switch: 31.25 kHz (IRCF<2:0> = 000)
 - 1. IRCF bits are modified to an INTOSC/INTOSC postscaler frequency.
 - 2. The clock switching circuitry waits for a falling edge of the current clock, at which point CLKO is held low.
 - 3. The clock switching circuitry then waits for eight falling edges of requested clock, after which it switches CLKO to this new clock source.
 - The IOFS bit is clear to indicate that the clock is unstable and a 4 ms (approx.) delay is started. Time dependent code should wait for IOFS to become set.
 - 5. Switchover is complete.
- Clock before switch: One of INTOSC/INTOSC postscaler (IRCF<2:0> ≠ 000)
 - 1. IRCF bits are modified to INTRC (IRCF<2:0> = 000).
 - 2. The clock switching circuitry waits for a falling edge of the current clock, at which point CLKO is held low.
 - 3. The clock switching circuitry then waits for eight falling edges of requested clock, after which it switches CLKO to this new clock source.
 - 4. Oscillator switchover is complete.
- Clock before switch: One of INTOSC/INTOSC postscaler (IRCF<2:0> ≠ 000)
 - 1. IRCF bits are modified to a different INTOSC/ INTOSC postscaler frequency.
 - 2. The clock switching circuitry waits for a falling edge of the current clock, at which point CLKO is held low.
 - 3. The clock switching circuitry then waits for eight falling edges of requested clock, after which it switches CLKO to this new clock source.
 - 4. The IOFS bit is set.
 - 5. Oscillator switchover is complete.

TABLE 5-3:	PORTB FUNCTIONS
TABLE 5-3:	PURID FUNCTIONS

Name	Bit#	Buffer	Function
RB0/INT	bit 0	TTL/ST ⁽¹⁾	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1/SDI/SDA	bit 1	TTL/ST ⁽⁵⁾	Input/output pin, SPI data input pin or I ² C™ data I/O pin. Internal software programmable weak pull-up.
RB2/SDO/CCP1	bit 2	TTL/ST ⁽⁴⁾	Input/output pin, SPI data output pin or Capture input/Compare output/PWM output pin. Internal software programmable weak pull-up.
RB3/CCP1/PGM ⁽³⁾	bit 3	TTL/ST ⁽²⁾	Input/output pin, Capture input/Compare output/PWM output pin or programming in LVP mode. Internal software programmable weak pull-up.
RB4/SCK/SCL	bit 4	TTL/ST ⁽⁵⁾	Input/output pin or SPI and I ² C clock pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB5/SS	bit 5	TTL	Input/output pin or SPI slave select pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB6/T1OSO/T1CKI/ PGC	bit 6	TTL/ST ⁽²⁾	Input/output pin, Timer1 oscillator output pin, Timer1 clock input pin or serial programming clock (with interrupt-on-change). Internal software programmable weak pull-up.
RB7/T1OSI/PGD	bit 7	TTL/ST ⁽²⁾	Input/output pin, Timer1 oscillator input pin or serial programming data (with interrupt-on-change). Internal software programmable weak pull-up.

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

3: Low-Voltage ICSP[™] Programming (LVP) is enabled by default which disables the RB3 I/O function. LVP must be disabled to enable RB3 as an I/O pin and allow maximum compatibility to the other 18-pin mid-range devices.

- 4: This buffer is a Schmitt Trigger input when configured for CCP or SSP mode.
- **5:** This buffer is a Schmitt Trigger input when configured for SPI or I²C mode.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
06h, 106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
86h, 186h	TRISB	PORTB	ORTB Data Direction Register					1111 1111	1111 1111		
81h, 181h	OPTION_REG	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.





7.0 TIMER1 MODULE

The Timer1 module is a 16-bit timer/counter consisting of two 8-bit registers (TMR1H and TMR1L) which are readable and writable. The TMR1 register pair (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The TMR1 interrupt, if enabled, is generated on overflow which is latched in interrupt flag bit, TMR1IF (PIR1<0>). This interrupt can be enabled/disabled by setting/clearing TMR1 Interrupt Enable bit, TMR1IE (PIE1<0>).

Timer1 can also be used to provide Real-Time Clock (RTC) functionality to applications with only a minimal addition of external components and code overhead.

7.1 Timer1 Operation

Timer1 can operate in one of three modes:

- as a timer
- as a synchronous counter
- · as an asynchronous counter

The operating mode is determined by the clock select bit, TMR1CS (T1CON<1>).

In Timer mode, Timer1 increments every instruction cycle. In Counter mode, it increments on every rising edge of the external clock input.

Timer1 can be enabled/disabled by setting/clearing control bit, TMR1ON (T1CON<0>).

Timer1 also has an internal "Reset input". This Reset can be generated by the CCP1 module as the special event trigger (see **Section 9.1** "**Capture Mode**"). Register 7-1 shows the Timer1 Control register.

When the Timer1 oscillator is enabled (T1OSCEN is set), the RB6/T1OSO/T1CKI/PGC and RB7/T1OSI/ PGD pins become inputs. That is, the TRISB<7:6> value is ignored and these pins read as '0'.

Additional information on timer modules is available in the "*PIC*[®] *Mid-Range MCU Family Reference Manual*" (DS33023).

REGISTER 7-1: T1CON: TIMER1 CONTROL REGISTER (ADDRESS 10h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_		T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N
bit 7							bit 0

bit 7-6	Unimplemented: Read	as '0'								
bit 5-4	T1CKPS1:T1CKPS0: Ti	T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits								
	11 = 1:8 Prescale value									
	10 = 1:4 Prescale value									
	01 = 1:2 Prescale value									
L H 0		llatar Enchla Control hit								
DILS		INALOF ENABLE CONTROL DIL								
	1 = Oscillator is enabled 0 = Oscillator is shut-off	(the oscillator inverter is	s turned off to eliminate power drain)							
hit 2	TISYNC: Timer1 Extern	al Clock Input Synchror	nization Control bit							
	TMR1CS = 1°									
	1 = Do not synchronize external clock input									
	0 = Synchronize externa	I clock input								
	<u>TMR1CS = 0:</u>									
	This bit is ignored. Time	r1 uses the internal cloc	k when TMR1CS = 0.							
bit 1	TMR1CS: Timer1 Clock	Source Select bit								
	1 = External clock from 0 = Internal clock (Eosc	pin RB6/T1OSO/T1CKI	/PGC (on the rising edge)							
bit 0	TMR10N: Timer1 On bit	t i								
	1 = Enables Timer1									
	0 = Stops Timer1									
	Legend:									
	R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'							

R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

7.5 Timer1 Operation in Asynchronous Counter Mode

If control bit, $\overline{\text{T1SYNC}}$ (T1CON<2>), is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during Sleep and can generate an interrupt on overflow that will wake-up the processor. However, special precautions in software are needed to read/write the timer.

In Asynchronous Counter mode, Timer1 cannot be used as a time base for capture or compare operations.

7.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers while the register is incrementing. This may produce an unpredictable value in the timer register.

Reading the 16-bit value requires some care. The example codes provided in Example 7-1 and Example 7-2 demonstrate how to write to and read Timer1 while it is running in Asynchronous mode.

FXAMPI F 7-1 .	WRITING & 16-BIT FREE BUINN	ING TIMER
EARIVIFLE (-I.	WATTING A TO-DIT FREE AUNIN	

EXAMPLE 7-2: READING A 16-BIT FREE RUNNING TIMER

; All interrupts are	disabled
MOVF TMR1H, W	; Read high byte
MOVWF TMPH	
MOVF TMR1L, W	; Read low byte
MOVWF TMPL	
MOVF TMR1H, W	; Read high byte
SUBWF TMPH, W	; Sub 1st read with 2nd read
BTFSC STATUS, Z	; Is result = 0
GOTO CONTINUE	; Good 16-bit read
; TMR1L may have rol	led over between the read of the high and low bytes.
; Reading the high a	nd low bytes now will read a good value.
MOVF TMR1H, W	; Read high byte
MOVWF TMPH	
MOVF TMR1L, W	; Read low byte
MOVWF TMPL	; Re-enable the Interrupt (if required)
CONTINUE	; Continue with your code

7.6 Timer1 Oscillator

A crystal oscillator circuit is built-in between pins T1OSI (input) and T1OSO (amplifier output). It is enabled by setting control bit, T1OSCEN (T1CON<3>). The oscillator is a low-power oscillator, rated up to 32.768 kHz. It will continue to run during Sleep. It is primarily intended for a 32 kHz crystal. The circuit for a typical LP oscillator is shown in Figure 7-3. Table 7-1 shows the capacitor selection for the Timer1 oscillator.

The user must provide a software time delay to ensure proper oscillator start-up.

Note: The Timer1 oscillator shares the T1OSI and T1OSO pins with the PGD and PGC pins used for programming and debugging.

When using the Timer1 oscillator, In-Circuit Serial Programming[™] (ICSP[™]) may not function correctly (high-voltage or lowvoltage) or the In-Circuit Debugger (ICD) may not communicate with the controller. As a result of using either ICSP or ICD, the Timer1 crystal may be damaged.

If ICSP or ICD operations are required, the crystal should be disconnected from the circuit (disconnect either lead) or installed after programming. The oscillator loading capacitors may remain in-circuit during ICSP or ICD operation.

FIGURE 7-3: EXTERNAL COMPONENTS FOR THE TIMER1 LP OSCILLATOR



TABLE 7-1:CAPACITOR SELECTION FOR
THE TIMER1 OSCILLATOR

Osc Type	Freq	C1	C2		
LP	LP 32 kHz		33 pF		

- **Note 1:** Microchip suggests this value as a starting point in validating the oscillator circuit.
 - 2: Higher capacitance increases the stability of the oscillator but also increases the start-up time.
 - 3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
 - 4: Capacitor values are for design guidance only.

7.7 Timer1 Oscillator Layout Considerations

The Timer1 oscillator circuit draws very little power during operation. Due to the low-power nature of the oscillator, it may also be sensitive to rapidly changing signals in close proximity.

The oscillator circuit, shown in Figure 7-3, should be located as close as possible to the microcontroller. There should be no circuits passing within the oscillator circuit boundaries other than VSS or VDD.

If a high-speed circuit must be located near the oscillator, a grounded guard ring around the oscillator circuit, as shown in Figure 7-4, may be helpful when used on a single-sided PCB or in addition to a ground plane.



EXAMPLE 7-3:	IMPLEMENTING A REAL-TIME CLOCK USING A TIMER1 INTERRUPT SERVICE
-	

RTCinit	BANKSEL	TMR1H		
	MOVLW	0x80	;	Preload TMR1 register pair
	MOVWF	TMR1H	;	for 1 second overflow
	CLRF	TMR1L		
	MOVLW	b'00001111'	;	Configure for external clock,
	MOVWF	T1CON	;	Asynchronous operation, external oscillator
	CLRF	secs	;	Initialize timekeeping registers
	CLRF	mins		
	MOVLW	.12		
	MOVWF	hours		
	BANKSEL	PIE1		
	BSF	PIE1, TMR1IE	;	Enable Timer1 interrupt
	RETURN			
RTCisr	BANKSEL	TMR1H		
	BSF	TMR1H, 7	;	Preload for 1 sec overflow
	BCF	PIR1, TMR1IF	;	Clear interrupt flag
	INCF	secs, F	;	Increment seconds
	MOVF	secs, w		
	SUBLW	.60		
	BTFSS	STATUS, Z	;	60 seconds elapsed?
	RETURN	_	;	No, done
	CLRF	seconds	;	Clear seconds
	INCF	mins, f	;	Increment minutes
	MOVF	mins, w		
	SUBLW	.60		
	BTFSS	STATUS, Z	;	60 seconds elapsed?
	RETURN		;	No, done
	CLRF	mins	;	Clear minutes
	INCF	hours, f	;	Increment hours
	MOVE	hours, w		
	SUBLW	.24		
	BIFSS	STATUS, Z	;	24 nours elapsed?
	RETURN	h	;	No, done
	CLKF	nours	;	Clear nours
	RETURN		;	Doue

TABLE 7-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Valu POR,	e on BOR	Valu all c Res	e on other sets
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000	000x	0000	000u
0Ch	PIR1	_	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	- 0	0000	- 0	0000
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	- 0	0000	- 0	0000
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx	xxxx	uuuu	uuuu
0Fh	TMR1H	Holding	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register							xxxx	xxxx	uuuu	uuuu
10h	T1CON	_	_	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00	0000	uu	uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

8.0 TIMER2 MODULE

Timer2 is an 8-bit timer with a prescaler and a postscaler. It can be used as the PWM time base for the PWM mode of the CCP1 module. The TMR2 register is readable and writable and is cleared on any device Reset.

The input clock (FOSC/4) has a prescale option of 1:1, 1:4 or 1:16, selected by control bits, T2CKPS1:T2CKPS0 (T2CON<1:0>).

The Timer2 module has an 8-bit period register, PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon Reset.

The match output of TMR2 goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling inclusive) to generate a TMR2 interrupt (latched in flag bit, TMR2IF (PIR1<1>)).

Timer2 can be shut-off by clearing control bit, TMR2ON (T2CON<2>), to minimize power consumption.

Register 8-1 shows the Timer2 Control register.

Additional information on timer modules is available in the "*PIC*[®] *Mid-Range MCU Family Reference Manual*" (DS33023).

8.1 Timer2 Prescaler and Postscaler

The prescaler and postscaler counters are cleared when any of the following occurs:

- A write to the TMR2 register
- A write to the T2CON register
- Any device Reset (Power-on Reset, MCLR, WDT Reset or Brown-out Reset)

TMR2 is not cleared when T2CON is written.

8.2 Output of TMR2

The output of TMR2 (before the postscaler) is fed to the Synchronous Serial Port module which optionally uses it to generate a shift clock.

FIGURE 8-1: TIMER2 BLOCK DIAGRAM



PIC16F818/819

REGISTER 10-1:	SSPSTAT: SYNCHRONOUS SERIAL PORT STATUS REGISTER (ADDRESS 94h)									
	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0		
	SMP	CKE	D/A	Р	S	R/W	UA	BF		
	bit 7	•			•		1	bit 0		
bit 7	SMP: SPI D	Data Input S	ample Phas	e bit						
	<u>SPI Master</u>	<u>mode:</u> ta sampled	at and of da	to output tim						
	1 = Input da 0 = Input da 10 = 0	ata sampled	at middle of	^t data output	time (Micro	wire)				
	SPI Slave r	node:								
	This bit mus	st be cleared	d when SPI i	is used in Sla	ave mode.					
	<u>I²C mode:</u>									
	This bit mus	st be mainta	ined clear.							
bit 6	CKE: SPIC	lock Edge S	Select bit							
	 1 = Transmit occurs on transition from active to Idle clock state 0 = Transmit occurs on transition from Idle to active clock state 									
	Note:	Polarity of c	lock state is	set by the C	KP bit (SSF	PCON<4>).				
	I ² C mode: This bit mus	st be mainta	ined clear.							
bit 5	D/A: Data/Address bit (I ² C mode only)									
	In I ² C Slave mode:									
	1 = Indicates that the last byte received was data									
hit 4	P. Stop bit(1) (1 ² C mode	only)		1633					
Dit 4	1 = Indicat	es that a Sto	bit has be	en detected	last					
	0 = Stop bit was not detected last									
bit 3	S: Start bit ⁽¹⁾ (I ² C mode only)									
	 1 = Indicates that a Start bit has been detected last (this bit is '0' on Reset) 0 = Start bit was not detected last 									
bit 2	R/W: Read/Write Information bit (I ² C mode only)									
	Holds the R/W bit information following the last address match and is only valid from address match to the next Start bit, Stop bit or ACK bit.									
	1 = Read 0 = Write									
bit 1	UA: Update	Address bi	t (10-bit I ² C	mode only)						
	1 = Indicate 0 = Addres	es that the u is does not r	iser needs to need to be u	o update the pdated	address in t	the SSPADI	D register			
bit 0	BF: Buffer I	Full Status b	it							
	Receive (SI	PI and I ² C m	nodes):							
	1 = Receive	e complete,	SSPBUF is	full - is seenthy						
	0 = Receive	e^{12} C mode	ete, SSPBUI	- is empty						
	1 = Transmit(Ir)	it in progres	s. SSPBUF	is full (8 bits)					
	0 = Transm	it complete,	SSPBUF is	empty	,					
	Note 1:	This bit is cl	eared when	the SSP mo	dule is disab	led (i.e., the	SSPEN bit i	s cleared).		

Leg	jend:			
R =	Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
-n =	Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

11.1 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 11-2. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD), see Figure 11-2. The maximum recommended impedance for analog sources is 2.5 k\Omega. As the impedance is decreased, the acquisition time may be decreased.

After the analog input channel is selected (changed), this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 11-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

To calculate the minimum acquisition time, TACQ, see the "*PIC*[®] *Mid-Range MCU Family Reference Manual*" (DS33023).

EQUATION 11-1: ACQUISITION TIME

TACQ = Amplifier Settling Time + Hold Capacitor Charging Time + Temperature Coefficient = TAMP + TC + TCOFF $= 2 \mu s + TC + [(Temperature - 25^{\circ}C)(0.05 \mu s/^{\circ}C)]$ TC = CHOLD (RIC + Rss + Rs) In(1/2047) $= -120 pF (1 k\Omega + 7 k\Omega + 10 k\Omega) In(0.0004885)$ $= 16.47 \mu s$ $TACQ = 2 \mu s + 16.47 \mu s + [(50^{\circ}C - 25^{\circ}C)(0.05 \mu s/^{\circ}C)]$ $= 19.72 \mu s$

Note 1: The reference voltage (VREF) has no effect on the equation since it cancels itself out.

- **2:** The charge holding capacitor (CHOLD) is not discharged after each conversion.
- **3:** The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.
- **4:** After a conversion has completed, a 2.0 TAD delay must complete before acquisition can begin again. During this time, the holding capacitor is not connected to the selected A/D input channel.

FIGURE 11-2: ANALOG INPUT MODEL



12.3 MCLR

PIC16F818/819 device has a noise filter in the MCLR Reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive MCLR pin low.

The behavior of the ESD protection on the MCLR pin has been altered from previous devices of this family. Voltages applied to the pin that exceed its specification can result in both MCLR and excessive current beyond the device specification during the ESD event. For this reason, Microchip recommends that the MCLR pin no longer be tied directly to VDD. The use of an RC network, as shown in Figure 12-2, is suggested.

The RA5/MCLR/VPP pin can be configured for $\overline{\text{MCLR}}$ (default) or as an I/O pin (RA5). This is configured through the MCLRE bit in the Configuration Word register.

FIGURE 12-2: RECOMMENDED MCLR CIRCUIT



12.4 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.2V-1.7V). To take advantage of the POR, tie the \underline{MCLR} pin to VDD as described in Section 12.3 "MCLR". A maximum rise time for VDD is specified. See Section 15.0 "Electrical Characteristics" for details.

When the device starts normal operation (exits the Reset condition), device operating parameters (voltage, frequency, temperature, ...) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met. For more information, see Application Note *AN607, "Power-up Trouble Shooting"* (DS00607).

12.5 Power-up Timer (PWRT)

The Power-up Timer (PWRT) of the PIC16F818/819 is a counter that uses the INTRC oscillator as the clock input. This yields a count of 72 ms. While the PWRT is counting, the device is held in Reset.

The power-up time delay depends on the INTRC and will vary from chip-to-chip due to temperature and process variation. See DC parameter #33 for details.

The PWRT is enabled by clearing configuration bit, PWRTEN.

12.6 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides 1024 oscillator cycles (from OSC1 input) delay after the PWRT delay is over (if enabled). This helps to ensure that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from Sleep.

12.7 Brown-out Reset (BOR)

The configuration bit, BOREN, can enable or disable the Brown-out Reset circuit. If VDD falls below VBOR (parameter #D005, about 4V) for longer than TBOR (parameter #35, about 100 μ s), the brown-out situation will reset the device. If VDD falls below VBOR for less than TBOR, a Reset may not occur.

Once the brown-out occurs, the device will remain in Brown-out Reset until VDD rises above VBOR. The Power-up Timer (if enabled) will keep the device in Reset for TPWRT (parameter #33, about 72 ms). If VDD should fall below VBOR during TPWRT, the Brown-out Reset process will restart when VDD rises above VBOR with the Power-up Timer Reset. Unlike previous PIC16 devices, the PWRT is no longer automatically enabled when the Brown-out Reset circuit is enabled. The PWRTEN and BOREN configuration bits are independent of each other.

12.8 Time-out Sequence

On power-up, the time-out sequence is as follows: the PWRT delay starts (if enabled) when a POR occurs. Then, OST starts counting 1024 oscillator cycles when PWRT ends (LP, XT, HS). When the OST ends, the device comes out of Reset.

If MCLR is kept low long enough, all delays will expire. Bringing MCLR high will begin execution immediately. This is useful for testing purposes or to synchronize more than one PIC16F818/819 device operating in parallel.

Table 12-3 shows the Reset conditions for the Status, PCON and PC registers, while Table 12-4 shows the Reset conditions for all the registers.













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15.1 DC Characteristics: Supply Voltage PIC16F818/819 (Industrial, Extended) PIC16LF818/819 (Industrial)

PIC16LF818/819 (Industrial)		Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial										
PIC16F818/819 (Industrial, Extended)		Standard Operating Condition				ons (unless otherwise stated) -40°C \leq TA \leq +85°C for industrial -40°C \leq TA \leq +125°C for extended						
Param No.	Symbol	Characteristic	Min	Тур	Conditions							
	Vdd	Supply Voltage	Supply Voltage									
D001		PIC16LF818/819	2.0	_	5.5	V	HS, XT, RC and LP Oscillator mode					
D001		PIC16F818/819	4.0		5.5	V						
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾	1.5	_	_	V						
D003	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal	—	—	0.7	V	See Section 12.4 "Power-on Reset (POR)" for details					
D004	Svdd	VDD Rise Rate to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See Section 12.4 "Power-on Reset (POR)" for details					
	VBOR	Brown-out Reset Voltage										
D005		PIC16LF818/819	3.65	_	4.35	V						
D005		PIC16F818/819	3.65	_	4.35	V	FMAX = 14 MHz ⁽²⁾					

Legend: Shading of rows is to assist in readability of the table.

Note 1: This is the limit to which VDD can be lowered in Sleep mode, or during a device Reset, without losing RAM data

2: When BOR is enabled, the device will operate correctly until the VBOR voltage trip point is reached.

15.5 Timing Parameter Symbology

The timing parameter symbols have been created using one of the following formats:

1. TppS2pp	S	3. Tcc:s⊤	(I ² C specifications only)
2. TppS		4. Ts	(I ² C specifications only)
Т			
F	Frequency	Т	Time
Lowercas	e letters (pp) and their meanings:		
рр			
сс	CCP1	OSC	OSC1
ck	CLKO	rd	RD
CS	CS	rw	RD or WR
di	SDI	SC	SCK
do	SDO	SS	SS
dt	Data in	tO	TOCKI
io	I/O port	t1	T1CKI
mc	MCLR	wr	WR
Uppercas	e letters and their meanings:		
S			
F	Fall	Р	Period
Н	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance
I ² C only			
AA	output access	High	High
BUF	Bus free	Low	Low
TCC:ST (I ²	C specifications only)		
CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	Stop condition
STA	Start condition		

FIGURE 15-3: LOAD CONDITIONS





TABLE 15-1: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
	Fosc	External CLKI Frequency (Note 1)	DC		1	MHz	XT and RC Oscillator mode
			DC	—	20	MHz	HS Oscillator mode
			DC	_	32	kHz	LP Oscillator mode
		Oscillator Frequency (Note 1)	DC		4	MHz	RC Oscillator mode
			0.1	—	4	MHz	XT Oscillator mode
			4	—	20	MHz	HS Oscillator mode
			5	_	200	kHz	LP Oscillator mode
1	Tosc	External CLKI Period (Note 1)	1000	—	_	ns	XT and RC Oscillator mode
			50	—	—	ns	HS Oscillator mode
			5	_		ms	LP Oscillator mode
		Oscillator Period (Note 1)	250		_	ns	RC Oscillator mode
			250	—	10,000	ns	XT Oscillator mode
			50	—	250	ns	HS Oscillator mode
			5	_	—	ms	LP Oscillator mode
2	Тсү	Instruction Cycle Time (Note 1)	200	Тсү	DC	ns	TCY = 4/FOSC
3	TosL,	External Clock in (OSC1) High	500	_	_	ns	XT Oscillator
	TosH	or Low Time	2.5	—	—	ms	LP Oscillator
			15	—	—	ns	HS Oscillator
4	TosR,	External Clock in (OSC1) Rise or	—	_	25	ns	XT Oscillator
	TosF	Fall Time	—	—	50	ns	LP Oscillator
			—	—	15	ns	HS Oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type, under standard operating conditions, with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin. When an external clock input is used, the "max." cycle time limit is "DC" (no clock) for all devices.







Param. No.	Symbol	Characte	eristic	Min	Мах	Units	Conditions
100*	Тнідн	Clock High Time	100 kHz mode	4.0	—	μs	
			400 kHz mode	0.6	—	μs	
			SSP Module	1.5 TCY	—		
101*	TLOW	Clock Low Time	100 kHz mode	4.7	—	μs	
			400 kHz mode	1.3	_	μs	
			SSP Module	1.5 TCY	_		
102*	TR	SDA and SCL Rise	100 kHz mode	—	1000	ns	
		Time	400 kHz mode	20 + 0.1 Св	300	ns	CB is specified to be from 10-400 pF
103*	TF	SDA and SCL Fall	100 kHz mode	—	300	ns	
		Time	400 kHz mode	20 + 0.1 Св	300	ns	CB is specified to be from 10-400 pF
90*	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7	—	μs	Only relevant for Repeated
			400 kHz mode	0.6	_	μs	Start condition
91*	THD:STA	Start Condition Hold	100 kHz mode	4.0	—	μs	After this period, the first
		Time	400 kHz mode	0.6	_	μS	clock pulse is generated
106*	THD:DAT	Data Input Hold	100 kHz mode	0	_	ns	
		Time	400 kHz mode	0	0.9	μS	
107*	TSU:DAT	Data Input Setup	100 kHz mode	250	_	ns	(Note 2)
		Time	400 kHz mode	100	—	ns	
92*	Tsu:sto	Stop Condition	100 kHz mode	4.7	—	μS	
		Setup Time	400 kHz mode	0.6	—	μs	
109*	ΤΑΑ	Output Valid from	100 kHz mode	—	3500	ns	(Note 1)
		Clock	400 kHz mode	—	—	ns	
110*	TBUF	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be free
			400 kHz mode	1.3		μs	before a new transmission can start
	Св	Bus Capacitive Load	ling	_	400	pF	

TABLE 15-8: I²C™ BUS DATA REQUIREMENTS

* These parameters are characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

2: A Fast mode (400 kHz) I²CTM bus device can be used in a Standard mode (100 kHz) I²C bus system but the requirement, TSU:DAT ≥ 250 ns, must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line, TR max. + TSU:DAT = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification), before the SCL line is released.

PIC16F818/819

NOTES: