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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	10MHz
Connectivity	I <sup>2</sup> C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf818-i-ptsl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

#### **Pin Diagrams**



An example of the complete four-word write sequence is shown in Example 3-5. The initial address is loaded into the EEADRH:EEADR register pair; the four words of data are loaded using indirect addressing, assuming that a row erase sequence has already been performed.

#### EXAMPLE 3-5: WRITING TO FLASH PROGRAM MEMORY

; This write routine assumes the following: ; 1. The 32 words in the erase block have already been erased. ; 2. A valid starting address (the least significant bits = '00') is loaded into EEADRH:EEADR ; 3. This example is starting at 0x100, this is an application dependent setting. ; 4. The 8 bytes (4 words) of data are loaded, starting at an address in RAM called ARRAY. ; 5. This is an example only, location of data to program is application dependent. ; 6. word\_block is located in data memory. BANKSEL EECON1 ;prepare for WRITE procedure EECON1, EEPGD BSF ; point to program memory EECON1, WREN BSF ;allow write cycles BCF EECON1, FREE ;perform write only BANKSEL word block MOVLW .4 MOVWF word block ;prepare for 4 words to be written BANKSEL EEADRH ;Start writing at 0x100 MOVLW  $0 \times 01$ MOVWF ;load HIGH address EEADRH MOVLW 0x00 MOVWF EEADR ;load LOW address BANKSEL ARRAY MOVLW ARRAY ; initialize FSR to start of data MOVWF FSR LOOP BANKSEL EEDATA MOVF INDF, W ; indirectly load EEDATA MOVWF EEDATA INCF FSR. F ; increment data pointer MOVF INDF, W ; indirectly load EEDATH MOVWF EEDATH INCE FSR, F ; increment data pointer BANKSEL EECON1 ;required sequence MOVLW 0x55 MOVWF EECON2 MOVIW 0xAA ner MOVWF EECON2 BSF EECON1, WR ;set WR bit to begin write NOP ; instructions here are ignored as processor NOP BANKSEL EEADR INCF EEADR, f ;load next word address BANKSEL word\_block DECFSZ word\_block, f ; have 4 words been written? GOTO loop ;NO, continue with writing BANKSEL EECON1 BCF EECON1, WREN ;YES, 4 words complete, disable writes BSF INTCON, GIE ;enable interrupts

#### 3.8 Protection Against Spurious Write

There are conditions when the device should not write to the data EEPROM memory. To protect against spurious EEPROM writes, various mechanisms have been built-in. On power-up, WREN is cleared. Also, the Power-up Timer (72 ms duration) prevents an EEPROM write.

The write initiate sequence and the WREN bit together help prevent an accidental write during brown-out, power glitch or software malfunction.

#### 3.9 Operation During Code-Protect

When the data EEPROM is code-protected, the microcontroller can read and write to the EEPROM normally. However, all external access to the EEPROM is disabled. External write access to the program memory is also disabled.

When program memory is code-protected, the microcontroller can read and write to program memory normally as well as execute instructions. Writes by the device may be selectively inhibited to regions of the memory depending on the setting of bits, WRT1:WRT0, of the Configuration Word (see **Section 12.1 "Configuration Bits"** for additional information). External access to the memory is also disabled.

### TABLE 3-1:REGISTERS/BITS ASSOCIATED WITH DATA EEPROM AND<br/>FLASH PROGRAM MEMORIES

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other Resets
10Ch	EEDATA	EEPRON	EEPROM/Flash Data Register Low Byte								uuuu uuuu
10Dh	EEADR	EEPRON	1/Flash A	ddress Reg	gister Lov	v Byte				xxxx xxxx	uuuu uuuu
10Eh	EEDATH	_	_	EEPROM	/Flash Da	ata Registe	r High Byte			xx xxxx	uu uuuu
10Fh	EEADRH	—	_	—	—	—	EEPROM/ Register H	'Flash Addr ligh Byte	xxx	uuu	
18Ch	EECON1	EEPGD	_	_	FREE	WRERR	WREN	WR	RD	xx x000	xx q000
18Dh	EECON2	EEPROM Control Register 2 (not a physical register)									
0Dh	PIR2		—	—	EEIF	—	—	—	—		0
8Dh	PIE2	—	—	_	EEIE	_	—	—	—		

**Legend:** x = unknown, u = unchanged, - = unimplemented, read as '0', q = value depends upon condition. Shaded cells are not used by data EEPROM or Flash program memory.

#### FIGURE 4-6: PIC16F818/819 CLOCK DIAGRAM



#### **REGISTER 4-2: OSCCON: OSCILLATOR CONTROL REGISTER (ADDRESS 8Fh)**

U-0	R/W-0	R/W-0	R/W-0	U-0	R-0	U-0	U-0
—	IRCF2	IRCF1	IRCF0	—	IOFS	_	—
bit 7							bit 0

#### bit 7 Unimplemented: Read as '0'

bit 6-4	IRCF2:IRCF0: Internal Oscillator Frequency Select bits						
	111 = 8 MHz (8 MHz source drives clock directly)						
	110 = 4 MHz						
	101 = 2 MHz						
	100 = 1 MHz						
	011 = 500 kHz						
	010 <b>= 250 kHz</b>						
	001 = 125 kHz						
	000 = 31.25 kHz (INTRC source drives clock directly)						
bit 3	Unimplemented: Read as '0'						
bit 2	IOFS: INTOSC Frequency Stable bit						
	1 = Frequency is stable						
	0 = Frequency is not stable						
bit 1-0	Unimplemented: Read as '0'						
	Legend:						

Legena:			
R = Readable bit	W = Writable bit	U = Unimplemented b	oit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown







An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF must be cleared in software and the SSPSTAT register is used to determine the status of the byte. Flag bit SSPIF is set on the falling edge of the ninth clock pulse.

As a slave-transmitter, the  $\overline{ACK}$  pulse from the masterreceiver is latched on the rising edge of the ninth SCL input pulse. If the SDA line was high (not  $\overline{ACK}$ ), then the data transfer is complete. When the  $\overline{ACK}$  is latched by the slave device, the slave logic is reset (resets SSPSTAT register) and the slave device then monitors for another occurrence of the Start bit. If the SDA line was low ( $\overline{ACK}$ ), the transmit data must be loaded into the SSPBUF register which also loads the SSPSR register. Then pin RB4/SCK/SCL should be enabled by setting bit, CKP.

TABLE 10-2: DATA TRANSFER RECEIVED BYTE ACTIONS	TABLE 10-2:	DATA TRANSFER RECEIVED BYTE ACTIONS
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Status Bits as Data Transfer is Received		$SSPSR \rightarrow SSPBUF$	Generate ACK Pulse	Set bit SSPIF		
BF	SSPOV			(SSP interrupt occurs if enabled)		
0	0	Yes	Yes	Yes		
1	0	No	No	Yes		
1	1	No	No	Yes		
0	1	No	No	Yes		

Note 1: Shaded cells show the conditions where the user software did not properly clear the overflow condition.

#### FIGURE 10-6: I<sup>2</sup>C<sup>™</sup> WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)



#### FIGURE 10-7: I<sup>2</sup>C<sup>™</sup> WAVEFORMS FOR TRANSMISSION (7-BIT ADDRESS)



#### 12.9 Power Control/Status Register (PCON)

The Power Control/Status register, PCON, has two bits to indicate the type of Reset that last occurred.

Bit 0 is Brown-out Reset Status bit,  $\overline{\text{BOR}}$ . Bit  $\overline{\text{BOR}}$  is unknown on a Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if

# bit BOR cleared, indicating a Brown-out Reset occurred. When the Brown-out Reset is disabled, the state of the BOR bit is unpredictable.

Bit 1 is Power-on Reset Status bit,  $\overline{\text{POR}}$ . It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

#### TABLE 12-1: TIME-OUT IN VARIOUS SITUATIONS

Oscillator	Power-u	p	Brown-out R	Wake-up	
Configuration	PWRTE = 0	PWRTE = 1	PWRTE = 0	PWRTE = 1	from Sleep
XT, HS, LP	TPWRT + 1024 • TOSC	1024 • Tosc	TPWRT + 1024 • TOSC	1024 • Tosc	1024 • Tosc
EXTRC, EXTCLK, INTRC	TPWRT	5-10 μs <b>(1)</b>	Tpwrt	5-10 μs <sup>(1)</sup>	5-10 μs <b>(1)</b>

**Note 1:** CPU start-up is always invoked on POR, BOR and wake-up from Sleep.

#### TABLE 12-2: STATUS BITS AND THEIR SIGNIFICANCE

POR	BOR	ТО	PD	
0	x	1	1	Power-on Reset
0	x	0	x	Illegal, $\overline{\text{TO}}$ is set on $\overline{\text{POR}}$
0	x	x	0	Illegal, PD is set on POR
1	0	1	1	Brown-out Reset
1	1	0	1	WDT Reset
1	1	0	0	WDT wake-up
1	1	u	u	MCLR Reset during normal operation
1	1	1	0	MCLR Reset during Sleep or interrupt wake-up from Sleep

**Legend:** u = unchanged, x = unknown

#### TABLE 12-3: RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	Status Register	PCON Register
Power-on Reset	000h	0001 1xxx	0x
MCLR Reset during normal operation	000h	000u uuuu	uu
MCLR Reset during Sleep	000h	0001 Ouuu	uu
WDT Reset	000h	0000 luuu	uu
WDT wake-up	PC + 1	uuu0 0uuu	uu
Brown-out Reset	000h	0001 luuu	u0
Interrupt wake-up from Sleep	PC + 1 <sup>(1)</sup>	uuul Ouuu	uu

**Legend:** u = unchanged, x = unknown, - = unimplemented bit, read as '0'

**Note 1:** When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).













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### 12.17 In-Circuit Serial Programming

PIC16F818/819 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data and three other lines for power, ground and the programming voltage (see Figure 12-10 for an example). This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

For more information on serial programming, please refer to the *"PIC16F818/819 Flash Memory Programming Specification"* (DS39603).

Note:	The Timer1 oscillator shares the T1OSI and T1OSO pins with the PGD and PGC pins used for programming and debugging.
	When using the Timer1 oscillator, In-Circuit Serial Programming <sup>™</sup> (ICSP <sup>™</sup> ) may not function correctly (high voltage or low voltage) or the In-Circuit Debugger (ICD) may not communicate with the controller. As a result of using either ICSP or ICD, the Timer1 crystal may be damaged.
	If ICSP or ICD operations are required, the crystal should be disconnected from the circuit (disconnect either lead) or installed after programming. The oscillator loading capacitors may remain in-circuit during

ICSP or ICD operation.

#### FIGURE 12-10: TYPICAL IN-CIRCUIT

#### SERIAL PROGRAMMING CONNECTION



#### 14.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC<sup>®</sup> DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

#### 14.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC<sup>®</sup> Flash MCUs and dsPIC<sup>®</sup> Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with incircuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

#### 14.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC<sup>®</sup> Flash microcontrollers and dsPIC<sup>®</sup> DSCs with the powerful, yet easyto-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

### 14.10 PICkit 3 In-Circuit Debugger/ Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC<sup>®</sup> and dsPIC<sup>®</sup> Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming<sup>™</sup>.

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

### 15.2 DC Characteristics: Power-Down and Supply Current PIC16F818/819 (Industrial, Extended) PIC16LF818/819 (Industrial) (Continued)

PIC16LF8 (Indus	Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial								
PIC16F818/819 (Industrial, Extended)		<b>Standa</b> Operati	Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended						
Param Device		Тур	Max	Units	Conditions				
Supply Current (IDD) <sup>(2,3)</sup>									
	PIC16LF818/819	9	20	μΑ	-40°C	Vdd = 2.0V			
		7	15	μΑ	+25°C				
		7	15	μA	+85°C				
	PIC16LF818/819	16	30	μA	-40°C				
		14	25	μA	+25°C	VDD = 3.0V	Fosc = 32 kHz		
		14	25	μA	+85°C		(LP Oscillator)		
	All devices	32	40	μA	-40°C				
		26	35	μA	+25°C				
		26	35	μΑ	+85°C	VDD = 5.0V			
	Extended devices	35	53	μA	+125°C				

**Legend:** Shading of rows is to assist in readability of the table.

**Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;

MCLR = VDD; WDT enabled/disabled as specified.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.

### 15.2 DC Characteristics: Power-Down and Supply Current PIC16F818/819 (Industrial, Extended) PIC16LF818/819 (Industrial) (Continued)

PIC16LF818/819 (Industrial)		Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial									
PIC16F81 (Indus	$\begin{array}{llllllllllllllllllllllllllllllllllll$										
Param No.	Device	Тур	Max	Units		Conditions					
	Supply Current (IDD) <sup>(2,3)</sup>										
	All devices	1.8	2.3	mA	-40°C		Fosc = 20 MHz (HS Oscillator)				
		1.6	2.2	mA	+25°C	VDD = 4.0V					
		1.3	2.2	mA	+85°C						
	All devices	3.0	4.2	mA	-40°C						
		2.5	4.0	mA	+25°C						
		2.5	4.0	mA	+85°C	vuu ≅ 5.0v					
	Extended devices	3.0	5.0	mA	+125°C						

Legend: Shading of rows is to assist in readability of the table.

**Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

 $\frac{OSC1}{MCLR}$  = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;  $\frac{MCLR}{MCLR}$  = VDD; WDT enabled/disabled as specified.

**3:** For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.

#### 15.3 DC Characteristics: Internal RC Accuracy PIC16F818/819, PIC16F818/819 TSL (Industrial, Extended) PIC16LF818/819, PIC16LF818/819 TSL (Industrial)

PIC16LF818/819 <sup>(3)</sup> PIC16LF818/819 TSL <sup>(3)</sup> (Industrial)		Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial								
PIC16F818/819 <sup>(3)</sup> PIC16F818/819 TSL <sup>(3)</sup> (Industrial, Extended)		$\begin{array}{llllllllllllllllllllllllllllllllllll$								
Param No.	Device	Min	Тур	Max	Units	Conditions				
	INTOSC Accuracy @ Freq = 8 MHz, 4 MHz, 2 MHz, 1 MHz, 500 kHz, 250 kHz, 125 kHz <sup>(1)</sup>									
	PIC16LF818/819	-5	±1	5	%	+25°C				
		-25	_	25	%	-10°C to +85°C	VDD = 2.7-3.3V			
		-30	_	30	%	-40°C to +85°C				
	PIC16F818/819 <sup>(4)</sup>	-5	±1	5	%	+25°C				
		-25	_	25	%	-10°C to +85°C	Vpp – 4 5-5 5V			
		-30	_	30	%	-40°C to +85°C	100 - 4.0 0.01			
		-35	_	35	%	-40°C to +125°C				
	PIC16LF818/819 TSL	-2	±1	2	%	+25°C				
		-5	_	5	%	-10°C to +85°C	VDD = 2.7-3.3V			
		-10	_	10	%	-40°C to +85°C				
	PIC16F818/819 TSL <sup>(5)</sup>	-2	±1	2	%	+25°C				
		-5	_	5	%	-10°C to +85°C	Vpp – 4 5-5 5V			
		-10	—	10	%	-40°C to +85°C	100 - 4.0 0.01			
		-15	—	15	%	-40°C to +125°C				
	INTRC Accuracy @ Freq = 31 kHz <sup>(2)</sup>									
	PIC16LF818/819	26.562		35.938	kHz	-40°C to +85°C	VDD = 2.7-3.3V			
	PIC16F818/819 <sup>(4)</sup>	26.562	—	35.938	kHz	-40°C to +85°C	VDD = 4.5-5.5V			
	PIC16LF818/819 TSL	26.562	_	35.938	kHz	-40°C to +85°C	VDD = 2.7-3.3V			
	PIC16F818/819 TSL <sup>(5)</sup>	26.562	—	35.938	kHz	-40°C to +85°C	VDD = 4.5-5.5V			

**Legend:** Shading of rows is to assist in readability of the table.

Note 1: Frequency calibrated at 25°C. OSCTUNE register can be used to compensate for temperature drift.

**2:** INTRC frequency after calibration.

3: The only specification difference between a non-TSL device and a TSL device is the internal RC oscillator specifications listed above. All other specifications are maintained.

4: Example part number for the specifications listed above: PIC16F818-I/SS (PIC16F818 device, Industrial temperature, SSOP package).

5: Example part number for the specifications listed above: PIC16F818-I/SSTSL (PIC16F818 device, Industrial temperature, SSOP package).





Param No.	Symbol	Characte	Min	Тур†	Max	Units	Conditions	
130 TAD A/D Clock Period		A/D Clock Period	PIC16F818/819	1.6	—	_	μS	Tosc based, VREF $\ge 3.0V$
			PIC16LF818/819	3.0	_	—	μs	Tosc based, VREF $\ge 2.0V$
			PIC16F818/819	2.0	4.0	6.0	μs	A/D RC mode
			PIC16LF818/819	3.0	6.0	9.0	μs	A/D RC mode
131	TCNV	Conversion Time (not i (Note 1)		—	12	Tad		
132	TACQ Acquisition Time		(Note 2)	40	—	μS		
				10*	_	_	μs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1 LSb (i.e., 5.0 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD).
134	TGO	Q4 to A/D Clock Start		_	Tosc/2 §	_	—	If the A/D clock source is selected as RC, a time of Tcy is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

#### TABLE 15-10: A/D CONVERSION REQUIREMENTS

These parameters are characterized but not tested.

Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are t not tested.

§ This specification ensured by design.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 11.1 "A/D Acquisition Requirements" for minimum conditions.



















FIGURE 16-19: TYPICAL, MINIMUM AND MAXIMUM Vol vs. Iol (VDD = 5V, -40°C TO +125°C)





NOTES:

### 20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS			
Dimension	n Limits	MIN	NOM	MAX	
Number of Pins	20				
Pitch	е	0.65 BSC			
Overall Height	Α	-	-	2.00	
Molded Package Thickness	A2	1.65	1.75	1.85	
Standoff	A1	0.05	-	-	
Overall Width	E	7.40	7.80	8.20	
Molded Package Width	E1	5.00	5.30	5.60	
Overall Length	D	6.90	7.20	7.50	
Foot Length	L	0.55	0.75	0.95	
Footprint	L1	1.25 REF			
Lead Thickness	С	0.09	_	0.25	
Foot Angle	φ	0°	4°	8°	
Lead Width	b	0.22	_	0.38	

#### Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.

- 3. Dimensioning and tolerancing per ASME Y14.5M.
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B