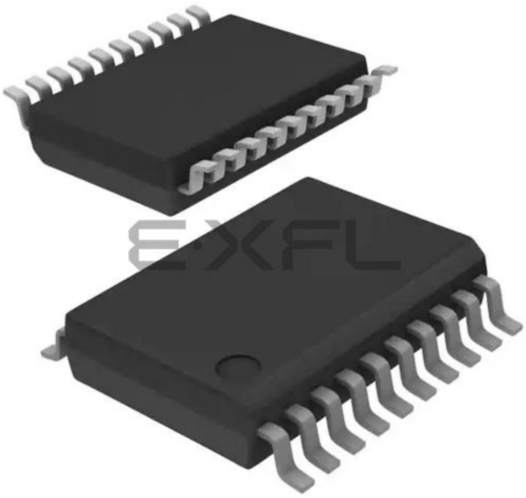
Microchip Technology - PIC16LF819T-I/SSTSL Datasheet



What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	10MHz
Connectivity	I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf819t-i-sstsl

FIGURE 2-4: PIC16F819 REGISTER FILE MAP

Bank 0	File Address	Bank 1	File Address	Bank 2	File Address	Bank 3	File Address
Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h	▨	105h	▨	185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
▨	07h	▨	87h	▨	107h	▨	187h
▨	08h	▨	88h	▨	108h	▨	188h
▨	09h	▨	89h	▨	109h	▨	189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	EEDATA	10Ch	EECON1	18Ch
PIR2	0Dh	PIE2	8Dh	EEADR	10Dh	EECON2	18Dh
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	▨ Reserved(1)	18Eh
TMR1H	0Fh	OSCCON	8Fh	EEADRH	10Fh	▨ Reserved(1)	18Fh
T1CON	10h	OSCTUNE	90h	▨	110h	▨	190h
TMR2	11h	▨	91h				
T2CON	12h	PR2	92h				
SSPBUF	13h	SSPADD	93h				
SSPCON	14h	SSPSTAT	94h				
CCPR1L	15h	▨	95h				
CCPR1H	16h	▨	96h				
CCP1CON	17h	▨	97h				
▨	18h	▨	98h				
▨	19h	▨	99h				
▨	1Ah	▨	9Ah				
▨	1Bh	▨	9Bh				
▨	1Ch	▨	9Ch				
▨	1Dh	▨	9Dh				
ADRESH	1Eh	ADRESL	9Eh				
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
General Purpose Register 96 Bytes	20h	General Purpose Register 80 Bytes	A0h	General Purpose Register 80 Bytes	120h	Accesses 20h-7Fh	1A0h
			EFh		16Fh		
		Accesses 70h-7Fh	F0h	Accesses 70h-7Fh	170h		
	7Fh		FFh		17Fh		1FFh

▨ Unimplemented data memory locations, read as ‘`0`’.

* Not a physical register.

Note 1: These registers are reserved; maintain these registers clear.

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral modules for controlling the desired operation of the device. These registers are implemented as static RAM. A list of these registers is given in Table 2-1.

The Special Function Registers can be classified into two sets: core (CPU) and peripheral. Those registers associated with the core functions are described in detail in this section. Those related to the operation of the peripheral features are described in detail in the peripheral feature section.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page:
Bank 0											
00h(1)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	23
01h	TMR0	Timer0 Module Register								xxxx xxxx	53, 17
02h(1)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	23
03h(1)	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	C	0001 1xxx	16
04h(1)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	23
05h	PORTA	PORTA Data Latch when written; PORTA pins when read								xxx0 0000	39
06h	PORTB	PORTB Data Latch when written; PORTB pins when read								xxxx xxxx	43
07h	—	Unimplemented								—	—
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	23
0Bh(1)	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	18
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0-- 0000	20
0Dh	PIR2	—	—	—	EEIF	—	—	—	—	---0 ----	21
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	57
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	57
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	--00 0000	57
11h	TMR2	Timer2 Module Register								0000 0000	63
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	64
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	71, 76
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	73
15h	CCPR1L	Capture/Compare/PWM Register (LSB)								xxxx xxxx	66, 67, 68
16h	CCPR1H	Capture/Compare/PWM Register (MSB)								xxxx xxxx	66, 67, 68
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	65
18h	—	Unimplemented								—	—
19h	—	Unimplemented								—	—
1Ah	—	Unimplemented								—	—
1Bh	—	Unimplemented								—	—
1Ch	—	Unimplemented								—	—
1Dh	—	Unimplemented								—	—
1Eh	ADRESH	A/D Result Register High Byte								xxxx xxxx	81
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON	0000 00-0	81

Legend: `x` = unknown, `u` = unchanged, `q` = value depends on condition, - = unimplemented, read as '`0`', `r` = reserved.
Shaded locations are unimplemented, read as '`0`'.

Note 1: These registers can be addressed from any bank.

2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter.

3: Pin 5 is an input only; the state of the TRISA5 bit has no effect and will always read '`1`'.

2.2.2.2 OPTION_REG Register

The OPTION_REG register is a readable and writable register that contains various control bits to configure the TMR0 prescaler/WDT postscaler (single assignable register known also as the prescaler), the external INT interrupt, TMR0 and the weak pull-ups on PORTB.

Note: To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer.

REGISTER 2-2: OPTION_REG: OPTION REGISTER (ADDRESS 81h, 181h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7 **$\overline{\text{RBPU}}$**: PORTB Pull-up Enable bit
`1` = PORTB pull-ups are disabled
`0` = PORTB pull-ups are enabled by individual port latch values

bit 6 **INTEDG:** Interrupt Edge Select bit
`1` = Interrupt on rising edge of RB0/INT pin
`0` = Interrupt on falling edge of RB0/INT pin

bit 5 **T0CS:** TMR0 Clock Source Select bit
`1` = Transition on T0CKI pin
`0` = Internal instruction cycle clock (CLKO)

bit 4 **T0SE:** TMR0 Source Edge Select bit
`1` = Increment on high-to-low transition on T0CKI pin
`0` = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
`1` = Prescaler is assigned to the WDT
`0` = Prescaler is assigned to the Timer0 module

bit 2-0 **PS2:PS0:** Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
`000`	1 : 2	1 : 1
`001`	1 : 4	1 : 2
`010`	1 : 8	1 : 4
`011`	1 : 16	1 : 8
`100`	1 : 32	1 : 16
`101`	1 : 64	1 : 32
`110`	1 : 128	1 : 64
`111`	1 : 256	1 : 128

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

REGISTER 3-1: EECON1: EEPROM ACCESS CONTROL REGISTER 1 (ADDRESS 18Ch)

R/W-x	U-0	U-0	R/W-x	R/W-x	R/W-0	R/S-0	R/S-0
EEPGD	—	—	FREE	WRERR	WREN	WR	RD

bit 7 bit 0

bit 7 **EEPGD**: Program/Data EEPROM Select bit

`1` = Accesses program memory
`0` = Accesses data memory
Reads '`0`' after a POR; this bit cannot be changed while a write operation is in progress.

bit 6-5 **Unimplemented:** Read as '`0`'

bit 4 **FREE:** EEPROM Forced Row Erase bit

`1` = Erase the program memory row addressed by EEADRH:EEADR on the next WR command
`0` = Perform write-only

bit 3 **WRERR:** EEPROM Error Flag bit

`1` = A write operation is prematurely terminated (any $\overline{\text{MCLR}}$ or any WDT Reset during normal operation)
`0` = The write operation completed

bit 2 **WREN:** EEPROM Write Enable bit

`1` = Allows write cycles
`0` = Inhibits write to the EEPROM

bit 1 **WR:** Write Control bit

`1` = Initiates a write cycle. The bit is cleared by hardware once write is complete. The WR bit can only be set (not cleared) in software.
`0` = Write cycle to the EEPROM is complete

bit 0 **RD:** Read Control bit

`1` = Initiates an EEPROM read, RD is cleared in hardware. The RD bit can only be set (not cleared) in software.
`0` = Does not initiate an EEPROM read

Legend:

R = Readable bit	W = Writable bit	S = Set only	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

An example of the complete four-word write sequence is shown in Example 3-5. The initial address is loaded into the EEADRH:EEADR register pair; the four words of data are loaded using indirect addressing, assuming that a row erase sequence has already been performed.

EXAMPLE 3-5: WRITING TO FLASH PROGRAM MEMORY

```
; This write routine assumes the following:

; 1. The 32 words in the erase block have already been erased.
; 2. A valid starting address (the least significant bits = '00') is loaded into EEADRH:EEADR
; 3. This example is starting at 0x100, this is an application dependent setting.
; 4. The 8 bytes (4 words) of data are loaded, starting at an address in RAM called ARRAY.
; 5. This is an example only, location of data to program is application dependent.
; 6. word_block is located in data memory.

       BANKSEL  EECON1            ;prepare for WRITE procedure
       BSF      EECON1, EEPGD     ;point to program memory
       BSF      EECON1, WREN      ;allow write cycles
       BCF      EECON1, FREE      ;perform write only

       BANKSEL  word_block
       MOVLW    .4
       MOVWF    word_block        ;prepare for 4 words to be written

       BANKSEL  EEADRH            ;Start writing at 0x100
       MOVLW    0x01
       MOVWF    EEADRH            ;load HIGH address
       MOVLW    0x00
       MOVWF    EEADR             ;load LOW address
       BANKSEL  ARRAY
       MOVLW    ARRAY             ;initialize FSR to start of data
       MOVWF    FSR
LOOP
       BANKSEL  EEDATA
       MOVF     INDF, W           ;indirectly load EEDATA
       MOVWF    EEDATA
       INCF     FSR, F            ;increment data pointer
       MOVF     INDF, W           ;indirectly load EEDATH
       MOVWF    EEDATH
       INCF     FSR, F            ;increment data pointer

       BANKSEL  EECON1
       MOVLW    0x55              ;required sequence
       MOVWF    EECON2
       MOVLW    0xAA
       MOVWF    EECON2
       BSF      EECON1, WR        ;set WR bit to begin write
       NOP                        ;instructions here are ignored as processor
       NOP

       BANKSEL  EEADR
       INCF     EEADR, f          ;load next word address
       BANKSEL  word_block
       DECFSZ   word_block, f     ;have 4 words been written?
       GOTO     loop              ;NO, continue with writing

       BANKSEL  EECON1
       BCF      EECON1, WREN      ;YES, 4 words complete, disable writes
       BSF      INTCON, GIE       ;enable interrupts
```

Required Sequence

7.6 Timer1 Oscillator

A crystal oscillator circuit is built-in between pins T1OSI (input) and T1OSO (amplifier output). It is enabled by setting control bit, T1OSCEN (T1CON<3>). The oscillator is a low-power oscillator, rated up to 32.768 kHz. It will continue to run during Sleep. It is primarily intended for a 32 kHz crystal. The circuit for a typical LP oscillator is shown in Figure 7-3. Table 7-1 shows the capacitor selection for the Timer1 oscillator.

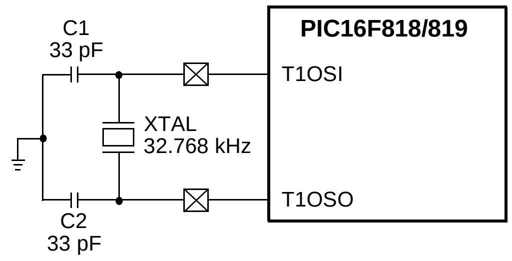
The user must provide a software time delay to ensure proper oscillator start-up.

Note: The Timer1 oscillator shares the T1OSI and T1OSO pins with the PGD and PGC pins used for programming and debugging.

When using the Timer1 oscillator, In-Circuit Serial Programming™ (ICSP™) may not function correctly (high-voltage or low-voltage) or the In-Circuit Debugger (ICD) may not communicate with the controller. As a result of using either ICSP or ICD, the Timer1 crystal may be damaged.

If ICSP or ICD operations are required, the crystal should be disconnected from the circuit (disconnect either lead) or installed after programming. The oscillator loading capacitors may remain in-circuit during ICSP or ICD operation.

FIGURE 7-3: EXTERNAL COMPONENTS FOR THE TIMER1 LP OSCILLATOR



Note: See the Notes with Table 7-1 for additional information about capacitor selection.

TABLE 7-1: CAPACITOR SELECTION FOR THE TIMER1 OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 kHz	33 pF	33 pF

Note 1: Microchip suggests this value as a starting point in validating the oscillator circuit.

2: Higher capacitance increases the stability of the oscillator but also increases the start-up time.

3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.

4: Capacitor values are for design guidance only.

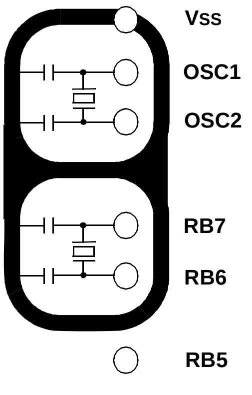
7.7 Timer1 Oscillator Layout Considerations

The Timer1 oscillator circuit draws very little power during operation. Due to the low-power nature of the oscillator, it may also be sensitive to rapidly changing signals in close proximity.

The oscillator circuit, shown in Figure 7-3, should be located as close as possible to the microcontroller. There should be no circuits passing within the oscillator circuit boundaries other than V_{SS} or V_{DD}.

If a high-speed circuit must be located near the oscillator, a grounded guard ring around the oscillator circuit, as shown in Figure 7-4, may be helpful when used on a single-sided PCB or in addition to a ground plane.

FIGURE 7-4: OSCILLATOR CIRCUIT WITH GROUNDED GUARD RING



9.1 Capture Mode

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on the CCP1 pin. An event is defined as:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

An event is selected by control bits, CCP1M3:CCP1M0 (CCP1CON<3:0>). When a capture is made, the interrupt request flag bit, CCP1IF (PIR1<2>), is set. It must be cleared in software. If another capture occurs before the value in register CCPR1 is read, the old captured value is overwritten by the new captured value.

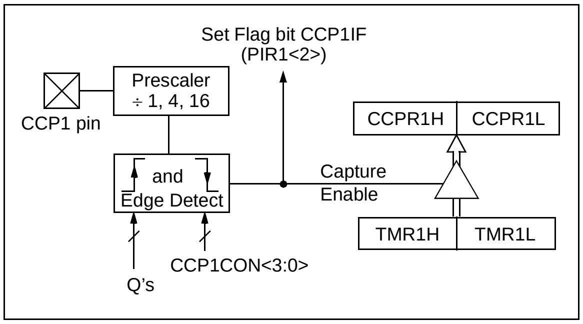
9.1.1 CCP PIN CONFIGURATION

In Capture mode, the CCP1 pin should be configured as an input by setting the TRISB<x> bit.

Note 1: If the CCP1 pin is configured as an output, a write to the port can cause a capture condition.

2: The TRISB bit (2 or 3) is dependent upon the setting of configuration bit 12 (CCPMX).

FIGURE 9-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



9.1.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

9.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep bit, CCP1IE (PIE1<2>), clear to avoid false interrupts and should clear the flag bit, CCP1IF, following any such change in operating mode.

9.1.4 CCP PRESCALER

There are four prescaler settings specified by bits CCP1M3:CCP1M0. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. This means that any Reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared; therefore, the first capture may be from a non-zero prescaler. Example 9-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the “false” interrupt.

EXAMPLE 9-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
CLRF   CCP1CON     ;Turn CCP module off
MOVLW  NEW_CAPT_PS ;Load the W reg with
                   ;the new prescaler
                   ;move value and CCP ON
MOVWF  CCP1CON     ;Load CCP1CON with this
                   ;value
```

NOTES:

14.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

14.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip’s next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC® Flash MCUs and dsPIC® Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer’s PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

14.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC® Flash microcontrollers and dsPIC® DSCs with the powerful, yet easy-to-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

14.10 PICkit 3 In-Circuit Debugger/Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC® and dsPIC® Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming™.

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user’s guide, lessons, tutorial, compiler and MPLAB IDE software.

15.2 DC Characteristics: Power-Down and Supply Current PIC16F818/819 (Industrial, Extended) PIC16LF818/819 (Industrial) (Continued)

PIC16LF818/819 (Industrial)	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial
PIC16F818/819 (Industrial, Extended)	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended

Param No.	Device	Typ	Max	Units	Conditions		
	Supply Current (IDD)[2,3]						
	PIC16LF818/819	9	20	μA	-40°C	VDD = 2.0V	FOSC = 32 kHz (LP Oscillator)
		7	15	μA	+25°C		
		7	15	μA	+85°C		
	PIC16LF818/819	16	30	μA	-40°C	VDD = 3.0V	
		14	25	μA	+25°C		
		14	25	μA	+85°C		
	All devices	32	40	μA	-40°C	VDD = 5.0V	
		26	35	μA	+25°C		
		26	35	μA	+85°C		
	Extended devices	35	53	μA	+125°C		

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
$\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.

15.2 DC Characteristics: Power-Down and Supply Current PIC16F818/819 (Industrial, Extended) PIC16LF818/819 (Industrial) (Continued)

PIC16LF818/819 (Industrial)	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +85°C for industrial
PIC16F818/819 (Industrial, Extended)	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +85°C for industrial -40°C ≤ T_A ≤ +125°C for extended

Param No.	Device	Typ	Max	Units	Conditions		
	Supply Current (I_{DD})[2,3]						
	PIC16LF818/819	72	95	µA	-40°C	V_{DD} = 2.0V	F_{OSC} = 1 MHz (RC Oscillator)[3]
		76	90	µA	+25°C		
		76	90	µA	+85°C		
	PIC16LF818/819	138	175	µA	-40°C	V_{DD} = 3.0V	
		136	170	µA	+25°C		
		136	170	µA	+85°C		
	All devices	310	380	µA	-40°C	V_{DD} = 5.0V	
		290	360	µA	+25°C		
		280	360	µA	+85°C		
	Extended devices	350	500	µA	+125°C		
	PIC16LF818/819	270	315	µA	-40°C	V_{DD} = 2.0V	F_{OSC} = 4 MHz (RC Oscillator)[3]
		280	310	µA	+25°C		
		285	310	µA	+85°C		
	PIC16LF818/819	460	610	µA	-40°C	V_{DD} = 3.0V	
		450	600	µA	+25°C		
		450	600	µA	+85°C		
	All devices	900	1060	µA	-40°C	V_{DD} = 5.0V	
		890	1050	µA	+25°C		
		890	1050	µA	+85°C		
	Extended devices	.920	1.5	mA	+125°C		

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{DD} or V_{SS} and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all I_{DD} measurements in active operation mode are:
$\underline{\text{OSC1}}$ = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD};
$\overline{\text{MCLR}}$ = V_{DD}; WDT enabled/disabled as specified.

3: For RC oscillator configurations, current through R_{EXT} is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in kΩ.

15.2 DC Characteristics: Power-Down and Supply Current PIC16F818/819 (Industrial, Extended) PIC16LF818/819 (Industrial) (Continued)

PIC16LF818/819 (Industrial)	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial
PIC16F818/819 (Industrial, Extended)	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended

Param No.	Device	Typ	Max	Units	Conditions		
D022 (ΔIWDT)	**Module Differential Currents (ΔIWDT, ΔIBOR, ΔILVD, ΔIOSCB, ΔIAD)**						
	Watchdog Timer	1.5	3.8	µA	-40°C	VDD = 2.0V	
		2.2	3.8	µA	+25°C		
		2.7	4.0	µA	+85°C		
		2.3	4.6	µA	-40°C	VDD = 3.0V	
		2.7	4.6	µA	+25°C		
		3.1	4.8	µA	+85°C		
		3.0	10.0	µA	-40°C	VDD = 5.0V	
		3.3	10.0	µA	+25°C		
		3.9	13.0	µA	+85°C		
	Extended Devices	5.0	21.0	µA	+125°C		
D022A (ΔIBOR)	**Brown-out Reset**	40	60	µA	-40°C to +85°C	VDD = 5.0V	
D025 (ΔIOSCB)	**Timer1 Oscillator**	1.7	2.3	µA	-40°C	VDD = 2.0V	32 kHz on Timer1
		1.8	2.3	µA	+25°C		
		2.0	2.3	µA	+85°C		
		2.2	3.8	µA	-40°C	VDD = 3.0V	
		2.6	3.8	µA	+25°C		
		2.9	3.8	µA	+85°C		
		3.0	6.0	µA	-40°C	VDD = 5.0V	
		3.2	6.0	µA	+25°C		
		3.4	7.0	µA	+85°C		
D026 (ΔIAD)	**A/D Converter**	0.001	2.0	µA	-40°C to +85°C	VDD = 2.0V	A/D on, Sleep, not converting
		0.001	2.0	µA	-40°C to +85°C	VDD = 3.0V	
		0.003	2.0	µA	-40°C to +85°C	VDD = 5.0V	
	Extended Devices	4.0	8.0	µA	-40°C to +125°C		

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
$\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.

15.3 DC Characteristics: Internal RC Accuracy
PIC16F818/819, PIC16F818/819 TSL (Industrial, Extended)
PIC16LF818/819, PIC16LF818/819 TSL (Industrial)

PIC16LF818/819(3) **PIC16LF818/819 TSL(3)** (Industrial)	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial
PIC16F818/819(3) **PIC16F818/819 TSL(3)** (Industrial, Extended)	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended

Param No.	Device	Min	Typ	Max	Units	Conditions	
	INTOSC Accuracy @ Freq = 8 MHz, 4 MHz, 2 MHz, 1 MHz, 500 kHz, 250 kHz, 125 kHz(1)						
	PIC16LF818/819	-5	±1	5	%	+25°C	VDD = 2.7-3.3V
		-25	—	25	%	-10°C to +85°C	
		-30	—	30	%	-40°C to +85°C	
	PIC16F818/819(4)	-5	±1	5	%	+25°C	VDD = 4.5-5.5V
		-25	—	25	%	-10°C to +85°C	
		-30	—	30	%	-40°C to +85°C	
		-35	—	35	%	-40°C to +125°C	
	PIC16LF818/819 TSL	-2	±1	2	%	+25°C	VDD = 2.7-3.3V
		-5	—	5	%	-10°C to +85°C	
		-10	—	10	%	-40°C to +85°C	
	PIC16F818/819 TSL(5)	-2	±1	2	%	+25°C	VDD = 4.5-5.5V
		-5	—	5	%	-10°C to +85°C	
		-10	—	10	%	-40°C to +85°C	
		-15	—	15	%	-40°C to +125°C	
	INTRC Accuracy @ Freq = 31 kHz(2)						
	PIC16LF818/819	26.562	—	35.938	kHz	-40°C to +85°C	VDD = 2.7-3.3V
	PIC16F818/819(4)	26.562	—	35.938	kHz	-40°C to +85°C	VDD = 4.5-5.5V
	PIC16LF818/819 TSL	26.562	—	35.938	kHz	-40°C to +85°C	VDD = 2.7-3.3V
	PIC16F818/819 TSL(5)	26.562	—	35.938	kHz	-40°C to +85°C	VDD = 4.5-5.5V

Legend: Shading of rows is to assist in readability of the table.

Note 1: Frequency calibrated at 25°C. OSCTUNE register can be used to compensate for temperature drift.

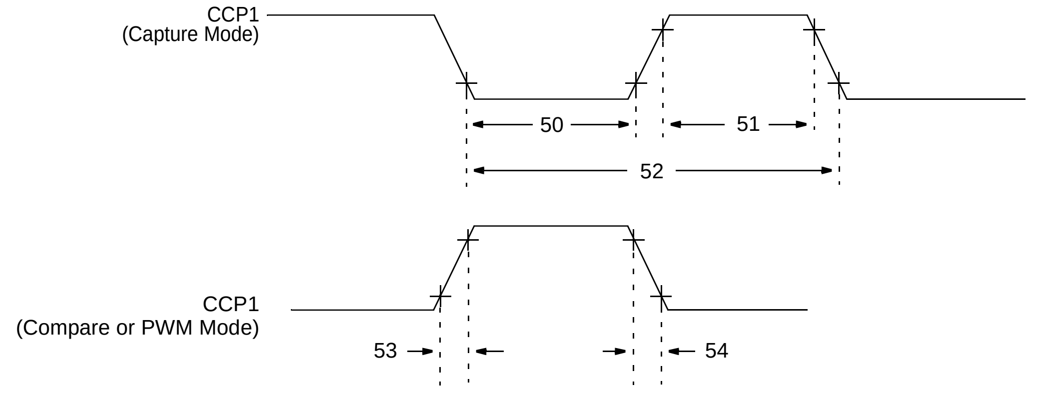
2: INTRC frequency after calibration.

3: The only specification difference between a non-TSL device and a TSL device is the internal RC oscillator specifications listed above. All other specifications are maintained.

4: Example part number for the specifications listed above: PIC16F818-I/SS (PIC16F818 device, Industrial temperature, SSOP package).

5: Example part number for the specifications listed above: PIC16F818-I/SSTSL (PIC16F818 device, Industrial temperature, SSOP package).

FIGURE 15-9: CAPTURE/COMPARE/PWM TIMINGS (CCP1)



Note: Refer to Figure 15-3 for load conditions.

TABLE 15-5: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1)

Param No.	Symbol	Characteristic			Min	Typ†	Max	Units	Conditions
50*	TCCL	CCP1 Input Low Time	No Prescaler		0.5 TCY + 20	—	—	ns	
			With Prescaler	PIC16**F**818/819	10	—	—	ns	
				PIC16**LF**818/819	20	—	—	ns	
51*	TCCH	CCP1 Input High Time	No Prescaler		0.5 TCY + 20	—	—	ns	
			With Prescaler	PIC16**F**818/819	10	—	—	ns	
				PIC16**LF**818/819	20	—	—	ns	
52*	TCCP	CCP1 Input Period			$\frac{3 \text{ TCY} + 40}{N}$	—	—	ns	N = prescale value (1,4 or 16)
53*	TCCR	CCP1 Output Rise Time		PIC16**F**818/819	—	10	25	ns	
				PIC16**LF**818/819	—	25	50	ns	
54*	TCCF	CCP1 Output Fall Time		PIC16**F**818/819	—	10	25	ns	
				PIC16**LF**818/819	—	25	45	ns	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 15-12: SPI SLAVE MODE TIMING (CKE = 0)

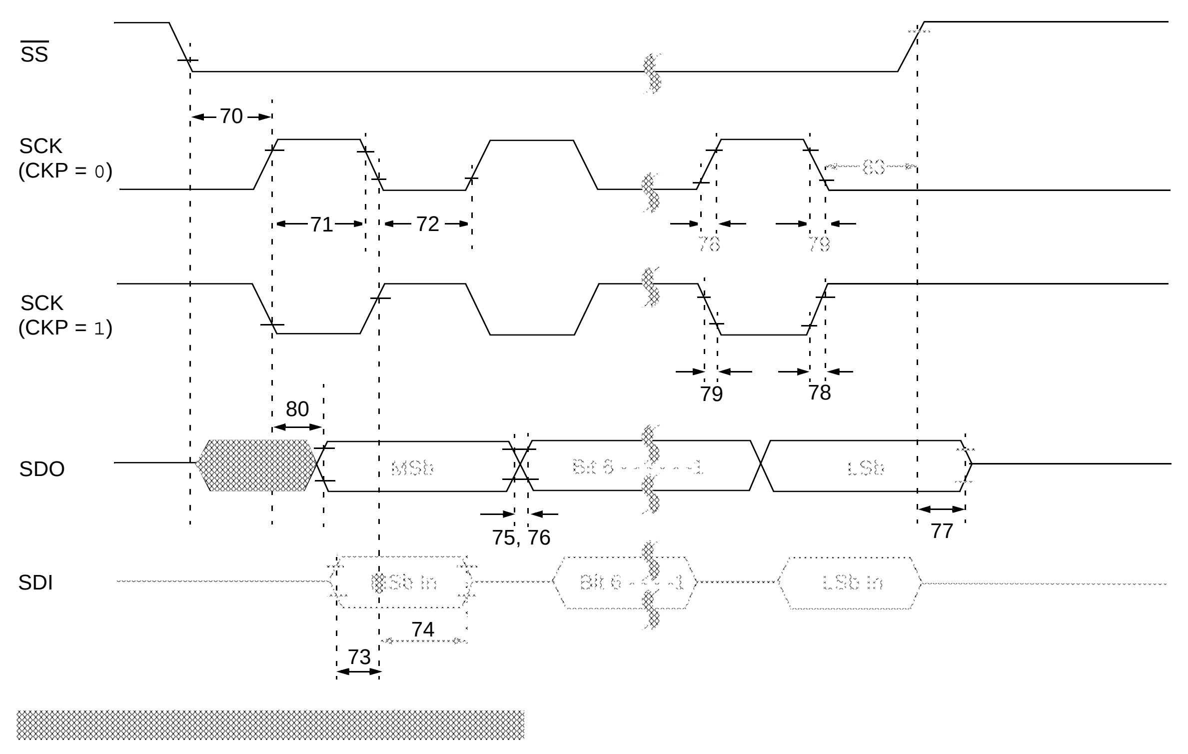


FIGURE 15-13: SPI SLAVE MODE TIMING (CKE = 1)

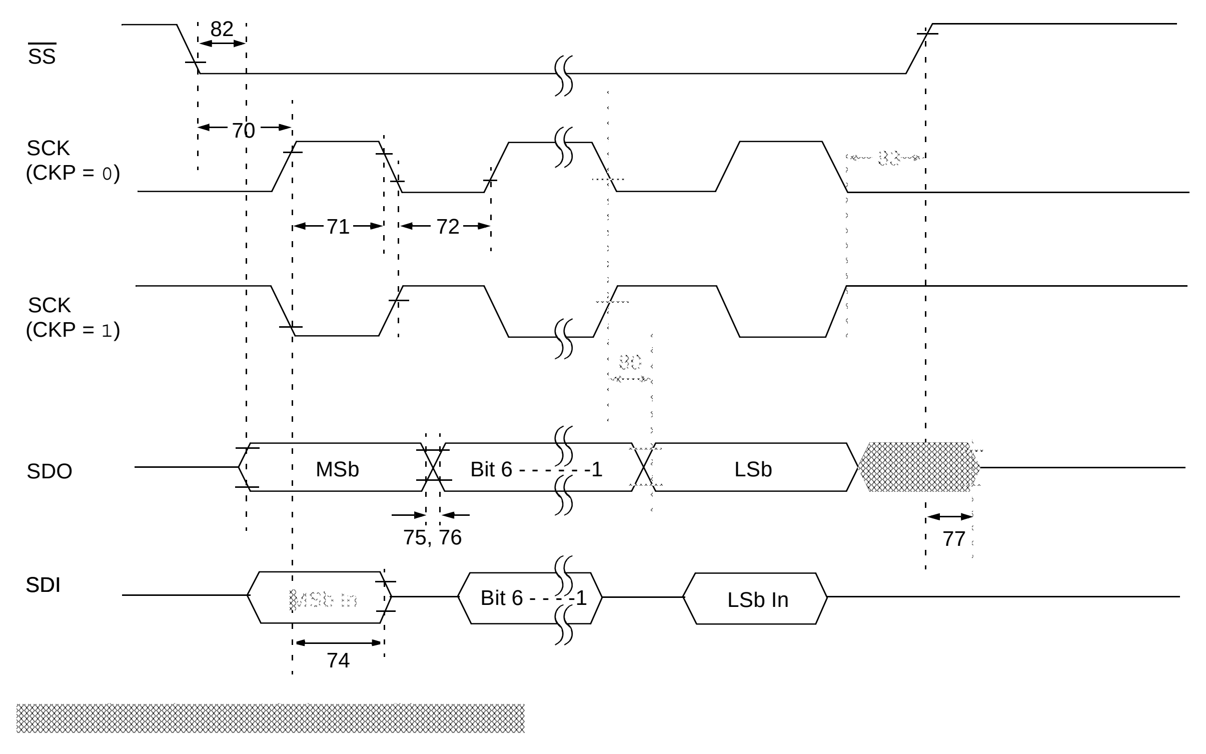
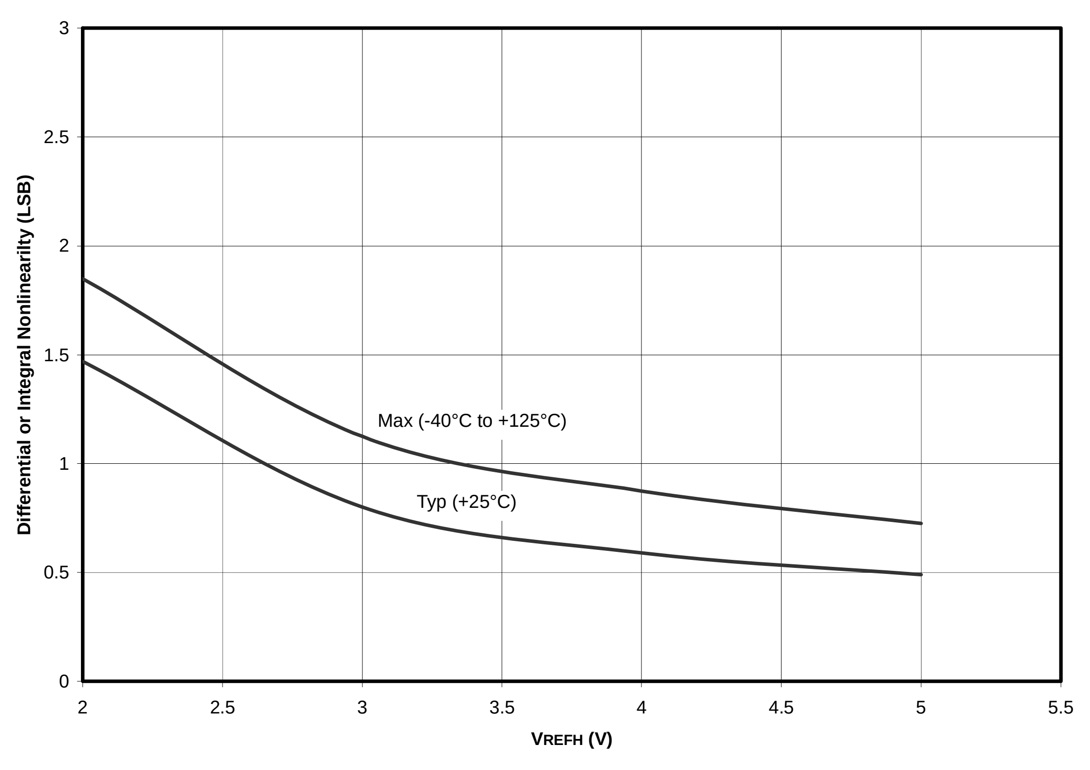
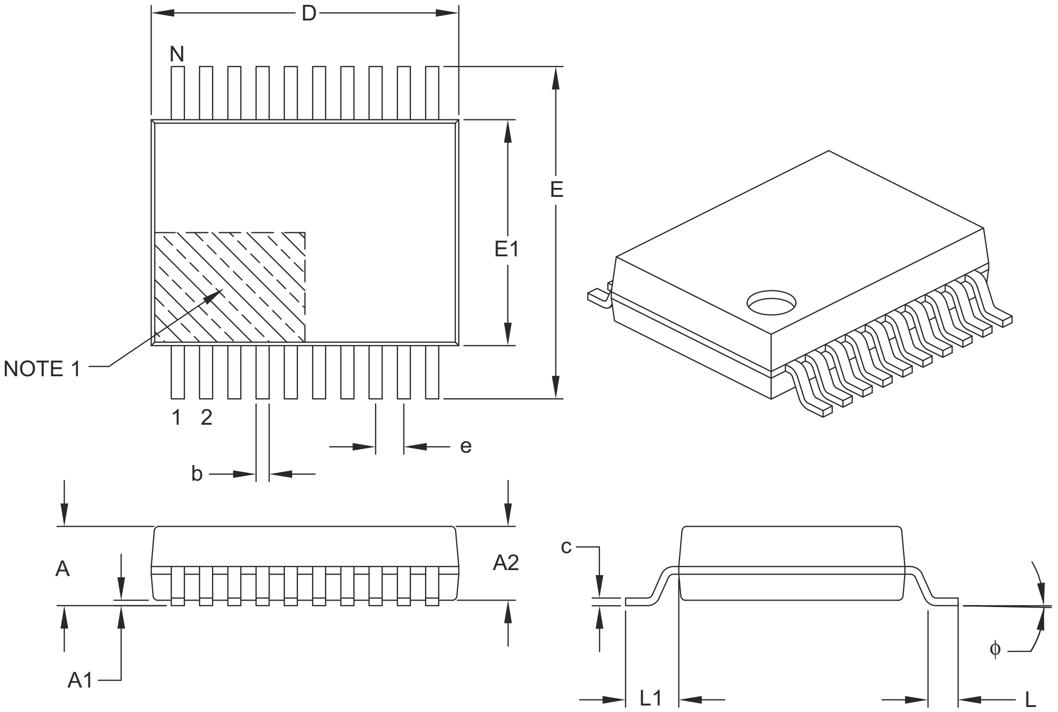


FIGURE 16-25: A/D NONLINEARITY vs. VREFH (VDD = 5V, -40°C TO +125°C)



20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	20		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1	1.25 REF		
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

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PIC16F818/819 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device	PIC16F818: Standard VDD range PIC16F818T: (Tape and Reel) PIC16LF818: Extended VDD range
Temperature Range	- = 0°C to +70°C I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)
Package	P = PDIP SO = SOIC SS = SSOP ML = QFN
Pattern	QTP, SQTP, ROM Code (factory specified) or Special Requirements. Blank for OTP and Windowed devices.

Examples:

a) PIC16LF818-I/P = Industrial temp., PDIP package, Extended VDD limits.

b) PIC16F818-I/SO = Industrial temp., SOIC package, normal VDD limits.

Note 1: F = CMOS Flash
LF = Low-Power CMOS Flash
2: T = in tape and reel – SOIC, SSOP packages only.