Infineon Technologies - SAK-TC1762-128F66HL AC Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	ASC, CANbus, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	81
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	52K x 8
Voltage - Supply (Vcc/Vdd)	1.42V ~ 1.58V
Data Converters	A/D 2x10b, 32x8b/10b/12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	PG-LQFP-176-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-tc1762-128f66hl-ac

1 Summary of Features

The TC1762 has the following features:

- High-performance 32-bit super-scaler TriCore v1.3 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 66 or 80 MHz operation at full temperature range
- Multiple on-chip memories
  - 32 Kbyte Local Data Memory (SRAM)
  - 4 Kbyte Overlay Memory
  - 8 Kbyte Scratch-Pad RAM (SPRAM)
  - 8 Kbyte Instruction Cache (ICACHE)
  - 1024 Kbyte Flash Memory
  - 16 Kbyte Data Flash (2 Kbyte EEPROM emulation)
  - 16 Kbyte Boot ROM
- 8-channel DMA Controller
- Fast-response interrupt system with 255 hardware priority arbitration levels serviced by CPU
- High-performance on-chip bus structure
  - 64-bit Local Memory Bus (LMB) to Flash memory
  - System Peripheral Bus (SPB) for interconnections of functional units
- Versatile on-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASCs) with baudrate generator, parity, framing and overrun error detection
  - One High Speed Synchronous Serial Channel (SSC) with programmable data length and shift direction
  - One Micro Second Bus (MSC) interface for serial port expansion to external power devices
  - One high-speed Micro Link Interface (MLI) for serial inter-processor communication
  - One MultiCAN Module with two CAN nodes and 64 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer
  - One General Purpose Timer Array Module (GPTA) with a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - One 16-channel Analog-to-Digital Converter unit (ADC) with selectable 8-bit, 10-bit, or 12-bit, supporting 32 input channels
  - One 2-channel Fast Analog-to-Digital Converter unit (FADC) with concatenated comb filters for hardware data reduction: supporting 10-bit resolution, with minimum conversion time of 262.5ns (@ 80 MHz) or 318.2ns (@ 66 MHz)

2.5 Pin Definitions and Functions

Table 2-1 shows the TC1762 pin definitions and functions.

Table 2-1 Pin Definitions and Functions

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
Parallel Ports					
P0		I/O	A1	V_{DDP}	**Port 0** Port 0 is a 16-bit bi-directional general-purpose I/O port which can be alternatively used for GPTA I/O lines or external trigger inputs.
P0.0	145				IN0 / OUT0 / OUT56 line of GPTA
P0.1	146				IN1 / OUT1 / OUT57 line of GPTA
P0.2	147				IN2 / OUT2 / OUT58 line of GPTA
P0.3	148				IN3 / OUT3 / OUT59 line of GPTA
P0.4	166				IN4 / OUT4 / OUT60 line of GPTA
P0.5	167				IN5 / OUT5 / OUT61 line of GPTA
P0.6	173				IN6 / OUT6 / OUT62 line of GPTA REQ2 External trigger input 2
P0.7	174				IN7 / OUT7 / OUT63 line of GPTA REQ3 External trigger input 3
P0.8	149				IN8 / OUT8 / OUT64 line of GPTA
P0.9	150				IN9 / OUT9 / OUT65 line of GPTA
P0.10	151				IN10 / OUT10 / OUT66 line of GPTA
P0.11	152				IN11 / OUT11 / OUT67 line of GPTA
P0.12	168				IN12 / OUT12 / OUT68 line of GPTA
P0.13	169				IN13 / OUT13 / OUT69 line of GPTA
P0.14	175				IN14 / OUT14 / OUT70 line of GPTA REQ4 External trigger input 4
P0.15	176				IN15 / OUT15 / OUT71 line of GPTA REQ5 External trigger input 5
					In addition, the state of the port pins are latched into the software configuration input register SCU_SCLIR at the rising edge of HDRST. Therefore, Port 0 pins can be used for operating mode selections by software.

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions	
P2		I/O		V_{DDP}	**Port 2** Port 2 is a 14-bit bi-directional general-purpose I/O port which can be alternatively used for GPTA I/O, and interface for MLI0, MSC0 or SSC0.	
P2.0	74		A2		TCLK0	MLI0 transmit channel clock output A
					IN32 / OUT32	line of GPTA
P2.1	75		A2		TREADY0A	MLI0 transmit channel ready input A
					IN33 / OUT33	line of GPTA
					SLSO03	SSC0 slave select output 3
P2.2	76		A2		TVALID0A	MLI0 transmit channel valid output A
					IN34 / OUT34	line of GPTA
P2.3	77		A2		TDATA0	MLI0 transmit channel data output A
					IN35 / OUT35	line of GPTA
P2.4	78		A1		RCLK0A	MLI0 receive channel clock input A
					IN36 / OUT36	line of GPTA
P2.5	79		A2		RREADY0A	MLI0 receive channel ready output A
					IN37 / OUT37	line of GPTA
P2.6	80		A1		RVALID0A	MLI0 receive channel valid input A
					IN38 / OUT38	line of GPTA
P2.7	81		A1		RDATA0A	MLI0 receive channel data input A
					IN39 / OUT39	line of GPTA

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
MSC0 Outputs					
			C	V_{DDP}	**LVDS MSC Clock and Data Outputs**[2)]
FCLP0A	157	O			MSC0 Differential Driver Clock Output Positive A
FCLN0	156	O			MSC0 Differential Driver Clock Output Negative
SOP0A	159	O			MSC0 Differential Driver Serial Data Output Positive A
SON0	158	O			MSC0 Differential Driver Serial Data Output Negative

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
Power Supplies					
V_{DDM}	54	–	–	–	**ADC Analog Part Power Supply (3.3 V)**
V_{SSM}	53	–	–	–	**ADC Analog Part Ground for V_{DDM}**
V_{DDMF}	24	–	–	–	**FADC Analog Part Power Supply (3.3 V)**
V_{SSMF}	25	–	–	–	**FADC Analog Part Ground for V_{DDMF}**
V_{DDAF}	23	–	–	–	**FADC Analog Part Logic Power Supply (1.5 V)**
V_{SSAF}	22	–	–	–	**FADC Analog Part Logic Ground for V_{DDAF}**
V_{AREF0}	52	–	–	–	**ADC Reference Voltage**
V_{AGND0}	51	–	–	–	**ADC Reference Ground**
V_{FAREF}	26	–	–	–	**FADC Reference Voltage**
V_{FAGND}	27	–	–	–	**FADC Reference Ground**
V_{DDOSC}	105	–	–	–	**Main Oscillator and PLL Power Supply (1.5 V)**
V_{DDOSC3}	106	–	–	–	**Main Oscillator Power Supply (3.3 V)**
V_{SSOSC}	104	–	–	–	**Main Oscillator and PLL Ground**
V_{DDFL3}	141	–	–	–	**Power Supply for Flash (3.3 V)**
V_{DD}	10, 68, 84, 99, 123, 153, 170	–	–	–	**Core Power Supply (1.5 V)**

3.3 Architectural Address Map

Table 3-1 shows the overall architectural address map as defined for the TriCore and as implemented in TC1762.

Table 3-1 TC1762 Architectural Address Map

Segment	Contents	Size	Description
0-7	Global	8 x 256 Mbyte	Reserved (MMU space); cached
8	Global Memory	256 Mbyte	Reserved (246 Mbyte); PMU, Boot ROM; cached
9	Global Memory	256 Mbyte	FPI space; cached
10	Global Memory	256 Mbyte	Reserved (246 Mbyte), PMU, Boot ROM; non-cached
11	Global Memory	256 Mbyte	FPI space; non-cached
12	Local LMB Memory	256 Mbyte	Reserved; bottom 4 Mbyte visible from FPI bus in segment 14; cached
13	DMI	64 Mbyte	Local Data Memory RAM; non-cached
	PMI	64 Mbyte	Local Code Memory RAM; non-cached
	EXT_PER	96 Mbyte	Reserved; non-cached
	EXT_EMU	16 Mbyte	Reserved; non-cached
	BOOTROM	16 Mbyte	Boot ROM space, Boot ROM mirror; non-cached
14	EXTPER	128 Mbyte	Reserved; non-speculative; non-cached; no execution
	CPU[0 ..15] image region	16 x 8 Mbyte	Non-speculative; non-cached; no execution
15	LMB_PER CSFRs INT_PER	256 Mbyte	CSFRs of CPUs[0 ..15]; LMB & FPI Peripheral Space; non-speculative; non-cached; no execution

3.6 Interrupt System

The TC1762 interrupt system provides a flexible and time-efficient means of processing interrupts. An interrupt request is serviced by the CPU, which is called the “Service Provider”. Interrupt requests are called “Service Requests” rather than “Interrupt Requests” in this document.

Each peripheral in the TC1762 can generate service requests. Additionally, the Bus Control Units, the Debug Unit, and even the CPU itself can generate service requests to the Service Provider.

As shown in **Figure 3-2**, each TC1762 unit that can generate service requests is connected to one or multiple Service Request Nodes (SRN). Each SRN contains a Service Request Control Register mod_SRCx, where “mod” is the identifier of the service requesting unit and “x” an optional index. The CPU Interrupt Arbitration Bus connects the SRNs with the Interrupt Control Unit (ICU), which arbitrates service requests for the CPU and administers the CPU Interrupt Arbitration Bus.

The Debug Unit can generate service requests to the CPU. The CPU makes service requests directly to itself (via the ICU). The CPU Service Request Nodes are activated through software.

Depending on the selected system clock frequency f_{SYS}, the number of f_{SYS} clock cycles per arbitration cycle must be selected as follows:

- $f_{SYS} < 60$ MHz: ICR.CONECYC = 1
- $f_{SYS} > 60$ MHz: ICR.CONECYC = 0

3.7 Asynchronous/Synchronous Serial Interfaces (ASC0, ASC1)

Figure 3-3 shows a global view of the functional blocks and interfaces of the two Asynchronous/Synchronous Serial Interfaces, ASC0 and ASC1.

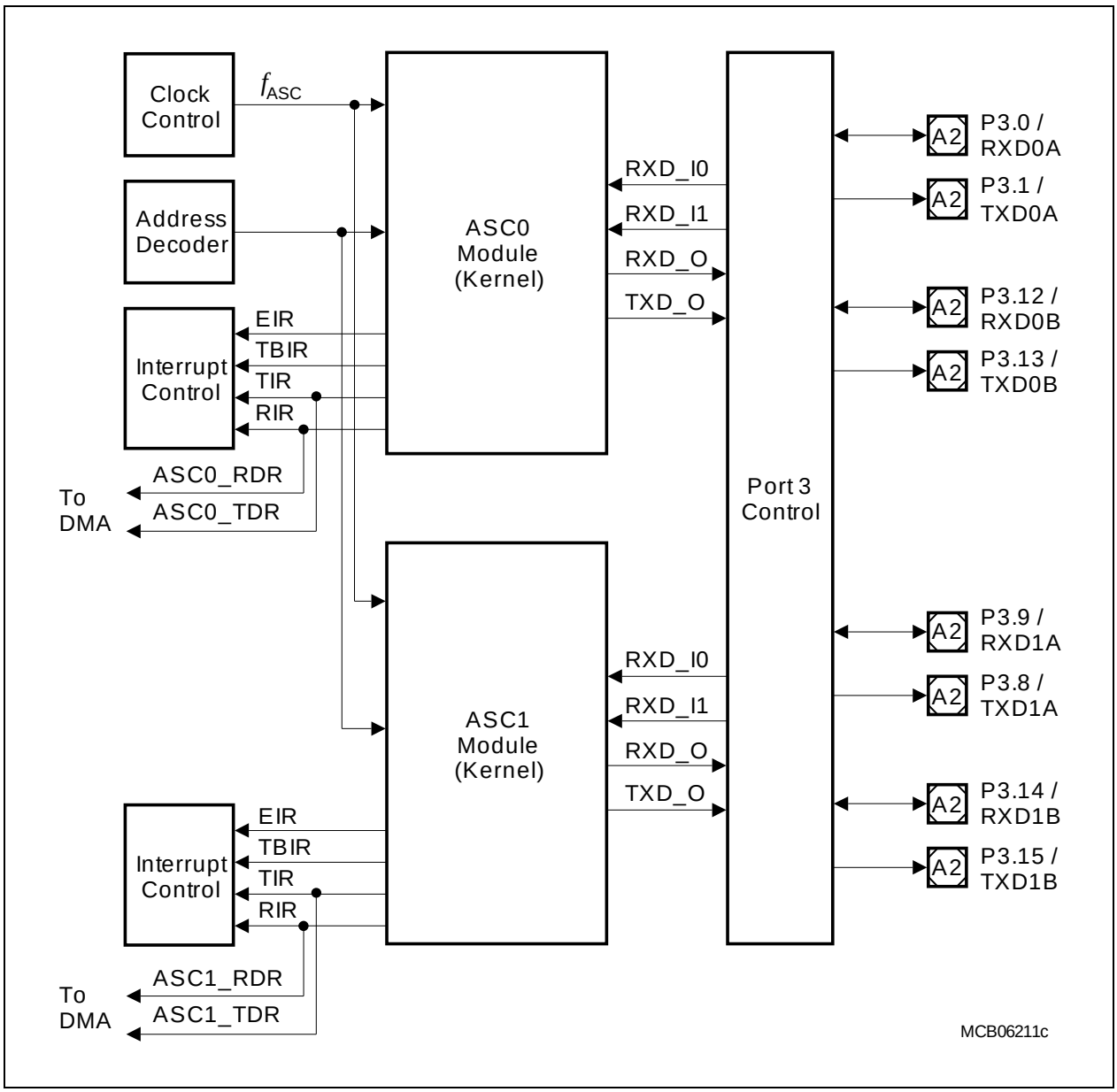

Figure 3-3 Block Diagram of the ASC Interfaces

The ASC provides serial communication between the TC1762 and other microcontrollers, microprocessors, or external peripherals.

The ASC supports full-duplex asynchronous communication and half-duplex synchronous communication. In Synchronous Mode, data is transmitted or received synchronous to a shift clock that is generated by the ASC internally. In Asynchronous Mode, 8-bit or 9-bit data transfer, parity generation, and the number of stop bits can be

Clock control, address decoding, and interrupt service request control are managed outside the MSC module kernel. Service request outputs are able to trigger an interrupt or a DMA request.

Features

- Fast synchronous serial interface to connect power switches in particular, or other peripheral devices via serial buses
- High-speed synchronous serial transmission on downstream channel
  - Serial output clock frequency: $f_{FCL} = f_{MSC}/2$
  - Fractional clock divider for precise frequency control of serial clock f_{MSC}
  - Command, data, and passive frame types
  - Start of serial frame: Software-controlled, timer-controlled, or free-running
  - Programmable upstream data frame length (16 or 12 bits)
  - Transmission with or without SEL bit
  - Flexible chip select generation indicates status during serial frame transmission
  - Emergency stop without CPU intervention
- Low-speed asynchronous serial reception on upstream channel
  - Baud rate: f_{MSC} divided by 4, 8, 16, 32, 64, 128, or 256
  - Standard asynchronous serial frames
  - Parity error checker
  - 8-to-1 input multiplexer for SDI lines
  - Built-in spike filter on SDI lines

same time when the lower part is read. The second read operation would then read the content of the STM_CAP to get the complete timer value.

The STM can also be read in sections from seven registers, STM_TIM0 through STM_TIM6, that select increasingly higher-order 32-bit ranges of the STM. These can be viewed as individual 32-bit timers, each with a different resolution and timing range.

The content of the 56-bit System Timer can be compared with the content of two compare values stored in the STM_CMP0 and STM_CMP1 registers. Interrupts can be generated on a compare match of the STM with the STM_CMP0 or STM_CMP1 registers.

The maximum clock period is $2^{56} \times f_{STM}$. At f_{STM} = 80 MHz, for example, the STM counts 28.56 years before overflowing. Thus, it is capable of timing the entire expected product life-time of a system without overflowing continuously.

Figure 3-12 shows an overview on the System Timer with the options for reading parts of the STM contents.

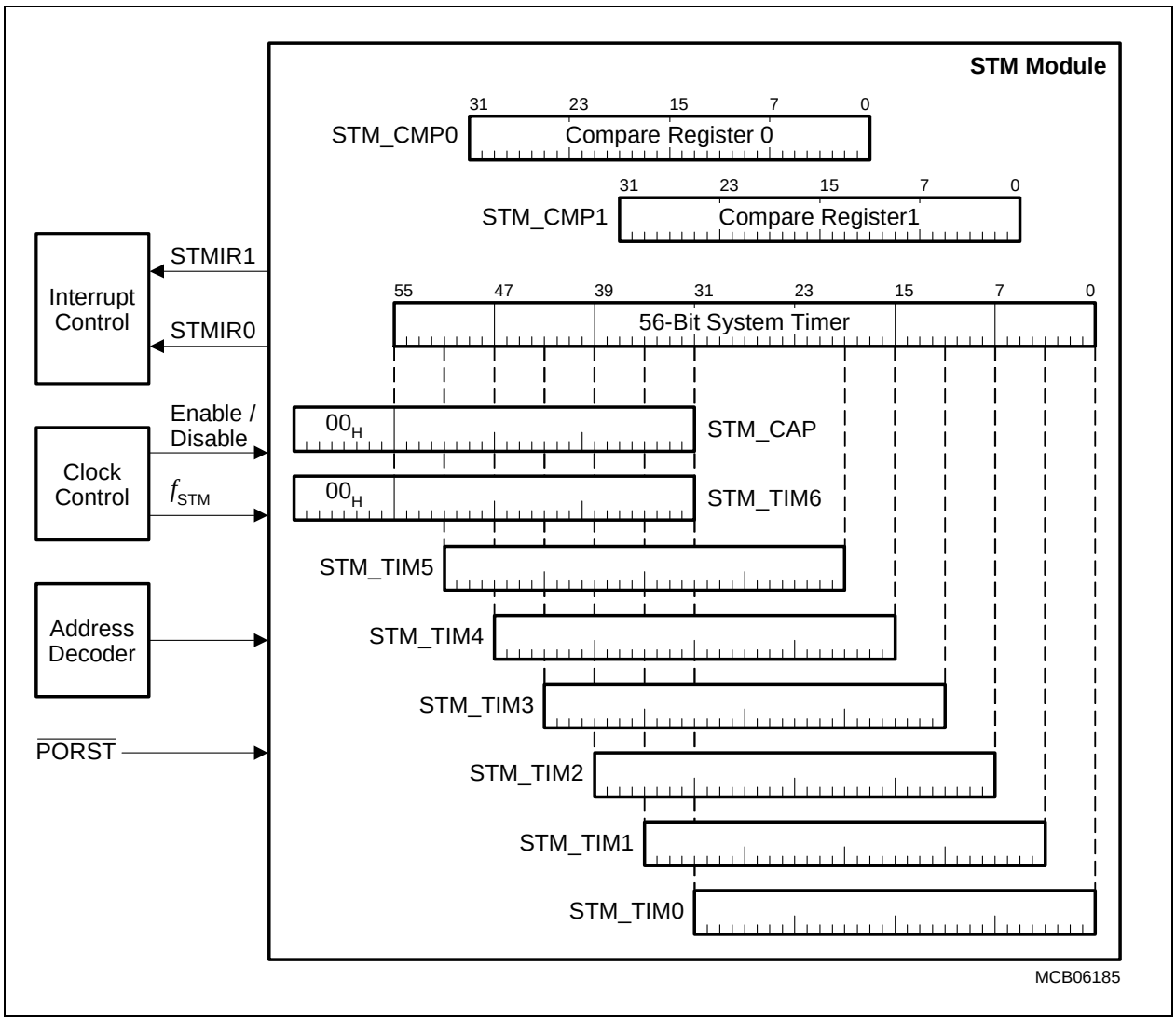

Figure 3-12 General Block Diagram of the STM Module Registers

3.19 Power Management System

The TC1762 power management system allows software to configure the various processing units so that they automatically adjust to draw the minimum necessary power for the application. There are three power management modes:

- Run Mode
- Idle Mode
- Sleep Mode

The operation of each system component in each of these states can be configured by software. The power-management modes provide flexible reduction of power consumption through a combination of techniques, including stopping the CPU clock, stopping the clocks of other system components individually, and individually clock-speed reduction of some peripheral components.

Besides these explicit software-controlled power-saving modes, special attention has been paid to automatic power-saving in those operating units which are not required at a certain point of time, or idle in the TC1762. In that case, they are shut off automatically until their operation is required again.

Table 3-3 describes the features of the power management modes.

Table 3-3 Power Management Mode Summary

Mode	Description
Run	The system is fully operational. All clocks and peripherals are enabled, as determined by software.
Idle	The CPU clock is disabled, waiting for a condition to return it to Run Mode. Idle Mode can be entered by software when the processor has no active tasks to perform. All peripherals remain powered and clocked. Processor memory is accessible to peripherals. A reset, Watchdog Timer event, a falling edge on the NMI pin, or any enabled interrupt event will return the system to Run Mode.
Sleep	The system clock signal is distributed only to those peripherals programmed to operate in Sleep Mode. The other peripheral module will be shut down by the suspend signal. Interrupts from operating peripherals, the Watchdog Timer, a falling edge on the NMI pin, or a reset event will return the system to Run Mode. Entering this state requires an orderly shut-down controlled by the Power Management State Machine.

In typical operation, Idle Mode and Sleep Mode may be entered and exited frequently during the run time of an application. For example, system software will typically cause the CPU to enter Idle Mode each time it has to wait for an interrupt before continuing its tasks. In Sleep Mode and Idle Mode, wake-up is performed automatically when any

4 Electrical Parameters

Chapter 4 provides the characteristics of the electrical parameters which are implementation-specific for the TC1762.

4.1 General Parameters

The general parameters are described here to aid the users in interpreting the parameters mainly in **Section 4.2** and **Section 4.3**. The absolute maximum ratings and its operating conditions are provided for the appropriate setting in the TC1762.

4.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the TC1762 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics which are a distinctive feature of the TC1762 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements which must provided by the microcontroller system in which the TC1762 designed in.

4.1.2 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in **Section 4.2.1**.

Table 4-1 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub Class	Speed Grade	Load	Leakage[1)]	Termination
A	3.3V	LVTTL I/O, LVTTL outputs	**A1** (e.g. GPIO)	6 MHz	100 pF	500 nA	No
			A2 (e.g. serial I/Os)	40 MHz	50 pF	6 µA	Series termination recommended
			A3 (e.g. BRKIN, BRKOUT)	66 or 80 MHz[2)]	50 pF	6 µA	Series termination recommended (for f > 25 MHz)
			A4 (e.g. Trace Clock)	66 or 80 MHz[2)]	25 pF	6 µA	Series termination recommended
C	3.3V	LVDS	–	50 MHz		–	Parallel termination[3)], 100Ω ± 10%
D	–	Analog inputs, reference voltage inputs					

1) Values are for T_{Jmax} = 150 °C.

2) This value corresponds to the operating frequency of the device, which depending on the derivative, can be 66 or 80 MHz.

3) In applications where the LVDS pins are not used (disabled), these pins must be either left unconnected, or properly terminated with the differential parallel termination of 100Ω ± 10%.

4.2.2 Analog to Digital Converter (ADC0)

Table 4-6 provides the characteristics of the ADC module in the TC1762.

Table 4-6 ADC Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions / Remarks
			Min.	Typ.	Max.		
Analog supply voltage	V_{DDM}	SR	3.13	3.3	3.47[1)]	V	–
	V_{DD}	SR	1.42	1.5	1.58[2)]	V	Power supply for ADC digital part, internal supply
Analog ground voltage	V_{SSM}	SR	-0.1	–	0.1	V	–
Analog reference voltage [17)]	V_{AREFx}	SR	V_{AGNDx}+ 1V	V_{DDM}	V_{DDM}+ 0.05[1)] [3)4)]	V	–
Analog reference ground [17)]	V_{AGNDx}	SR	V_{SSMx} - 0.05V	0	V_{AREF} - 1 V	V	–
Analog reference voltage range[5)17)]	V_{AREFx}- V_{AGNDx}	SR	V_{DDM}/2		V_{DDM} + 0.05		
Analog input voltage range	V_{AIN}	SR	V_{AGNDx}	–	V_{AREFx}	V	–
V_{DDM} supply current	I_{DDM}	SR		2.5	4	mA rms	[6)]
Power-up calibration time	t_{PUC}	CC	–	–	3840	f_{ADC} CLK	–
Internal ADC clocks	f_{BC}	CC	2	–	40	MHz	$f_{BC} = f_{ANA} \times 4$
	f_{ANA}	CC	0.5	–	10	MHz	$f_{ANA} = f_{BC} / 4$
Sample time	t_S	CC	4 × (CHCONn.STC + 2) × t_{BC}			µs	–
			8 × t_{BC}	–	–	µs	

15) I_{AREF_MAX} is valid for the minimum specified conversion time. The current flowing during an ADC conversion with a duration of up to t_C = 25µs can be calculated with the formula $I_{AREF\_MAX} = Q_{CONV}/t_C$. Every conversion needs a total charge of Q_{CONV} = 150pC from V_{AREF}.
All ADC conversions with a duration longer than t_C = 25µs consume an I_{AREF_MAX} = 6µA.

16) For the definition of the parameters see also **Figure 4-2**.

17) Applies to AIN0 and AIN1, when used as auxiliary reference inputs.

18) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead of this smaller capacitances are successively switched to the reference voltage.

19) The sampling capacity of the conversion C-Network is pre-charged to V_{AREF}/2 before the sampling moment. Because of the parasitic elements the voltage measured at AINx is lower then V_{AREF}/2.

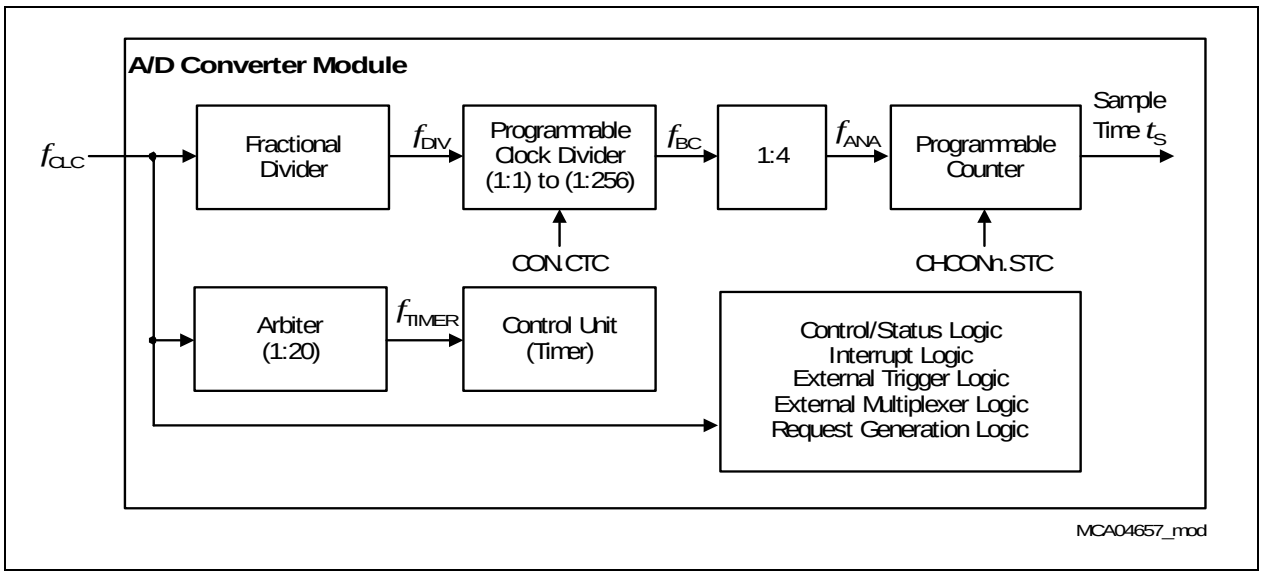

Figure 4-1 ADC0 Clock Circuit

4.2.4 Oscillator Pins

Table 4-8 provides the characteristics of the oscillator pins in the TC1762.

Table 4-8 Oscillator Pins Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit values		Unit	Test Conditions
			Min.	Max.		
Frequency Range	f_{OSC}	CC	4	25	MHz	–
Input low voltage at XTAL1[1)]	V_{ILX}	SR	-0.2	0.3 × V_{DDOSC3}	V	–
Input high voltage at XTAL1[1)]	V_{IHX}	SR	0.7 × V_{DDOSC3}	V_{DDOSC3} + 0.2	V	–
Input current at XTAL1	I_{IX1}	CC	–	±25	µA	0 V < V_{IN} < V_{DDOSC3}

1) If the XTAL1 pin is driven by a crystal, reaching a minimum amplitude (peak-to-peak) of 0.3 × V_{DDOSC3} is necessary.

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.

4.3.2 Output Rise/Fall Times

Table 4-11 provides the characteristics of the output rise/fall times in the TC1762.

Table 4-11 Output Rise/Fall Times (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Class A1 Pads					
Rise/fall times[1)] Class A1 pads	t_{RA1}, t_{FA1}		50 140 18000 150 550 65000	ns	Regular (medium) driver, 50 pF Regular (medium) driver, 150 pF Regular (medium) driver, 20 nF Weak driver, 20 pF Weak driver, 150 pF Weak driver, 20 000 pF
Class A2 Pads					
Rise/fall times [1)] Class A2 pads	t_{FA2}, t_{FA2}		3.3 6 5.5 16 50 140 18000 150 550 65000	ns	Strong driver, sharp edge, 50 pF Strong driver, sharp edge, 100pF Strong driver, med. edge, 50 pF Strong driver, soft edge, 50 pF Medium driver, 50 pF Medium driver, 150 pF Medium driver, 20 000 pF Weak driver, 20 pF Weak driver, 150 pF Weak driver, 20 000 pF
Class A3 Pads					
Rise/fall times [1)] Class A3 pads	t_{FA3}, t_{FA3}		2.5	ns	50 pF
Class A4 Pads					
Rise/fall times [1)] Class A4 pads	t_{FA4}, t_{FA4}		2.0	ns	25 pF
Class C Pads					
Rise/fall times Class C pads	t_{rC}, t_{fC}		2	ns	

1) Not all parameters are subject to production test, but verified by design/characterization and test correlation.

Table 4-16 JTAG Timing Parameter[1)]

Parameter	Symbol		Limit Values		Unit	Test Conditions / Remarks
			Min.	Max.		
TMS setup to TCK	t_1	SR	6.0	–	ns	–
TMS hold to TCK	t_2	SR	6.0	–	ns	–
TDI setup to TCK	t_1	SR	6.0	–	ns	–
TDI hold to TCK	t_2	SR	6.0	–	ns	–
TDO valid output from TCK[2)]	t_3	CC	–	14.5	ns	C_L = 50 pF[3)4)]
			3.0	–		C_L = 20 pF
TDO high impedance to valid output from TCK[2)]	t_4	CC	–	15.5	ns	C_L = 50 pF[3)4)]
TDO valid output to high impedance from TCK[2)]	t_5	CC	–	14.5	ns	C_L = 50 pF[4)]

1) Not subject to production test, verified by design / characterization.

2) The falling edge on TCK is used to capture the TDO timing.

3) By reducing the load from 50 pF to 20 pF, a reduction of approximately 1.0 ns in timing is expected.

4) By reducing the power supply range from +/-5 % to +5/-2 %, a reduction of approximately 0.5 ns in timing is expected.

5.3 Flash Memory Parameters

The data retention time of the TC1762's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Table 5-2 Flash Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Program Flash Retention Time, Physical Sector[1) 2)]	t_{RET}	20	–	years	Max. 1000 erase/program cycles
Program Flash Retention Time, Logical Sector[1)2)]	t_{RETL}	20	–	years	Max. 50 erase/program cycles
Data Flash Endurance (32 Kbyte)	N_E	15 000	–	–	Max. data retention time 5 years
Data Flash Endurance, EEPROM Emulation (8 × 4 Kbyte)	N_{E8}	120 000	–	–	Max. data retention time 5 years
Programming Time per Page[3)]	t_{PR}	–	5	ms	–
Program Flash Erase Time per 256-Kbyte sector	t_{ERP}	–	5	s	f_{CPU} = 80 MHz
Data Flash Erase Time per 16-Kbyte sector	t_{ERD}	–	0.625	s	f_{CPU} = 80 MHz
Wake-up time	t_{WU}	$4300 \times 1/f_{CPU}$ + 40µs			

1) Storage and inactive time included.

2) At average weighted junction temperature T_J = 100 °C, or
the retention time at average weighted temperature of T_J = 110 °C is minimum 10 years, or
the retention time at average weighted temperature of T_J = 150 °C is minimum 0.7 years.

3) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes additional 5ms.