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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Network Processor
Core Processor	4Kc
Program Memory Type	-
Controller Series	-
RAM Size	16K x 8
Interface	Ethernet, UART, USB
Number of I/O	-
Voltage - Supply	1.8V, 3.3V
Operating Temperature	-
Mounting Type	Surface Mount
Package / Case	208-BFQFP Exposed Pad
Supplier Device Package	P-FQFP-208-10
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=adm5120px-ab-t-2

Bus Interface Auxillary Port Input

Returns the confirmation that the SIF was flushed.

BIU_AUXI	Offset	Reset Value
BIU Auxillary Port Input Register	0200_H	$0000\ 0000_H$

Field	Bits	Type	Description
ACK	0	r	**SIF Flush ACK** Returns the acknlowdgement that the SIF was flushed. 0_B **No action** 1_B **Flushed** SIF was flushed.

Bus Interface Unit Auxillary Port Output

Used to configure the basic parameters of the BIU.

BIU_AUXO	Offset	Reset Value
BIU Auxillary Port Output Register	0208_H	$0000\ 0000_H$

Field	Bits	Type	Description
max_read_ws	15:8	rw	**Read WS** define number of waitstates for read
Sus	4	rw	**OCDS suspend** should written with 0
Ndt	3	rw	**delayed transaction** should written with 1
Ewa	2	rw	**early_wr_abotr_sup** should written with 0
Era	1	rw	**early_rd_abort_sup** should written with 0
SFR	0	rw	**SIF Flush request** request flush operation from SIF module

4.3.2 FPI Bus Register Description

Absolute Register Address = Module Base Address + Offset Address

5 MultiPort Memory Controller (MPMC)

The MultiPort Memory Controller (MPMC) description covers:

- Feature list (**Chapter 5.1**)
- Functional description (**Chapter 5.2**)
- External Interface; described in the dedicated chapter of the different interfaces
- Registers (**Chapter 5.3**)

5.1 Feature List

The MPMC offers the following features:

- Dynamic memory interface support including SDRAM, JEDEC low-power SDRAM
- Asynchronous static memory device support including SRAM, ROM and NOR Flash with or without asynchronous page mode
- Read and write buffers to reduce latency and to improve performance
- 8-bit, 16-bit and 32-bit wide static memory support
- Static memory features include:
  - Programmable wait states
  - Output enable, and write enable delays
  - Extended wait
  - Bus turnaround delay
  - Asynchronous page mode read
- Controller supports 2K, 4K and 8K row address synchronous memory parts. That is typical 512M, 256M, 128M and 16MB parts with 8, 16 or 32DQ bits per device.

5.2 Functional Description

The following describes the MPMC's functions

5.2.1 Static Memory Controller

Static memory descriptions:

5.2.1.1 Extended Wait Transfers

The static memory controller supports extremely long transfer times. In normal use the memory transfers are timed using the **MPMC Static Wait Rd 1** and **MPMC Static Wait Wr 1** registers. These registers enable transfers with up to 32 wait states. However, if an extremely slow static memory device has to be accessed you can enable the Extended Wait(EW) bit in register . When this bit is enabled the **MPMC Static Extended Wait** register is used to time both the read and write transfers. This register enables transfers to have up to 16368 wait states.

5.2.1.2 Wait State Generation

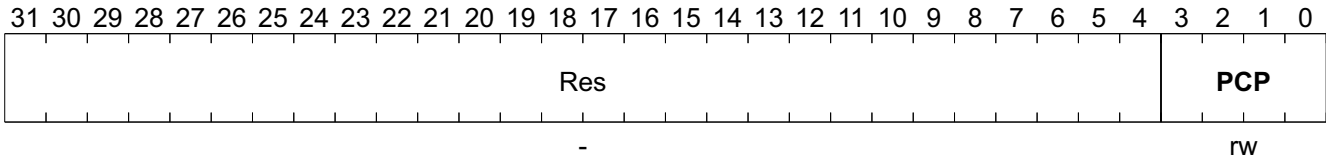
Each bank of the MPMC must be configured for external transfer wait states in read and write accesses. This is achieved by programming the appropriate fields of the bank control registers:

- **MPMC Static Wait Wen 1**
- **MPMC Static Wait Oen 1**
- **MPMC Static Wait Rd 1**
- **MPMC Static Wait Wr 1**
- **MPMC Static Wait Page 1**
- **MPMC Static Wait Turn 1**
- **MPMC Static Extended Wait**

MPMC Dynamic RP

Note: The delay is in MPMCCLK cycles.

MPMC_DRP	Offset	Reset Value
MPMC Dynamic RP	030_H	F_H

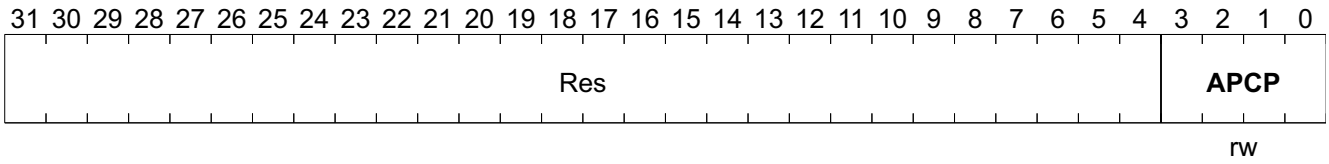


Field	Bits	Type	Description
Res	31:4	-	**Reserved** Read undefined. Must be written as zeros.
PCP	3:0	rw	**Precharge Command Period** 0_H 1 clock cycle ...H F_H 16 clock cycles (reset value on nPOR)

MPMC Dynamic RAS

Note: The delay is in MPMCCLK cycles.

MPMC_DRAS	Offset	Reset Value
MPMC Dynamic RAS	034_H	F_H



Field	Bits	Type	Description
Res	31:4		**Reserved** Read undefined. Must be written as zeros.
APCP	3:0	rw	**Active to Precharge Command Period** 0_H 1 clock cycle ...H F_H 16 clock cycles (reset value on nPOR)

MPMC Dynamic SREX

Note: The delay is in MPMCCLK cycles.

Table 30 Address Mapping Table

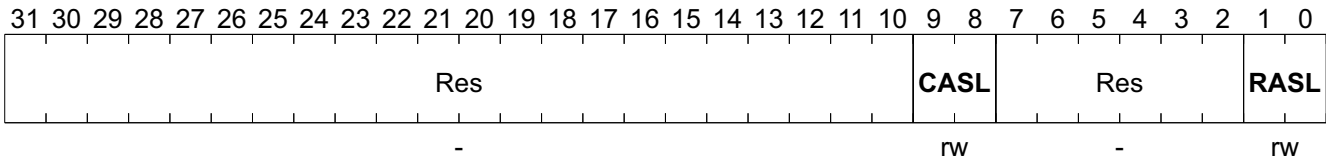
[14]	[12]	[11:9]	[8:7]	Description
0	1	010	01	128MB (8M X 16), 4 banks, row length=12, column length=9
0	1	011	00	256MB (32M X 8), 4 banks, row length=13, column length=10
0	1	011	01	256MB (16M X 16), 4 banks, row length=13, column length=9
0	1	100	00	512MB (64M X 8), 4 banks, row length=13, column length=11
0	1	100	01	512MB (32M X 16), 4 banks, row length=13, column length=10
32-Bit external bus High-Performance address mapping (Row, Bank, Column)				
1	0	000	00	16MB (2M X 8), 2 banks, row length=11, column length=9
1	0	000	01	16MB (1M X 16), 2 banks, row length=11, column length=8
1	0	001	00	64MB (8M X 8), 4 banks, row length=12, column length=9
1	0	001	01	64MB (4M X 16), 4 banks, row length=12, column length=8
1	0	001	10	64MB (2M X 32), 4 banks, row length=11, column length=8
1	0	010	00	128MB (16M X 8),4 banks, row length=12, column length=10
1	0	010	01	128MB (8M X 16), 4 banks, row length=12, column length=9
1	0	010	10	128MB (4M X 32), 4 banks, row length=12, column length=8
1	0	011	00	256MB (32M X 8), 4 banks, row length=13, column length=10
1	0	011	01	256MB (16M X 16), 4 banks, row length13, column length=9
1	0	011	10	256MB (8M X 32), 4 banks, row length=13, column length=8
1	0	100	00	512MB (64M X8),4 banks, row length=13, column length=11
1	0	100	01	512MB (32M X 16),4 banks, row length=13, column length=10
32-Bit external bus Low-Performance SDRAM mapping (Bank,Row, Column)				
1	0	100	01	512MB (32M X 16),4 banks, row length=13, column length=10
1	1	000	00	16MB (2M X 8), 2 banks, row length=11, column length=9
1	1	000	01	16MB (1M X 16), 2 banks, row length=11, column length=8
1	1	001	00	64MB (8M X 8), 4 banks, row length=12, column length=9
1	1	001	01	64MB (4M X 16), 4 banks, row length=12, column length=8
1	1	001	10	64MB (2M X 32), 4 banks, row length=11, column length=8
1	1	010	00	128MB (16M X 8),4 banks, row length=12, column length=10
1	1	010	01	128MB (8M X 16), 4 banks, row length=12, column length=9
1	1	010	10	128MB (4M X 32), 4 banks, row length=12, column length=8
1	1	011	00	256MB (32M X 8), 4 banks, row length=13, column length=10
1	1	011	01	256MB (16M X 16), 4 banks, row length13, column length=9
1	1	011	10	256MB (8M X 32), 4 banks, row length=13, column length=8
1	1	100	00	512MB (64M X8),4 banks, row length=13, column length=11
1	1	100	01	512MB (32M X 16),4 banks, row length=13, column length=10

MPMC Dynamic Ras Cas 1

Notes

1. *The RAS to CAS latency (RAS) and CAS latency (CAS) are both defined in MPMCCLK cycles.*
2. *The offset 104_H and 124_H is for SDRAM bank0 and bank1 respectively.*

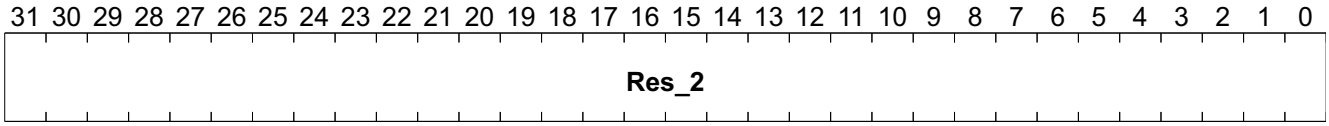
MPMC_DRC1	Offset	Reset Value
MPMC Dynamic Ras Cas 1	124_H	303_H



Field	Bits	Type	Description
Res	31:10	-	**Reserved**
CASL	9:8	rw	**CAS Latency** 00_B Reserved 01_B One clock cycle(a) 10_B Two clock cycles 11_B Three clock cycles(reset value on nPOR).
Res	7:2	-	**Reserved**
RASL	1:0	rw	**RAS Latency** Active to read or write delay 00_B Reserved 01_B One clock cycle(a) 10_B Two clock cycles 11_B Three clock cycles (reset value on nPOR).

Reserved 2

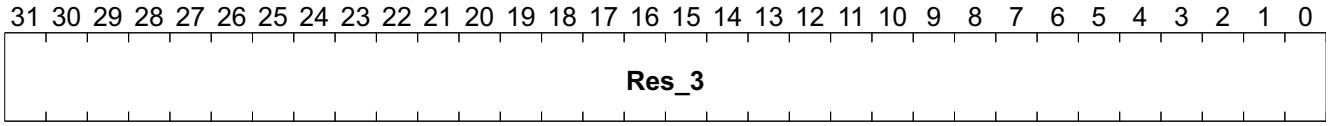
Res_2	Offset	Reset Value
Reserved 2	38_H	0_H



Field	Bits	Type	Description
Res_2	31:0		**Reserved** Not Applicable.

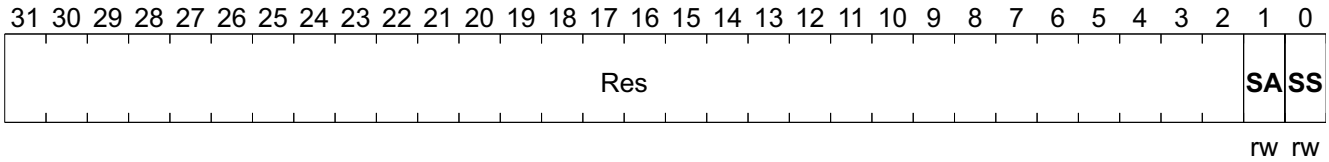
Reserved 3

Res_3	Offset	Reset Value
Reserved 3	$3C_H$	0_H



Field	Bits	Type	Description
Res_3	31:0		**Reserved** Not Applicable.

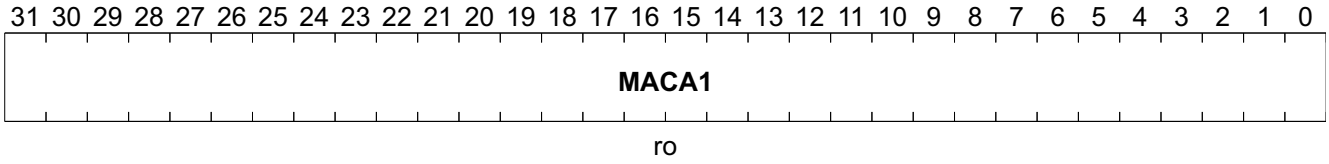
Srch_cmd	Offset	Reset Value
Search CMD	$4C_H$	0_H



Field	Bits	Type	Description
Res	31:2		**Reserved** Not Applicable.
SA	1	rw	**Search Again** Search for the next available address, self_clear (program again after data_rdy).
SS	0	rw	**Search Start** Searching from the start of address table, self_clear.

ADDR St1

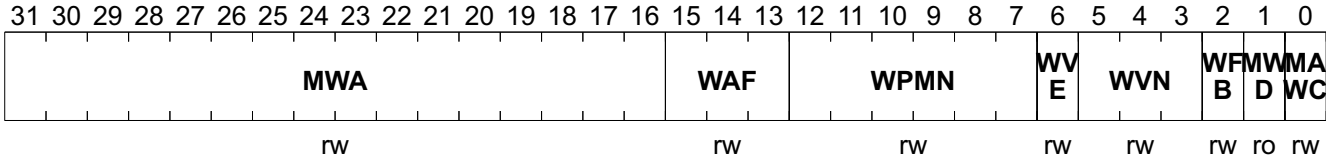
ADDR_st1	Offset	Reset Value
Address St1	54_H	0_H



Field	Bits	Type	Description
MACA1	31:0	ro	**MAC Address 47:16**

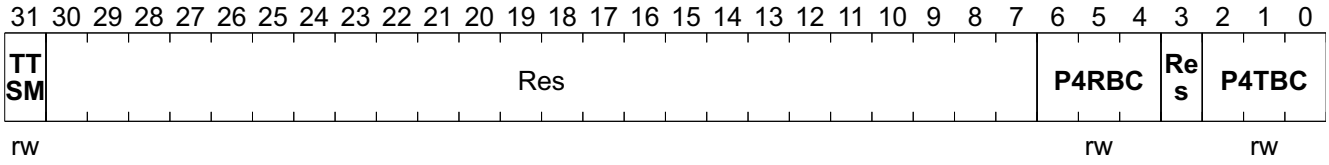
MAC Write Address 0

MAC_wt0	Offset	Reset Value
MAC Write Address 0	58_H	0_H



Field	Bits	Type	Description
MWA	31:16	rw	**MAC Write Address 15:0**
WAF	15:13	rw	**Write Age Field** 000_B Empty 001 to 110_B Existed MAC 111_B Static address
WPMN	12:7	rw	**Write Port Map Number**
WVE	6	rw	**Write VLAN Enable**
WVN	5:3	rw	**Write VLAN Number**
WFB	2	rw	**Write Filter Bit**
MWD	1	ro	**MAC Write Done** 1_B MAC address write complete, read_clear
MAWC	0	rw	**MAC Address Write Command** 1_B The MAC write data is ready and write toMAC table, self_clear

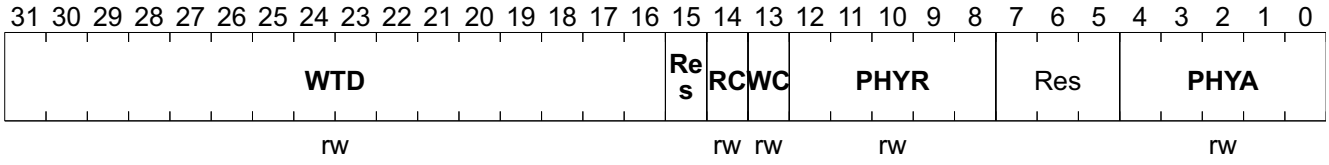
MAC Write Address 1



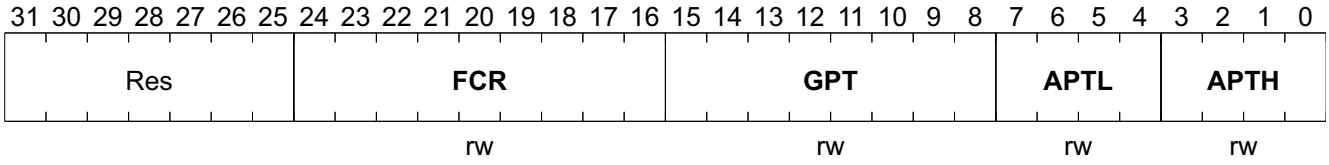
Field	Bits	Type	Description
TTSM	31	rw	**The Transmit Traffic Shaper Mode** 0_B Best effort mode (default) 1_B Average Inter Packet Gap (IPG) in the 1 second period
Res	30:7		**Reserved** Not Applicable.
P4RBC	6:4	rw	**Port 4 Receive Bandwidth Control** Please refer to **P3RBC** for bandwidth define.
Res	3		**Reserved** Not Applicable.
P4TBC	2:0	rw	**Port 4 Transmit Bandwidth Control** Please refer to **P3RBC** for bandwidth define.

PHY Control 0

PHY_cntl0	Offset	Reset Value
PHY Control 0	68_H	0_H



Field	Bits	Type	Description
WTD	31:16	rw	**The Data be Written into the PHY**
Res	15		**Reserved** Not Applicable.
RC	14	rw	**Read Command, self_clear**
WC	13		**Write Command, self_clear**
PHYR	12:8		**PHY Register Address**
Res	7:5		**Reserved** Not Applicable.
PHYA	4:0	rw	**PHY Address**



Field	Bits	Type	Description
Res	31:25		**Reserved** Not Applicable.
FCR	24:16	rw	**Switch Flow Control Release Threshold, 268 Free Blocks**
GPT	15:8	rw	**Giga Port Buffer Threshold, 32 Occupied Blocks**
APTL	7:4	rw	**Per Port Guaranteed High Priority pkt, 3 Blocks**
APTH	3:0		**Per Port Guaranteed Normal Priority pkt, 3 Blocks**

Field	Bits	Type	Description
RMAE	30	rw	**Recommend MCC Average Enable** Per port PHY auto MDIX enable. 0_B Default value
AMDIX	29:25		**Auto MDIX enable** *Note: [25] = port0, [26] = port 1 etc…* 0_B disable auto MDIX. 1_B enable auto MDIX. (default)
PHYR	24:20		**PHY Reset** *Note: [20] = port0, [21] = port 1 etc…* 0_B Reset(default) 1_B Normal
RFCV	19:15		**Recommended FC Value (reg4, bit10)** *Note: [15] = port0, [16] = port 1 etc…* 0_B No forced 1_B FC_rec ON
DC	14:10		**Duplex Control** *Note: [10] = port0, [11] = port 1 etc…* 0_B Half 1_B Full
SC	9:5		**Speed Control** *Note: [5] = port0, [6] = port 1 etc…* 0_B 10M 1_B 100M
ANE	4:0		**Auto Negotiation Enable** *Note: [0] = port0, [1] = port 1 etc…* 1_B Enable

PHY Control 3

PHY_cntl3	Offset	Reset Value
PHY Control 3	80_H	$1420B_H$

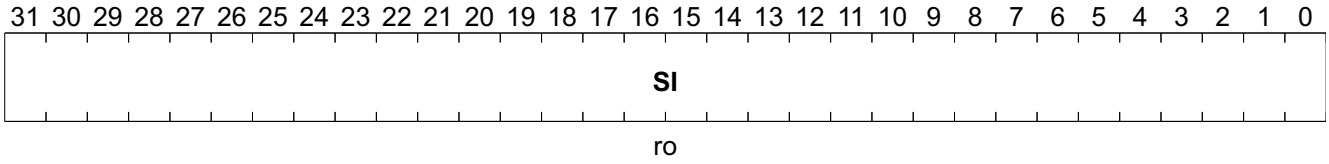
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res											FXE				DFE*	CBDE	RPIC	RPLFT		RFGL	RNT	RTJD	RRJE	RAPD	IIN*	RSHC		PFRV		RBLL		
											rw				rw	rw	rw	rw		rw	rw	rw	rw	rw	rw	rw		rw		rw		

Field	Bits	Type	Description
Res	31:22		**Reserved** Not Applicable.

Field	Bits	Type	Description
Res	31:24		**Reserved** Not Applicable.
OC	23:16	rw	**Offset Count from SA 7:0** This offset defines that the data will be extracted from the packets. The data will be compared with the Custom Field and Mask. The offset is counted from SA0 field of packet. If VLAN type found, it will add 4-byte automatically.
MCF	15:8		**Mask of Custom Field** The mask data for the Custom Field.
CFD	7:0		**Custom Field Define** This data defines the Custom Field that will be treated as higher priority or filtered.

Port Controller

Port_cnt	Offset	Reset Value
Port Controller	AC_H	0_H

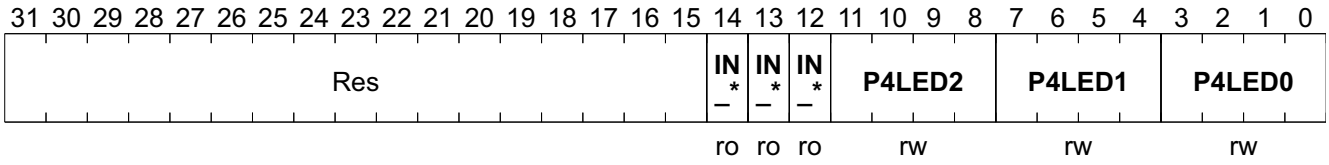


Field	Bits	Type	Description
SI	31:0	ro	**Sel Info** If port_sel=0, [24:16] port0 high packet count [8:0] port0 low packet count If port_sel=1, [24:16] port1 high packet count [8:0] port1 low packet count If port_sel=2, [24:16] port2 high packet count [8:0] port2 low packet count If port_sel=3, [24:16] port3 high packet count [8:0] port3 low packet count If port_sel=4, [24:16] port4 high packet count [8:0] port4 low packet count If port_sel=5, [24:16] port5 high packet count [8:0] port5 low packet count If port_sel=6, [24:16] port6 high packet count [8:0] port6 low packet count If port_sel=7, [24:16] port7 high packet count [8:0] port7 low packet count If port_sel=9, [8:0] flow control status If port_sel=10, [24:16] testing [8:0] ever flow control port If port_sel=11, [24:16] no_pkt status [7:0] no_pkt_status If port_sel=12, [24:16] receive bandwidth control port, [8:0] transmit bandwidth control port

port4_LED

Note: Port4 LED[2:0] pin (141,142,143) configuration register.

port4_LED	Offset	Reset Value
Port 4 LED	110_H	$A59_H$



Field	Bits	Type	Description
Res	31:15		**Reserved** Not Applicable.
IN_P4LED2	14	ro	**Input in Port 4 LED2** Input value at pin Port 4 LED2 when it is configured to GPIO_in mode
IN_P4LED1	13	ro	**Input in Port 4 LED1** Input value at pin Port 4 LED1 when it is configured to GPIO_in mode
IN_P4LED0	12	ro	**Input in Port 4 LED0** Input value at pin Port 4 LED0 when it is configured to GPIO_in mode
P4LED2	11:8	rw	**Port 4 LED2 State** Refer to the definition in **P0LED2** except the default value. 1010_B Default value, duplex/col
P4LED1	7:4		**Port 4 LED1 State** Refer to the definition in **P0LED2** except the default value. 0101_B Default value, speed
P4LED0	3:0		**Port 4 LED0 State** Refer to the definition in **P0LED2** except the default value. 1001_B Default value, link/activity

UART Receive Status Register/Error Clear

UARTRRS_ECR	Offset	Reset Value
UART Receive Status Register/Error Clear	04_H	0_H

7	6	5	4	3	2	1	0
RSR	Res			**OE**	**BE**	**PE**	**FE**
w	r			r	r	r	r

Field	Bits	Type	Description
RSR	7	w	**RSR** A write to this register clears the framing, parity, break and overrun errors. The data value is not important.
Res	6:4	r	**Reserved** Not applicable.
OE	3		**Overrun Error** This bit is set to 1 if data is received and the FIFO is already full.
BE	2		**Break Error** This bit is set to 1 if a break condition was detected, indicating that the received data input was held LOW for longer than a full-word transmission time.
PE	1		**Parity Error** When this bit is set to 1, it indicates that the parity of received data character does pot match the parity selected in UARTLCR_H (bit 2)
FE	0		**Framing Error** When this bit is set to 1, it indicates that the received character did not have a valid stop bit.

UART Line Control Register, High Byte

UARTLCR_H	Offset	Reset Value
UART Line Control Register, High Byte	08_H	0_H

7	6	5	4	3	2	1	0
Res	**WLEN**		**FEN**	**STP2**	**EPS**	**PEN**	**BRK**
	rw		rw	rw	rw	rw	rw

Field	Bits	Type	Description
Res	7		**Reserved** Not applicable

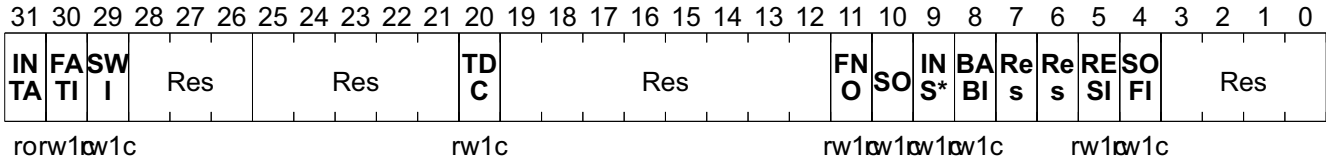
Field	Bits	Type	Description
CC	30:27		**Complete Code** The transfer status of each USB transfer. 0000_B No Error 0001_B CRC Check Error 0010_B Bit-Stuffing Error 0011_B Data Toggle Error 0100_B STALL 0101_B Device No Response (Timeout) 0110_B PID Error (Invalid PID) 0111_B Unexpected PID 1000_B Data Overrun (Packet Overrun) 1001_B Data Underrun (Packet Underrrun) 1100_B Buffer Overrun 1101_B Buffer Underrrun
EC	26:25		**Error Count** Error count the error that happens at each USB transfer.
DTB	24:23		**Data Toggle Bit** This field is used for data PID value. When 1, use but 23 as the toggle bit. 24_B When 0, use togglecarry bit in ED as the PID 23_B Toggle value
DIR	22:21		**Direction** These bits indicate this packet's direction. 00_B Setup packet 01_B Out packet 10_B IN packet 11_B **Res** Reserved
Res	20:14		**Reserved**
ISI	13:8		**Interrrupt Service Interval** This field indicates the frame interval where the interrupt transaction occurs. The frame interval = bit [13:8] + 1
Res	7:6		**Reserved**
FN	5:0		**Frame Number** This field indicates the frame number that receive/transmit this data, this field is only valid when configured in Isochronous and interrupt transaction. For Isochronous transaction, it indicates the frame number in which the isochronous transaction should occur. For interrupt transaction, software uses this field to indicate to hardware for the "starting frame number" of the interrupt transaction, hardware will update this field to the "next frame number" after the current transaction is done.

Data Buffer Pointer

Data_Buf_P	Offset	Reset Value
Data Buffer Pointer	$_H$	0_H

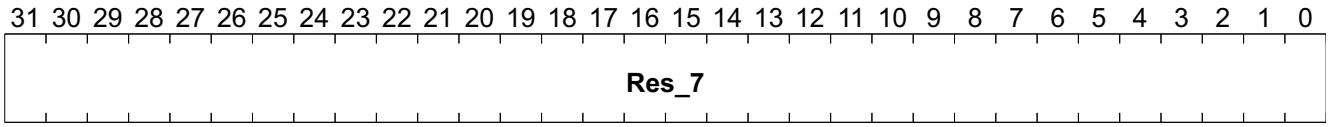
Interrupt Status

INT_S	Offset	Reset Value
Interrupt Status	04_H	0_H



Field	Bits	Type	Description
INTA	31	ro	**Interrupt Active** When this bit is set, it indicates that at least one unmasked interrupt status is set.
FATI	30	rw1c	**Fatal Interrupt, Device Mode** Reserved. Host mode: 1_B Fatal system bus error occurs
SWI	29		**Software Interrupt, Both Modes** 1_B Software Interrupt. This bit is set when software set one to SW_INT_REQ 00_H, and is cleared after software writes one to this bit.
Res	28:26		**Reserved** Not Applicable
Res	25:21		**Reserved** Not Applicable
TDC	20	rw1c	**A TD is Completed**
Res	19:12		**Reserved** Not Applicable
FNO	11	rw1c	**Frame Number Overflow** This bit is set when the MSB of the frame number changes.
SO	10		**Scheduling Overrun** This bit is set when USB schedules for current frame overruns.
INSMI	9		**Root Hub Status Change** 1_B Detected device insertion or remove. This bit will only be set for the device or hub, which is attached to host directly.
BABI	8		**Babble Detected, Host Mode** 1_B Detected babble
Res	7		**Reserved** Not Applicable
Res	6		**Reserved** Not Applicable

Res_7	Offset	Reset Value
Reserved 7	14_H	0_H



Field	Bits	Type	Description
Res_7	31:0		**Reserved** Not Applicable

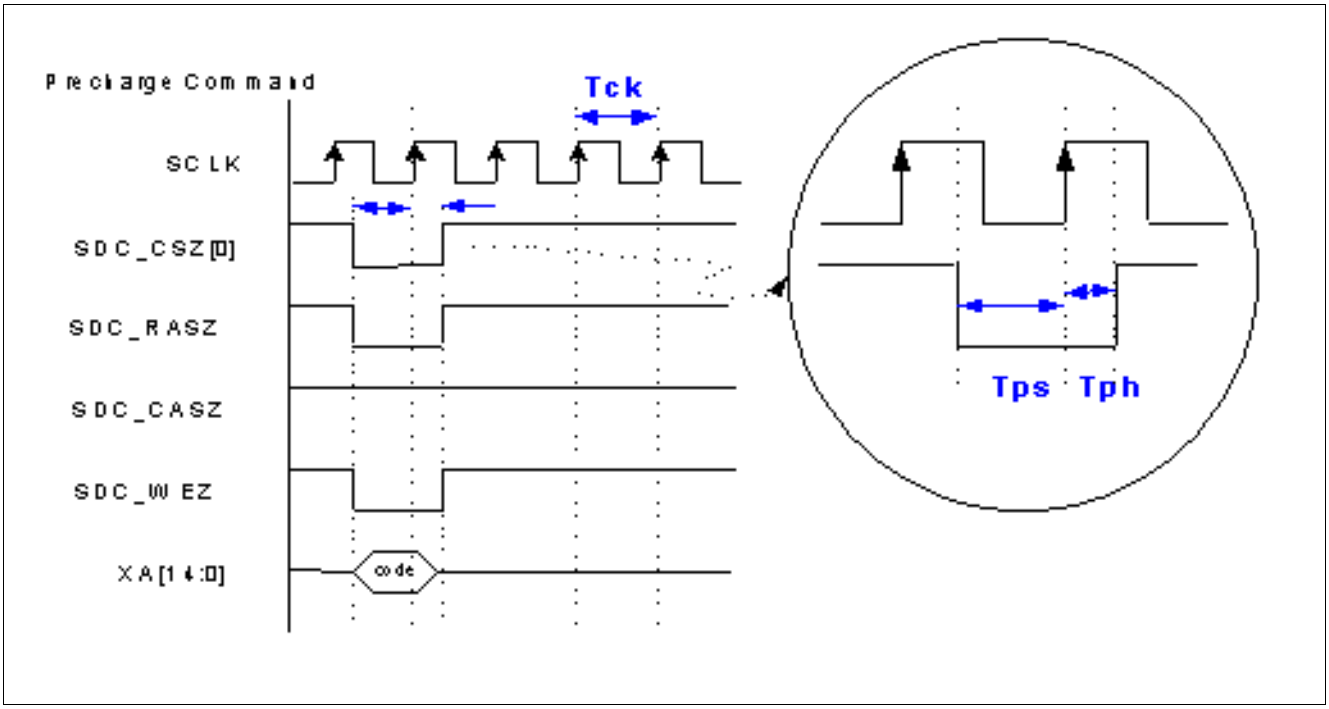


Figure 17 Precharge Command

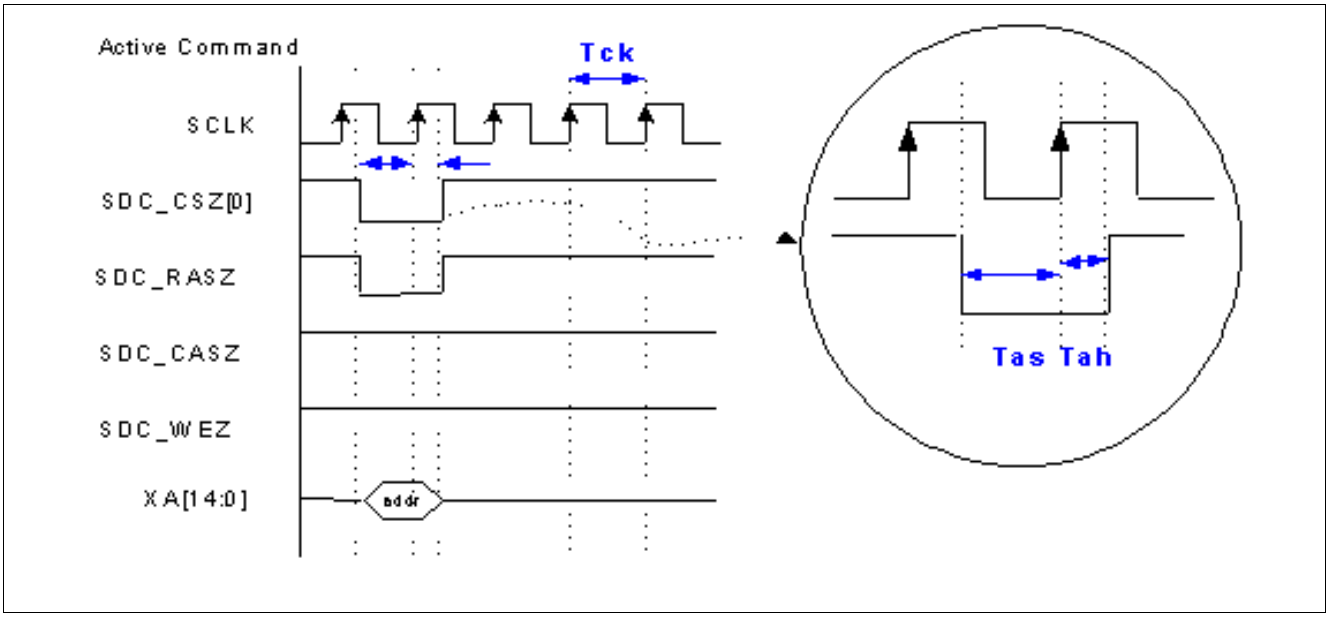


Figure 18 Active Command

VLAN	Virtual LAN
W	
WAN	Wide Area Networks