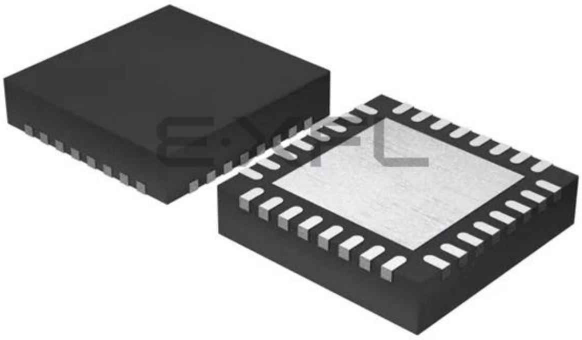
NXP USA Inc. - MKE02Z32VFM4 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LVD, PWM, WDT
Number of I/O	28
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x6b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount, Wettable Flank
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-HVQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mke02z32vfm4

- Timers
  - One 6-channel FlexTimer/PWM (FTM)
  - Two 2-channel FlexTimer/PWM (FTM)
  - One 2-channel periodic interrupt timer (PIT)
  - One real-time clock (RTC)
- Communication interfaces
  - Two SPI modules (SPI)
  - Up to three UART modules (UART)
  - One I2C module (I2C)
- Package options
  - 64-pin QFP/LQFP
  - 44-pin LQFP
  - 32-pin LQFP
  - 32-pin QFN

Table of Contents

Field	Description	Values
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• LC = 32 LQFP (7 mm x 7 mm) • FM = 32 QFN (5 mm x 5 mm) • LD = 44 LQFP (10 mm x 10 mm) • QH = 64 QFP (14 mm x 14 mm) • LH = 64 LQFP (10 mm x 10 mm)
CC	Maximum CPU frequency (MHz)	• 4 = 40 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

2.4 Example

This is an example part number:

MKE02Z64VQH4

3 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 1. Parameter classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
4. All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD}. PTA2 and PTA3 are true open drain I/O pins that are internally clamped to V_{SS}.
5. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger value.
6. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is higher than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as when no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Table 4. LVD and POR specification

Symbol	C	Description		Min	Typ	Max	Unit
V_{POR}	D	POR re-arm voltage[1]		1.5	1.75	2.0	V
V_{LVDH}	C	Falling low-voltage detect threshold—high range (LVDV = 1)[2]		4.2	4.3	4.4	V
V_{LVW1H}	C	Falling low-voltage warning threshold—high range	Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V
V_{LVW2H}	C		Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V_{LVW3H}	C		Level 3 falling (LVWV = 10)	4.6	4.6	4.7	V
V_{LVW4H}	C		Level 4 falling (LVWV = 11)	4.7	4.7	4.8	V
V_{HYSH}	C	High range low-voltage detect/warning hysteresis		—	100	—	mV
V_{LVDL}	C	Falling low-voltage detect threshold—low range (LVDV = 0)		2.56	2.61	2.66	V
V_{LVW1L}	C	Falling low-voltage warning threshold—low range	Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V
V_{LVW2L}	C		Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V
V_{LVW3L}	C		Level 3 falling (LVWV = 10)	2.82	2.9	2.98	V
V_{LVW4L}	C		Level 4 falling (LVWV = 11)	2.92	3.0	3.08	V
V_{HYSDL}	C	Low range low-voltage detect hysteresis		—	40	—	mV
V_{HYSWL}	C	Low range low-voltage warning hysteresis		—	80	—	mV
V_{BG}	P	Buffered bandgap output [3]		1.14	1.16	1.18	V

1. Maximum is highest voltage that POR is guaranteed.
2. Rising thresholds are falling threshold + hysteresis.
3. voltage Factory trimmed at V_{DD} = 5.0 V, Temp = 25 °C

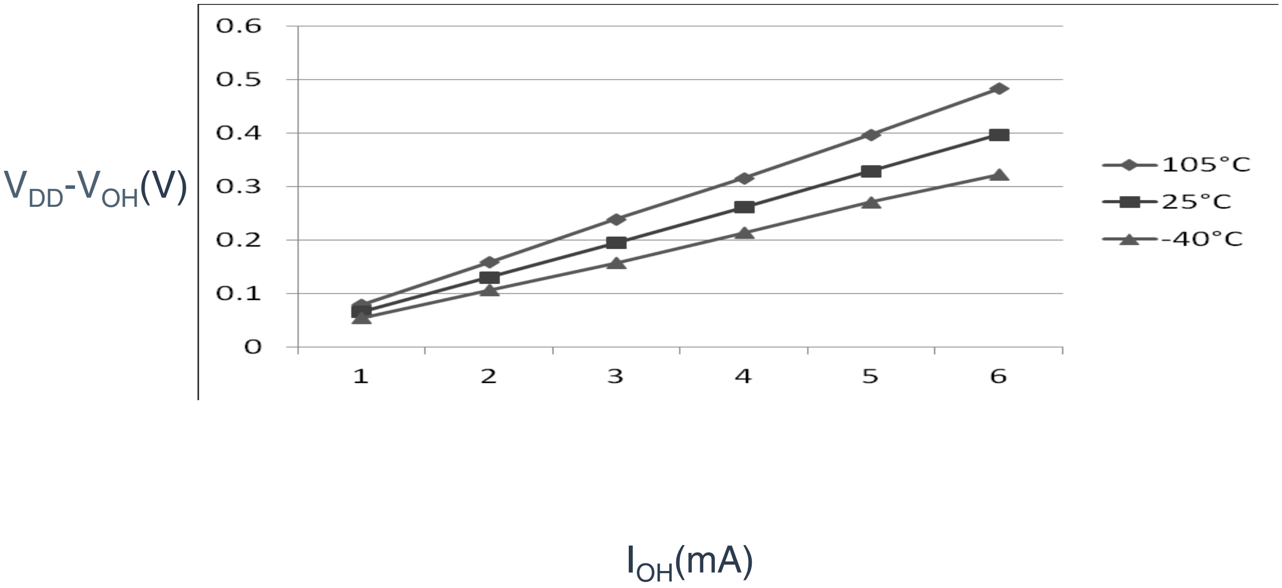


Figure 1. Typical V_{DD}-V_{OH} Vs. I_{OH} (standard drive strength) (V_{DD} = 5 V)

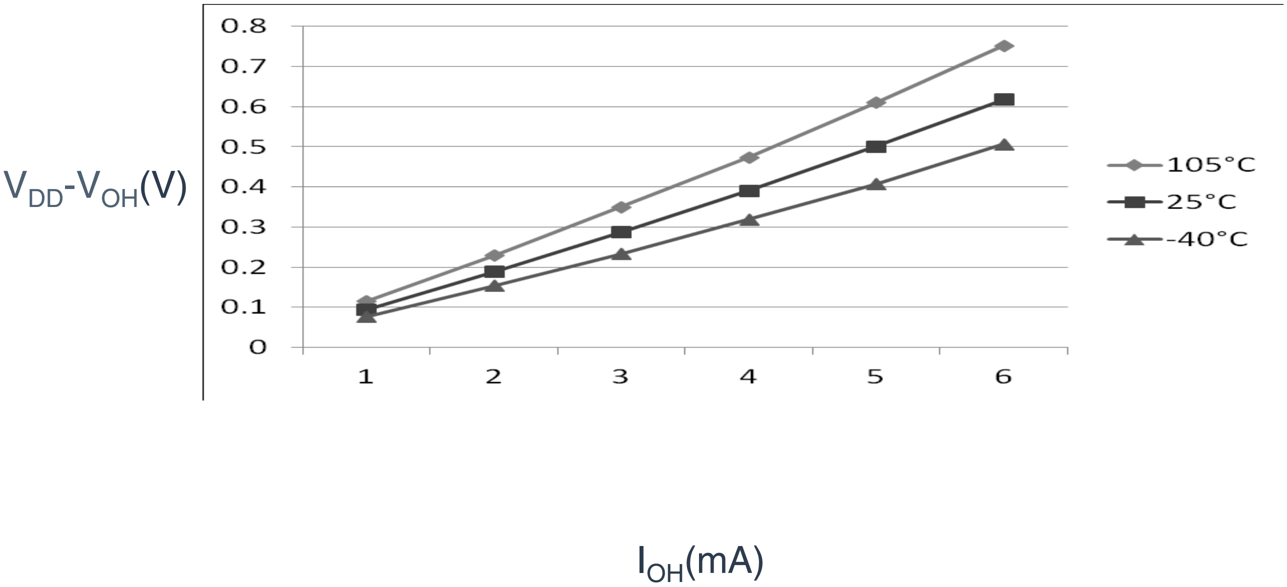


Figure 2. Typical V_{DD}-V_{OH} Vs. I_{OH} (standard drive strength) (V_{DD} = 3 V)

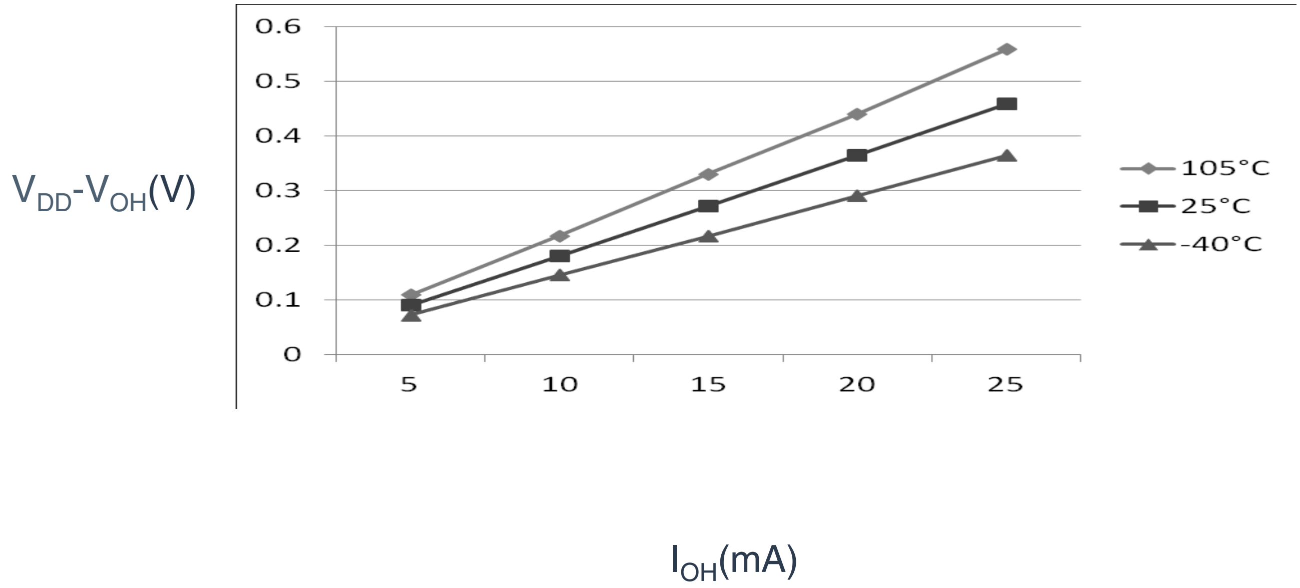


Figure 3. Typical V_{DD}-V_{OH} Vs. I_{OH} (high drive strength) (V_{DD} = 5 V)

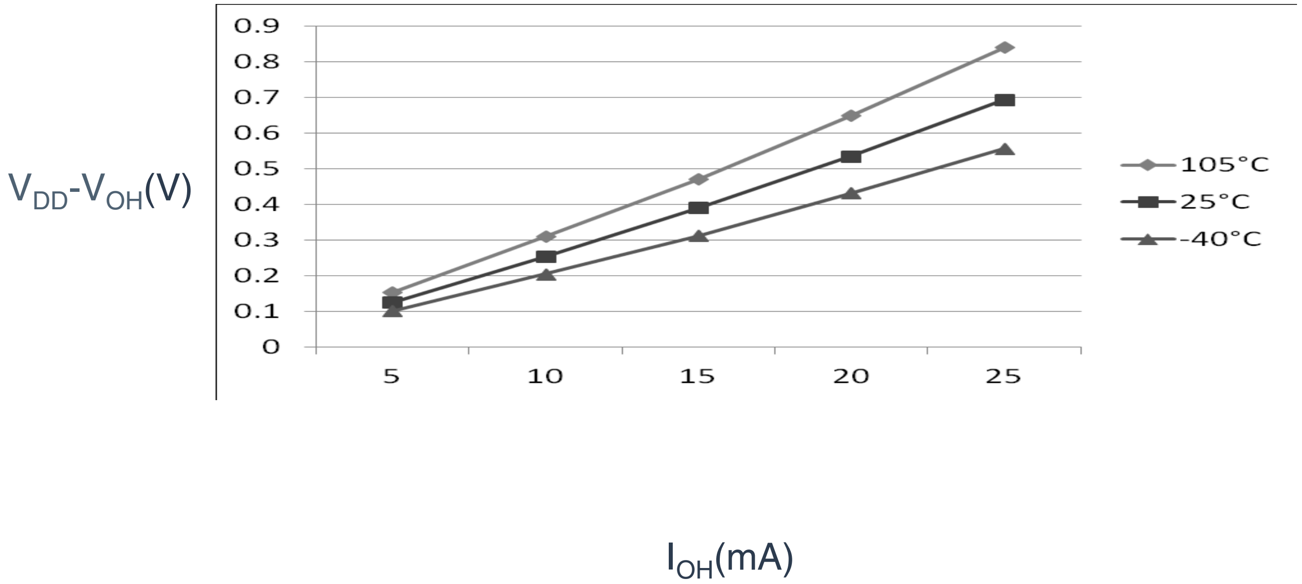


Figure 4. Typical V_{DD}-V_{OH} Vs. I_{OH} (high drive strength) (V_{DD} = 3 V)

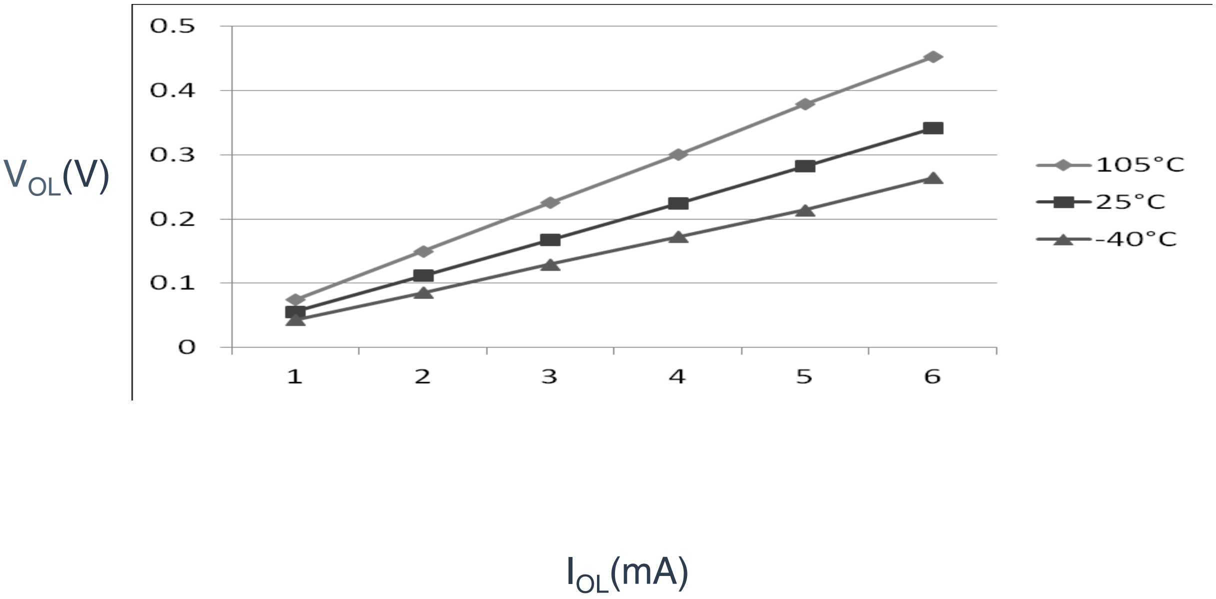


Figure 5. Typical V_{OL} Vs. I_{OL} (standard drive strength) (V_{DD} = 5 V)

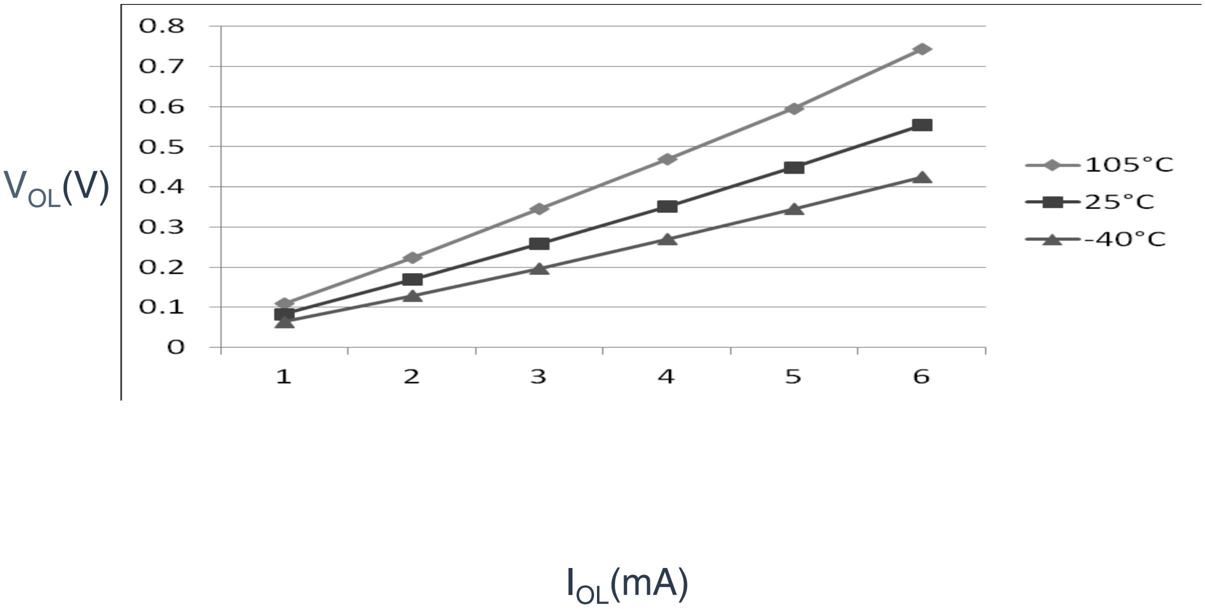


Figure 6. Typical V_{OL} Vs. I_{OL} (standard drive strength) (V_{DD} = 3 V)

5.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 5. Supply current characteristics

C	Parameter	Symbol	Core/Bus Freq	V_{DD} (V)	Typical[1]	Max[2]	Unit	Temp
C	Run supply current FEI mode, all modules clocks enabled; run from flash	RI_{DD}	40/20 MHz	5	7.8	—	mA	–40 to 105 °C
C			20/20 MHz		6.7	—		
C			10/10 MHz		4.5	—		
			1/1 MHz		1.5	—		
C			40/20 MHz	3	7.7	—		
C			20/20 MHz		6.6	—		
C			10/10 MHz		4.4	—		
			1/1 MHz		1.45	—		
C	Run supply current FEI mode, all modules clocks disabled; run from flash	RI_{DD}	40/20 MHz	5	6.3	—	mA	–40 to 105 °C
C			20/20 MHz		5.3	—		
C			10/10 MHz		3.7	—		
			1/1 MHz		1.5	—		
C			40/20 MHz	3	6.2	—		
C			20/20 MHz		5.3	—		
C			10/10 MHz		3.7	—		
			1/1 MHz		1.4	—		
C	Run supply current FBE mode, all modules clocks enabled; run from RAM	RI_{DD}	40/20 MHz	5	10.3	—	mA	–40 to 105 °C
P			20/20 MHz		9	14.8		
C			10/10 MHz		5.2	—		
			1/1 MHz		1.45	—		
C			40/20 MHz	3	10.2	—		
P			20/20 MHz		8.8	11.8		
C			10/10 MHz		5.1	—		
			1/1 MHz		1.4	—		
C	Run supply current FBE mode, all modules clocks disabled; run from RAM	RI_{DD}	40/20 MHz	5	8.9	—	mA	–40 to 105 °C
P			20/20 MHz		8	12.3		
C			10/10 MHz		4.4	—		
			1/1 MHz		1.35	—		
C			40/20 MHz	3	8.8	—		
P			20/20 MHz		7.8	9.2		
C			10/10 MHz		4.2	—		
			1/1 MHz		1.3	—		

Table continues on the next page...

Table 5. Supply current characteristics (continued)

C	Parameter	Symbol	Core/Bus Freq	V_{DD} (V)	Typical[1]	Max[2]	Unit	Temp
C	Wait mode current FEI mode, all modules clocks enabled	WI_{DD}	40/20 MHz	5	6.4	—	mA	–40 to 105 °C
P			20/20 MHz		5.5	—		
C			20/10 MHz		3.5	—		
			1/1 MHz		1.4	—		
C			40/20 MHz	3	6.3	—		
C			20/20 MHz		5.4	—		
			10/10 MHz		3.4	—		
			1/1 MHz		1.4	—		
P	Stop mode supply current no clocks active (except 1 kHz LPO clock)[3]	SI_{DD}	—	5	2	85	μA	–40 to 105 °C
P			—	3	1.9	80		–40 to 105 °C
C	ADC adder to Stop ADLPC = 1 ADLSMP = 1 ADCO = 1 MODE = 10B ADICLK = 11B	—	—	5	86 (64-, 44-pin packages) 42 (32-pin package)	—	μA	–40 to 105 °C
C				3	82 (64-, 44-pin packages) 41 (32-pin package)	—		
C	ACMP adder to Stop	—	—	5	12	—	μA	–40 to 105 °C
C				3	12	—		
C	LVD adder to stop[4]	—	—	5	128	—	μA	–40 to 105 °C
C				3	124	—		

[1] Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

[2] The Max current is observed at high temperature of 105 °C.

[3] RTC adder causes I_{DD} to increase typically by less than 1 μA; RTC clock source is 1 kHz LPO clock.

[4] LVD is periodically woken up from Stop by 5% duty cycle. The period is equal to or less than 2 ms.

5.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation play a significant role in EMC performance. The system designer must consult the following applications notes, available on **nxp.com** for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers

- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers
- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

5.1.3.1 EMC radiated emissions operating behaviors

Table 6. EMC radiated emissions operating behaviors for 64-pin QFP package

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	14	dBμV	[1], [2]
V_{RE2}	Radiated emissions voltage, band 2	50–150	15	dBμV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	3	dBμV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	4	dBμV	
V_{RE_IEC}	IEC level	0.15–1000	M	—	[2], [3]

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V_{DD} = 5.0 V, T_A = 25 °C, f_{OSC} = 10 MHz (crystal), f_{BUS} = 20 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

5.2 Switching specifications

5.2.1 Control timing

Table 7. Control timing

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
1	D	System and core clock		f_{Sys}	DC	—	40	MHz
2	P	Bus frequency ($t_{cyc} = 1/f_{Bus}$)		f_{Bus}	DC	—	20	MHz
3	P	Internal low power oscillator frequency		f_{LPO}	0.67	1.0	1.25	KHz
4	D	External reset pulse width[2]		t_{extrst}	1.5 × t_{cyc}	—	—	ns
5	D	Reset low drive		t_{rstdrv}	34 × t_{cyc}	—	—	ns
6	D	IRQ pulse width	Asynchronous path[2]	t_{ILIH}	100	—	—	ns
	D		Synchronous path[3]	t_{IHIL}	1.5 × t_{cyc}	—	—	ns

Table continues on the next page...

Table 7. Control timing (continued)

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
7	D	Keyboard interrupt pulse width	Asynchronous path[2]	t_{ILIH}	100	—	—	ns
	D		Synchronous path	t_{IHIL}	$1.5 \times t_{cyc}$	—	—	ns
8	C	Port rise and fall time - Normal drive strength (load = 50 pF)[4]	—	t_{Rise}	—	10.2	—	ns
	C			t_{Fall}	—	9.5	—	ns
	C	Port rise and fall time - high drive strength (load = 50 pF)[4]	—	t_{Rise}	—	5.4	—	ns
	C			t_{Fall}	—	4.6	—	ns

1. Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a $\overline{\text{RESET}}$ pin request.
3. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.
4. Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range -40 °C to 105 °C.

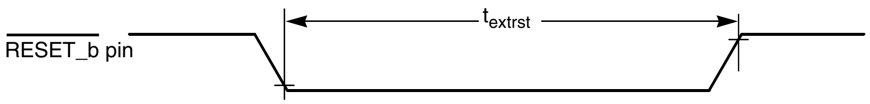


Figure 9. Reset timing

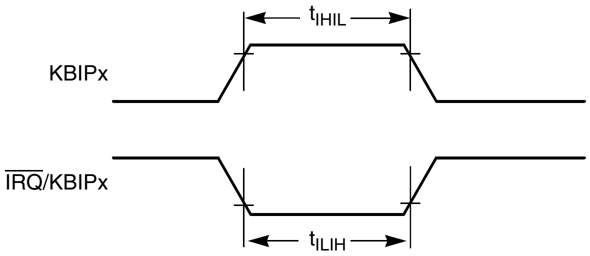


Figure 10. KBIPx timing

5.2.2 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 8. FTM input timing

C	Function	Symbol	Min	Max	Unit
D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
D	External clock period	t_{TCLK}	4	—	t_{cyc}

Table continues on the next page...

5.3.2 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 10. Thermal attributes

Board type	Symbol	Description	64 LQFP	64 QFP	44 LQFP	32 LQFP	32 QFN	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	71	61	75	86	97	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	53	47	53	57	33	°C/W	1, 3
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	59	50	62	72	81	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	46	41	47	51	27	°C/W	1, 3
—	$R_{\theta JB}$	Thermal resistance, junction to board	35	32	34	33	12	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	20	23	20	24	1.3	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	5	8	5	6	3	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Table 13. Flash and EEPROM characteristics (continued)

C	Characteristic	Symbol	Min[1]	Typical[2]	Max[3]	Unit[4]
D	NVM Bus frequency	f_{NVMBUS}	1	—	25	MHz
D	NVM Operating frequency	f_{NVMOP}	0.8	1	1.05	MHz
D	Erase Verify All Blocks	t_{VFYALL}	—	—	17338	t_{cyc}
D	Erase Verify Flash Block	t_{RD1BLK}	—	—	16913	t_{cyc}
D	Erase Verify EEPROM Block	t_{RD1BLK}	—	—	810	t_{cyc}
D	Erase Verify Flash Section	t_{RD1SEC}	—	—	484	t_{cyc}
D	Erase Verify EEPROM Section	$t_{DRD1SEC}$	—	—	555	t_{cyc}
D	Read Once	t_{RDONCE}	—	—	450	t_{cyc}
D	Program Flash (2 word)	t_{PGM2}	0.12	0.12	0.29	ms
D	Program Flash (4 word)	t_{PGM4}	0.20	0.21	0.46	ms
D	Program Once	$t_{PGMONCE}$	0.20	0.21	0.21	ms
D	Program EEPROM (1 Byte)	t_{DPGM1}	0.10	0.10	0.27	ms
D	Program EEPROM (2 Byte)	t_{DPGM2}	0.17	0.18	0.43	ms
D	Program EEPROM (3 Byte)	t_{DPGM3}	0.25	0.26	0.60	ms
D	Program EEPROM (4 Byte)	t_{DPGM4}	0.32	0.33	0.77	ms
D	Erase All Blocks	t_{ERSALL}	96.01	100.78	101.49	ms
D	Erase Flash Block	t_{ERSBLK}	95.98	100.75	101.44	ms
D	Erase Flash Sector	t_{ERSPG}	19.10	20.05	20.08	ms
D	Erase EEPROM Sector	t_{DERSPG}	4.81	5.05	20.57	ms
D	Unsecure Flash	t_{UNSECU}	96.01	100.78	101.48	ms
D	Verify Backdoor Access Key	t_{VFYKEY}	—	—	464	t_{cyc}
D	Set User Margin Level	t_{MLOADU}	—	—	407	t_{cyc}
C	FLASH Program/erase endurance T_L to T_H = -40 °C to 105 °C	n_{FLPE}	10 k	100 k	—	Cycles
C	EEPROM Program/erase endurance TL to TH = -40 °C to 105 °C	n_{FLPE}	50 k	500 k	—	Cycles
C	Data retention at an average junction temperature of T_{Javg} = 85°C after up to 10,000 program/erase cycles	t_{D_ret}	15	100	—	years

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}
2. Typical times are based on typical f_{NVMOP} and maximum f_{NVMBUS}
3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging
4. $t_{cyc} = 1 / f_{NVMBUS}$

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Flash Memory Module section in the reference manual.

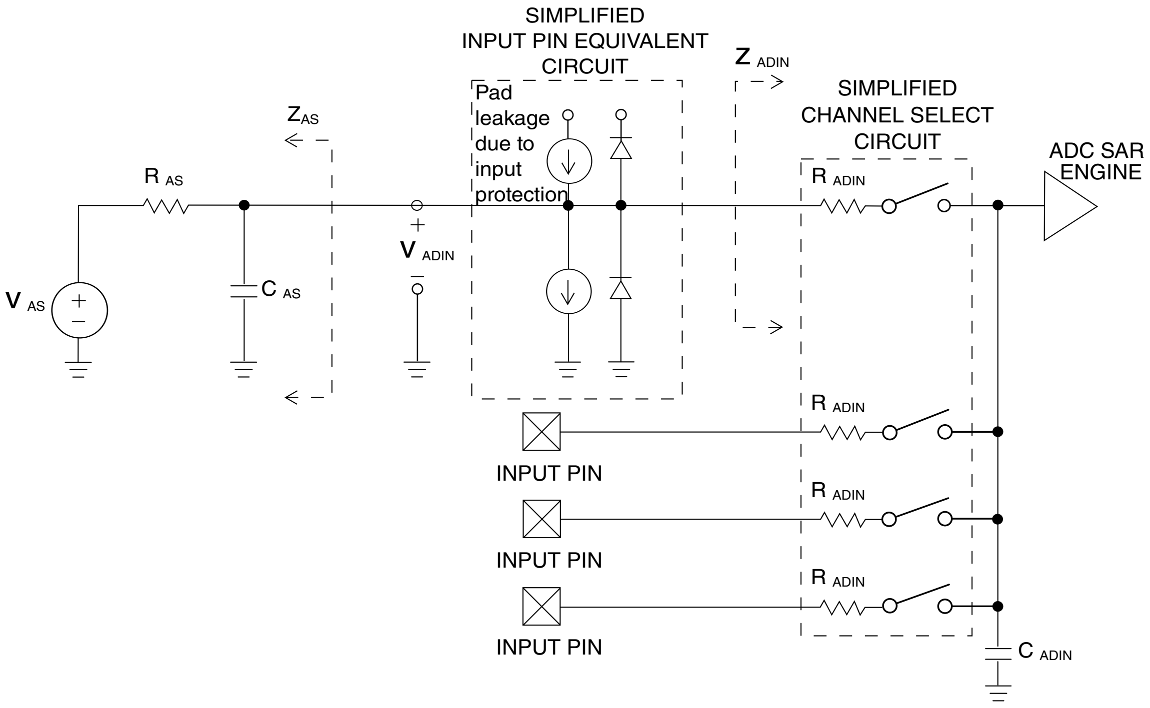


Figure 16. ADC input impedance equivalency diagram

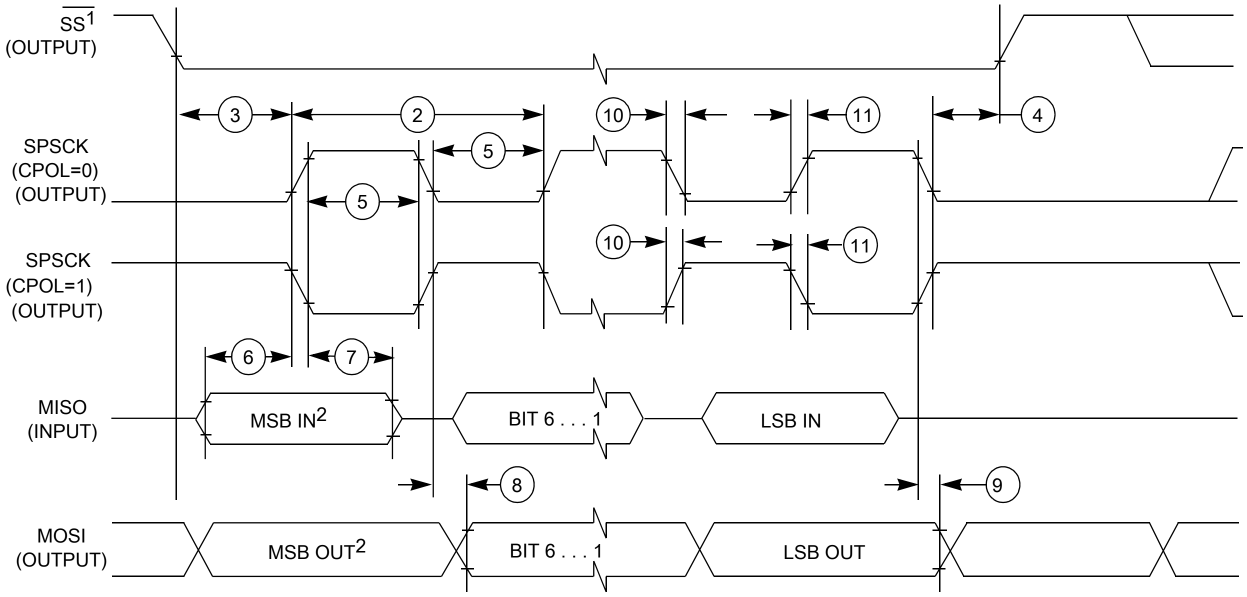
Table 15. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Characteristic	Conditions	C	Symbol	Min	Typ[1]	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	133	—	µA
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	218	—	µA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	327	—	µA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	582	990	µA
Supply current	Stop, reset, module off	T	I_{DDA}	—	0.011	1	µA
ADC asynchronous clock source	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz

Table continues on the next page...

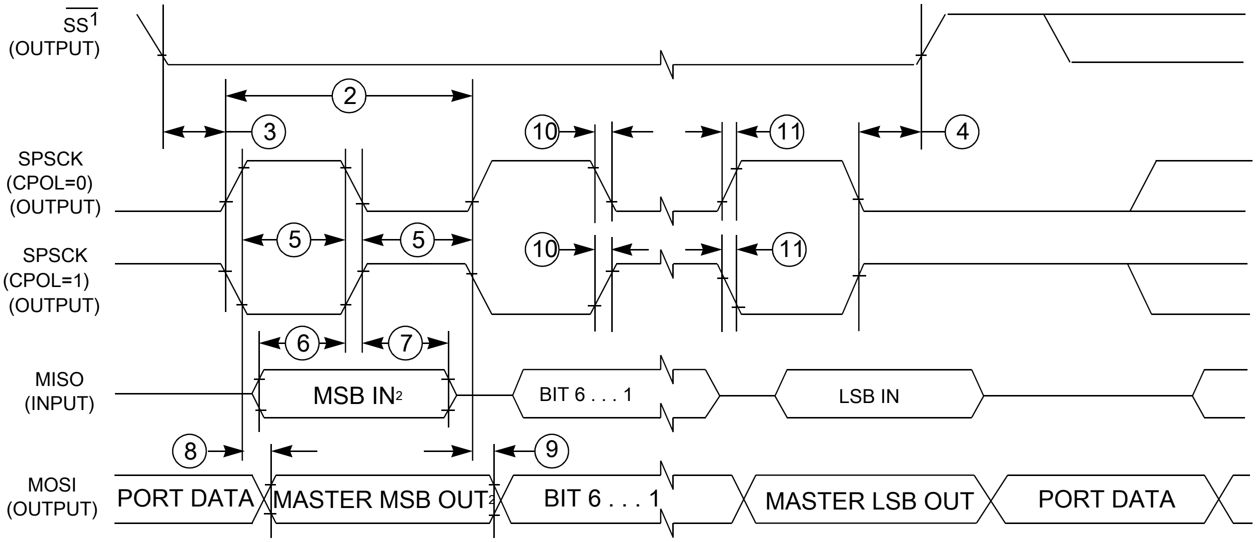
Table 17. SPI master mode timing (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Comment
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 17. SPI master mode timing (CPHA=0)

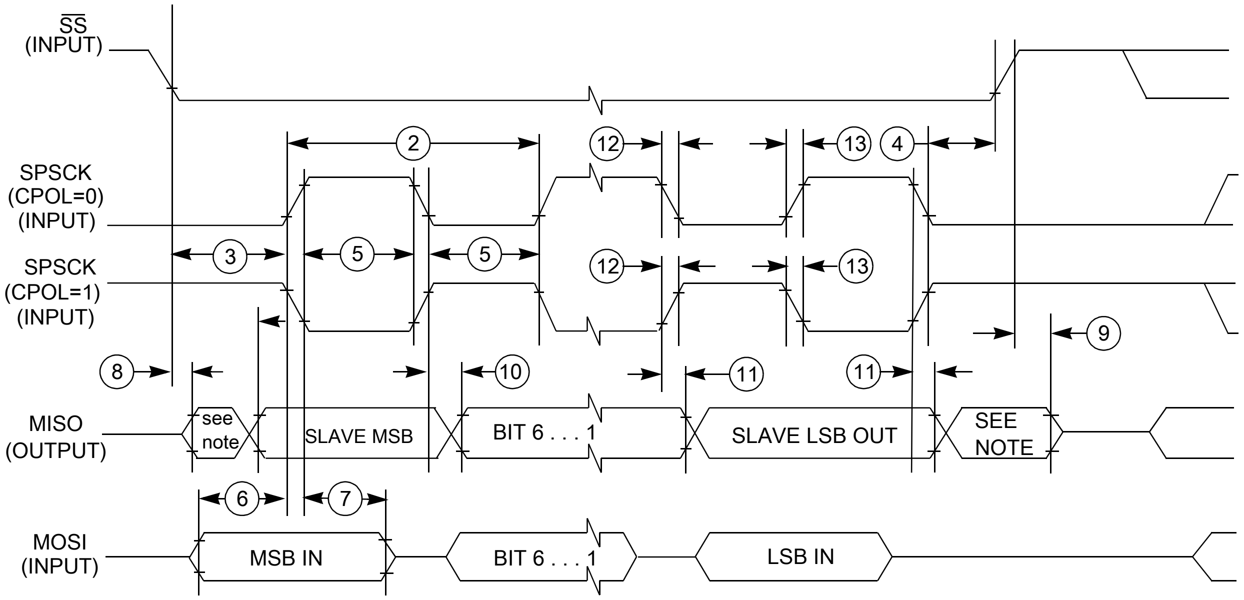


1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. SPI master mode timing (CPHA=1)

Table 18. SPI slave mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	0	$f_{Bus}/4$	Hz	f_{Bus} is the bus clock as defined in Control timing.
2	t_{SPSCK}	SPSCK period	4 x t_{Bus}	—	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1	—	t_{Bus}	—
4	t_{Lag}	Enable lag time	1	—	t_{Bus}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{Bus} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	25	—	ns	—
8	t_a	Slave access time	—	t_{Bus}	ns	Time to data active from high-impedance state
9	t_{dis}	Slave MISO disable time	—	t_{Bus}	ns	Hold time to high-impedance state
10	t_v	Data valid (after SPSCK edge)	—	25	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{Bus} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



NOTE: Not defined

Figure 19. SPI slave mode timing (CPHA = 0)

Table 19. Pin availability by package pin-count (continued)

Pin Number			Lowest Priority <-- --> Highest				
64-QFP/ LQFP	**44-LQFP**	**32- LQFP/QFN**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
28	—	—	PTF6	—	—	—	ADC0_SE14
29	—	—	PTF5	—	—	—	ADC0_SE13
30	—	—	PTF4	—	—	—	ADC0_SE12
31	21	15	PTB3	KBI0_P7	SPI0_MOSI	FTM0_CH1	ADC0_SE7
32	22	16	PTB2	KBI0_P6	SPI0_SCK	FTM0_CH0	ADC0_SE6
33	23	17	PTB1	KBI0_P5	UART0_TX	—	ADC0_SE5
34	24	18	PTB0	KBI0_P4	UART0_RX	—	ADC0_SE4
35	—	—	PTF3	—	—	—	—
36	—	—	PTF2	—	—	—	—
37	25	19	PTA7	—	FTM2_FLT2	ACMP1_IN1	ADC0_SE3
38	26	20	PTA6	—	FTM2_FLT1	ACMP1_IN0	ADC0_SE2
39	—	—	PTE4	—	—	—	—
40	27	—	—	—	—	—	VSS
41	28	—	—	—	—	—	VDD
42	—	—	PTF1	—	—	—	—
43	—	—	PTF0	—	—	—	—
44	29	—	PTD4	KBI1_P4	—	—	—
45	30	21	PTD3	KBI1_P3	SPI1_PCS0	—	—
46	31	22	PTD2	KBI1_P2	SPI1_MISO	—	—
47	32	23	PTA3[4]	KBI0_P3	UART0_TX	I2C0_SCL	—
48	33	24	PTA2[4]	KBI0_P2	UART0_RX	I2C0_SDA	—
49	34	25	PTA1	KBI0_P1	FTM0_CH1	ACMP0_IN1	ADC0_SE1
50	35	26	PTA0	KBI0_P0	FTM0_CH0	ACMP0_IN0	ADC0_SE0
51	36	27	PTC7	—	UART1_TX	—	—
52	37	28	PTC6	—	UART1_RX	—	—
53	—	—	PTE3	—	SPI0_PCS0	—	—
54	38	—	PTE2	—	SPI0_MISO	—	—
55	—	—	PTG3	—	—	—	—
56	—	—	PTG2	—	—	—	—
57	—	—	PTG1	—	—	—	—
58	—	—	PTG0	—	—	—	—
59	39	—	PTE1[1]	—	SPI0_MOSI	—	—
60	40	—	PTE0[1]	—	SPI0_SCK	FTM1_CLK	—
61	41	29	PTC5	—	FTM1_CH1	—	RTCO
62	42	30	PTC4	RTCO	FTM1_CH0	ACMP0_IN2	SWD_CLK
63	43	31	PTA5	IRQ	FTM0_CLK	—	$\overline{\text{RESET}}$
64	44	32	PTA4	—	ACMP0_OUT	—	SWD_DIO

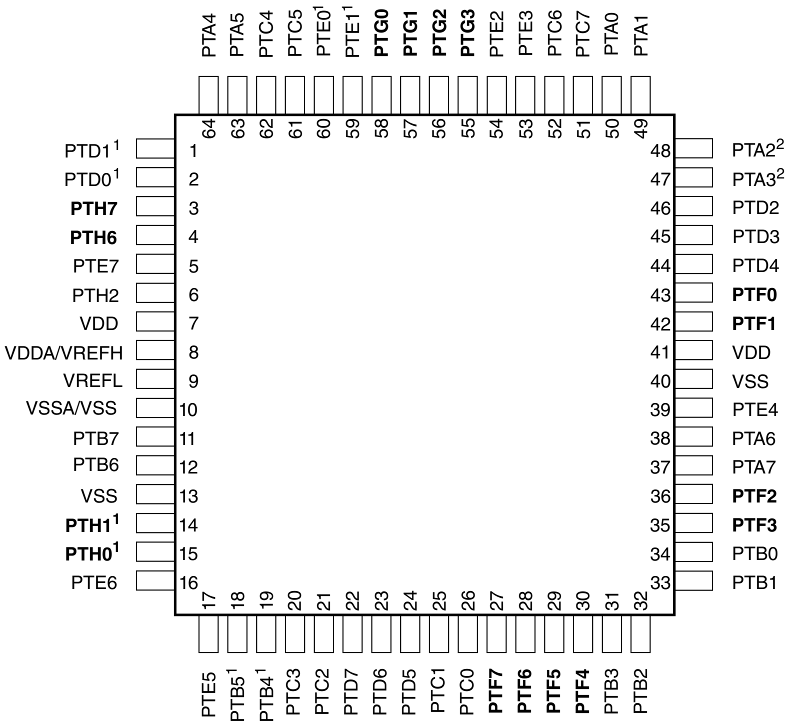
1. This is a high-current drive pin when operated as output.

2. VREFH and VDDA are internally connected.
3. VSSA and VSS are internally connected.
4. This is a true open-drain pin when operated as output.

Note

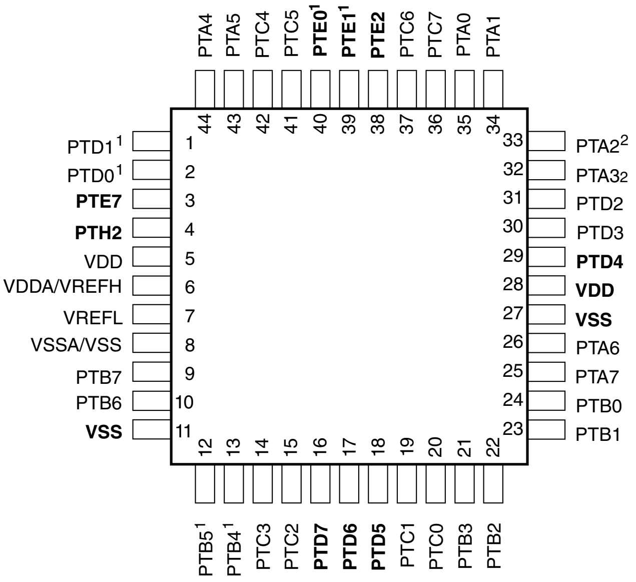
When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear any associated flags before interrupts are enabled. Table 19 illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

8.2 Device pin assignment



Pins in **bold** are not available on less pin-count packages.
1. High source/sink current pins
2. True open drain pins

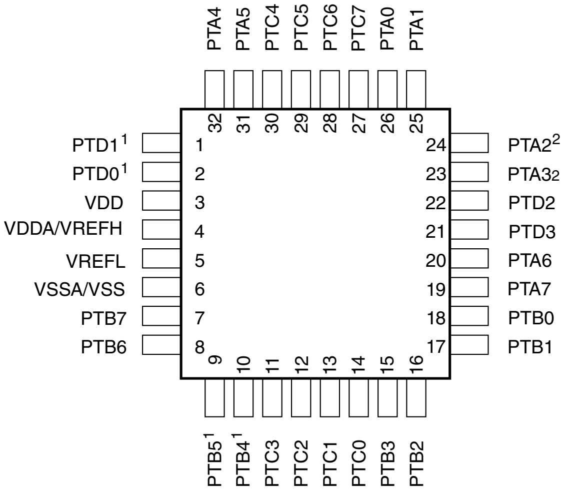
Figure 21. 64-pin QFP/LQFP packages



Pins in **bold** are not available on less pin-count packages.

1. High source/sink current pins
2. True open drain pins

Figure 22. 44-pin LQFP package



1. High source/sink current pins
2. True open drain pins

Figure 23. 32-pin LQFP package

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