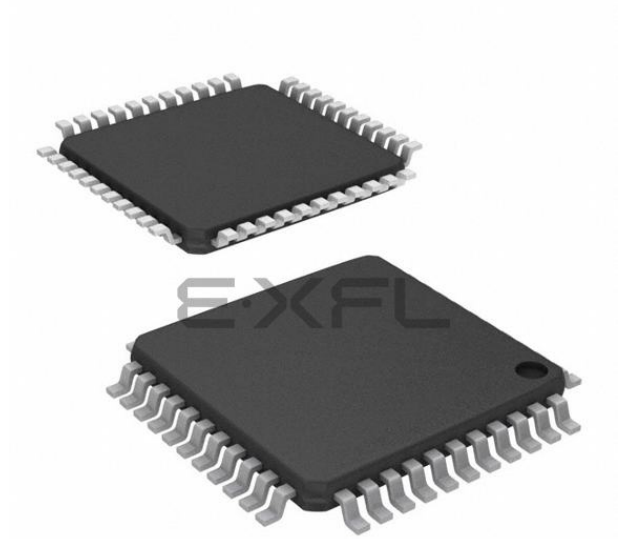

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LVD, PWM, WDT
Number of I/O	37
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x6b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mke02z32vld4

- Timers
  - One 6-channel FlexTimer/PWM (FTM)
  - Two 2-channel FlexTimer/PWM (FTM)
  - One 2-channel periodic interrupt timer (PIT)
  - One real-time clock (RTC)
- Communication interfaces
  - Two SPI modules (SPI)
  - Up to three UART modules (UART)
  - One I2C module (I2C)
- Package options
  - 64-pin QFP/LQFP
  - 44-pin LQFP
  - 32-pin LQFP
  - 32-pin QFN

Table of Contents

Field	Description	Values
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• LC = 32 LQFP (7 mm x 7 mm) • FM = 32 QFN (5 mm x 5 mm) • LD = 44 LQFP (10 mm x 10 mm) • QH = 64 QFP (14 mm x 14 mm) • LH = 64 LQFP (10 mm x 10 mm)
CC	Maximum CPU frequency (MHz)	• 4 = 40 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

2.4 Example

This is an example part number:

MKE02Z64VQH4

3 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 1. Parameter classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	–6000	+6000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 125°C	–100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78D, *IC Latch-up Test*.
   - Test was performed at 125 °C case temperature (Class II).
   - I/O pins pass ±100 mA I-test with I_{DD} current limit at 800 mA.
   - I/O pins pass +60/-100 mA I-test with I_{DD} current limit at 1000 mA.
   - Supply groups pass 1.5 V_{ccmax}.
   - $\overline{\text{RESET}}$ pin was only tested with negative I-test due to product conditioning requirement.

Table 3. DC characteristics (continued)

Symbol	C	Descriptions			Min	Typical[1]	Max	Unit
V_{OH}	P	Output high voltage	All I/O pins, except PTA2 and PTA3, standard-drive strength	5 V, I_{load} = –5 mA	V_{DD} – 0.8	—	—	V
	C			3 V, I_{load} = –2.5 mA	V_{DD} – 0.8	—	—	V
	P		High current drive pins, high-drive strength[2]	5 V, I_{load} = –20 mA	V_{DD} – 0.8	—	—	V
	C			3 V, I_{load} = –10 mA	V_{DD} – 0.8	—	—	V
I_{OHT}	D	Output high current	Max total I_{OH} for all ports	5 V	—	—	–100	mA
				3 V	—	—	–60	
V_{OL}	P	Output low voltage	All I/O pins, standard-drive strength	5 V, I_{load} = 5 mA	—	—	0.8	V
	C			3 V, I_{load} = 2.5 mA	—	—	0.8	V
	P		High current drive pins, high-drive strength[2]	5 V, I_{load} =20 mA	—	—	0.8	V
	C			3 V, I_{load} = 10 mA	—	—	0.8	V
I_{OLT}	D	Output low current	Max total I_{OL} for all ports	5 V	—	—	100	mA
				3 V	—	—	60	
V_{IH}	P	Input high voltage	All digital inputs	4.5≤V_{DD}<5.5 V	0.65 × V_{DD}	—	—	V
				2.7≤V_{DD}<4.5 V	0.70 × V_{DD}	—	—	
V_{IL}	P	Input low voltage	All digital inputs	4.5≤V_{DD}<5.5 V	—	—	0.35 × V_{DD}	V
				2.7≤V_{DD}<4.5 V	—	—	0.30 × V_{DD}	
V_{hys}	C	Input hysteresis	All digital inputs	—	0.06 × V_{DD}	—	—	mV
$\lvert I_{In} \rvert$	P	Input leakage current	Per pin (pins in high impedance input mode)	V_{IN} = V_{DD} or V_{SS}	—	0.1	1	µA
$\lvert I_{INTOT} \rvert$	C	Total leakage combined for all port pins	Pins in high impedance input mode	V_{IN} = V_{DD} or V_{SS}	—	—	2	µA
R_{PU}	P	Pullup resistors	All digital inputs, when enabled (all I/O pins other than PTA2 and PTA3)	—	30.0	—	50.0	kΩ
R_{PU}[3]	P	Pullup resistors	PTA2 and PTA3 pins	—	30.0	—	60.0	kΩ
I_{IC}	D	DC injection current[4, 5, 6]	Single pin limit	V_{IN} < V_{SS}, V_{IN} > V_{DD}	-2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	25	
C_{In}	C	Input capacitance, all pins		—	—	—	7	pF
V_{RAM}	C	RAM retention voltage		—	2.0	—	—	V

1. Typical values are measured at 25 °C. Characterized, not tested.
2. Only PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0, and PTH1 support high current output.

3. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
4. All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD}. PTA2 and PTA3 are true open drain I/O pins that are internally clamped to V_{SS}.
5. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger value.
6. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is higher than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as when no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Table 4. LVD and POR specification

Symbol	C	Description		Min	Typ	Max	Unit
V_{POR}	D	POR re-arm voltage[1]		1.5	1.75	2.0	V
V_{LVDH}	C	Falling low-voltage detect threshold—high range (LVDV = 1)[2]		4.2	4.3	4.4	V
V_{LVW1H}	C	Falling low-voltage warning threshold—high range	Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V
V_{LVW2H}	C		Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V_{LVW3H}	C		Level 3 falling (LVWV = 10)	4.6	4.6	4.7	V
V_{LVW4H}	C		Level 4 falling (LVWV = 11)	4.7	4.7	4.8	V
V_{HYSH}	C	High range low-voltage detect/warning hysteresis		—	100	—	mV
V_{LVDL}	C	Falling low-voltage detect threshold—low range (LVDV = 0)		2.56	2.61	2.66	V
V_{LVW1L}	C	Falling low-voltage warning threshold—low range	Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V
V_{LVW2L}	C		Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V
V_{LVW3L}	C		Level 3 falling (LVWV = 10)	2.82	2.9	2.98	V
V_{LVW4L}	C		Level 4 falling (LVWV = 11)	2.92	3.0	3.08	V
V_{HYSDL}	C	Low range low-voltage detect hysteresis		—	40	—	mV
V_{HYSWL}	C	Low range low-voltage warning hysteresis		—	80	—	mV
V_{BG}	P	Buffered bandgap output [3]		1.14	1.16	1.18	V

1. Maximum is highest voltage that POR is guaranteed.
2. Rising thresholds are falling threshold + hysteresis.
3. voltage Factory trimmed at V_{DD} = 5.0 V, Temp = 25 °C

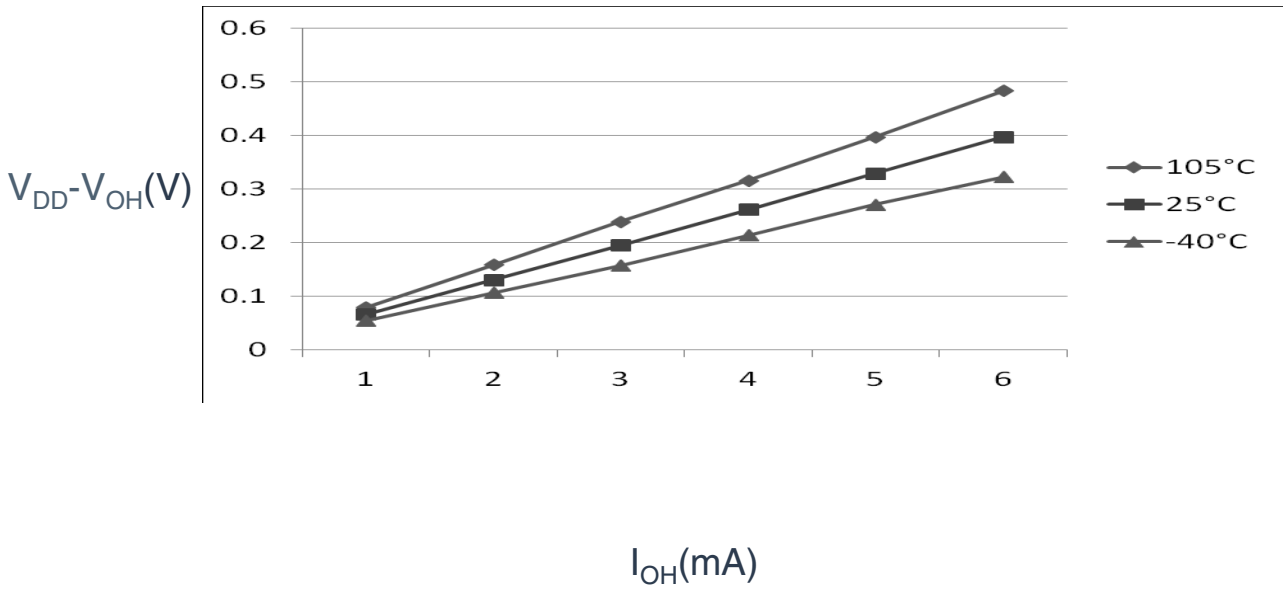


Figure 1. Typical V_{DD}-V_{OH} Vs. I_{OH} (standard drive strength) (V_{DD} = 5 V)

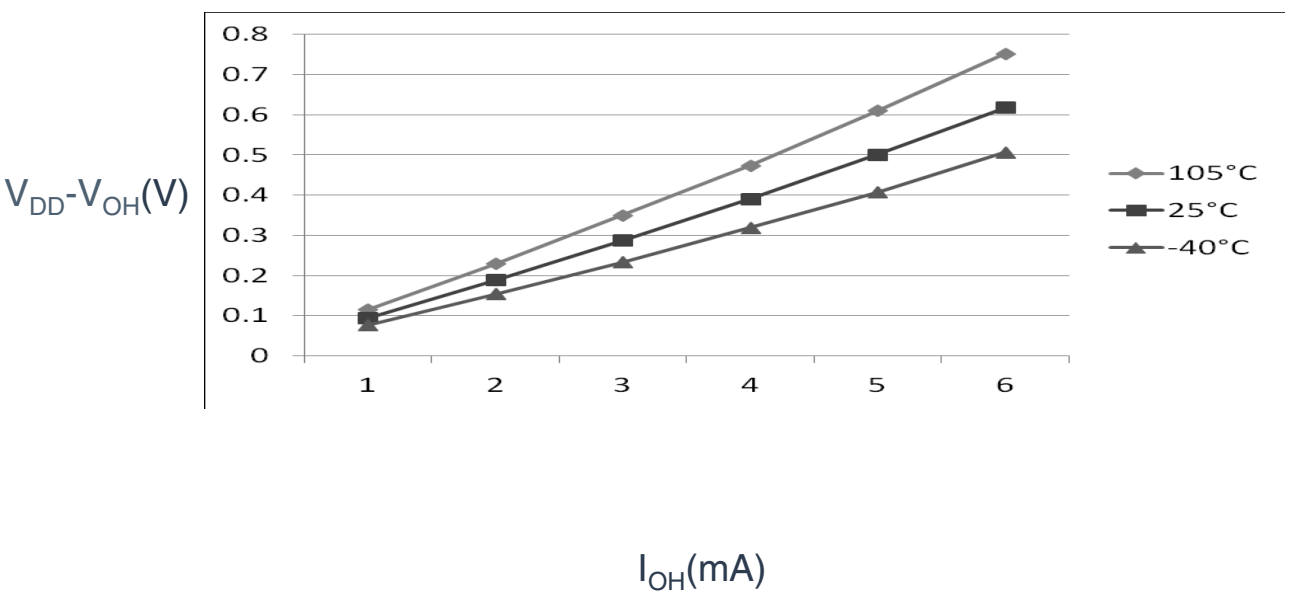


Figure 2. Typical V_{DD}-V_{OH} Vs. I_{OH} (standard drive strength) (V_{DD} = 3 V)

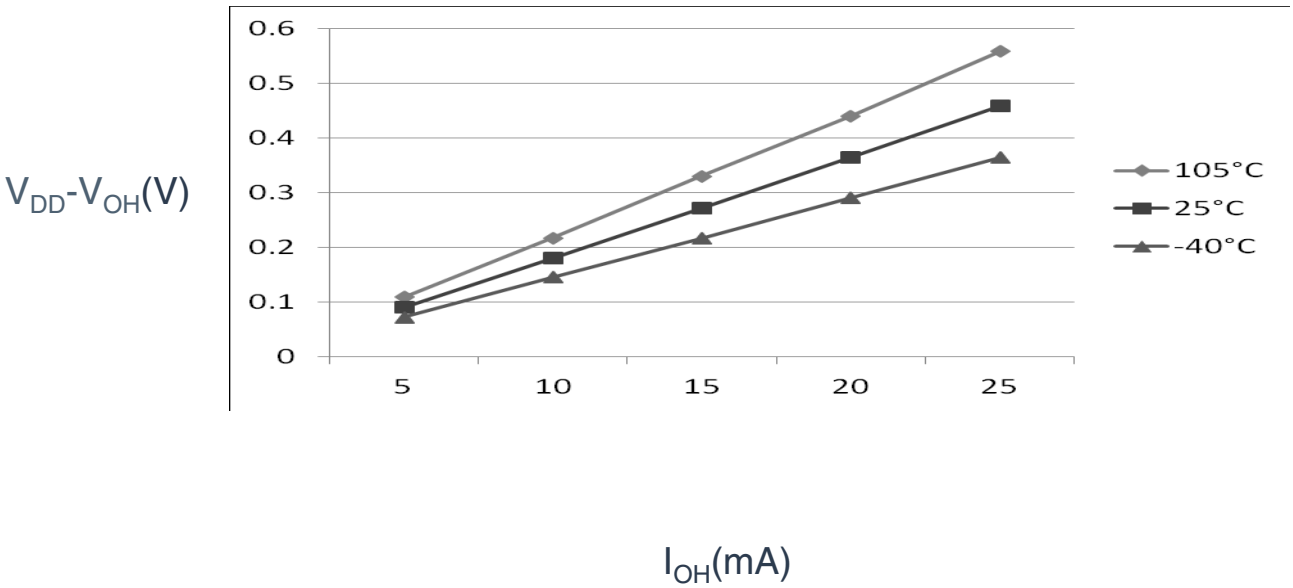


Figure 3. Typical V_{DD}-V_{OH} Vs. I_{OH} (high drive strength) (V_{DD} = 5 V)

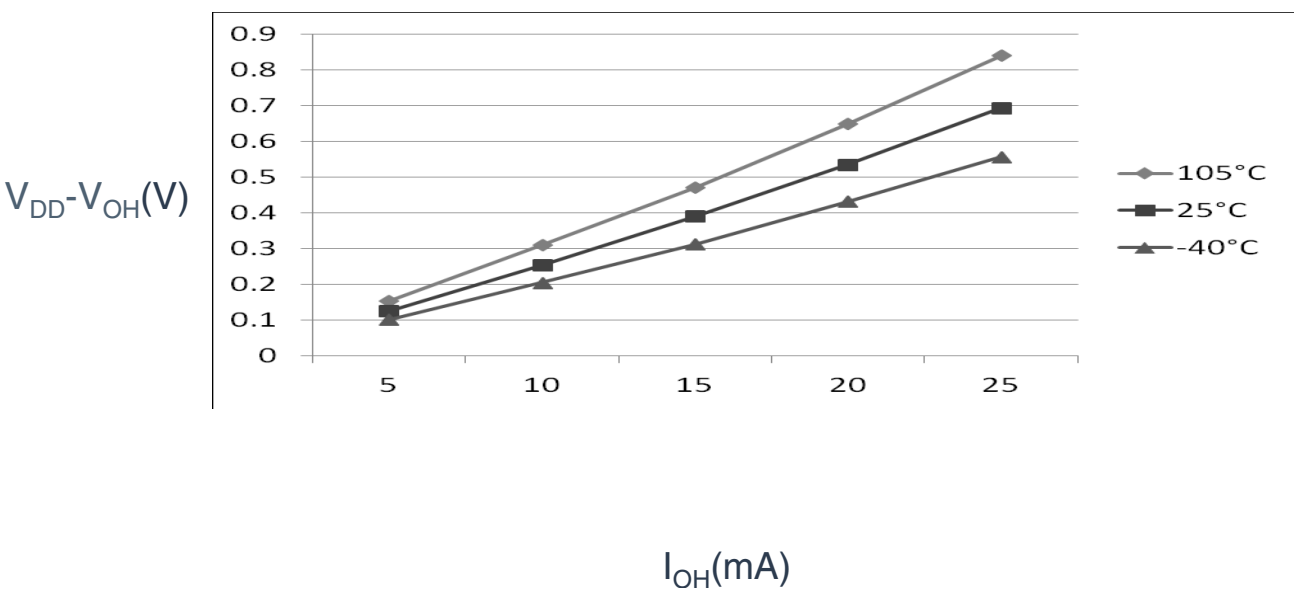


Figure 4. Typical V_{DD}-V_{OH} Vs. I_{OH} (high drive strength) (V_{DD} = 3 V)

Table 5. Supply current characteristics (continued)

C	Parameter	Symbol	Core/Bus Freq	V_{DD} (V)	Typical[1]	Max[2]	Unit	Temp
C	Wait mode current FEI mode, all modules clocks enabled	WI_{DD}	40/20 MHz	5	6.4	—	mA	–40 to 105 °C
P			20/20 MHz		5.5	—		
C			20/10 MHz		3.5	—		
			1/1 MHz		1.4	—		
C			40/20 MHz	3	6.3	—		
C			20/20 MHz		5.4	—		
			10/10 MHz		3.4	—		
			1/1 MHz		1.4	—		
P	Stop mode supply current no clocks active (except 1 kHz LPO clock)[3]	SI_{DD}	—	5	2	85	µA	–40 to 105 °C
P			—	3	1.9	80		–40 to 105 °C
C	ADC adder to Stop ADLPC = 1 ADLSMP = 1 ADCO = 1	—	—	5	86 (64-, 44-pin packages) 42 (32-pin package)	—	µA	–40 to 105 °C
C	MODE = 10B ADICLK = 11B			3	82 (64-, 44-pin packages) 41 (32-pin package)	—		
C	ACMP adder to Stop	—	—	5	12	—	µA	–40 to 105 °C
C				3	12	—		
C	LVD adder to stop[4]	—	—	5	128	—	µA	–40 to 105 °C
C				3	124	—		

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. The Max current is observed at high temperature of 105 °C.
3. RTC adder causes I_{DD} to increase typically by less than 1 µA; RTC clock source is 1 kHz LPO clock.
4. LVD is periodically woken up from Stop by 5% duty cycle. The period is equal to or less than 2 ms.

5.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation play a significant role in EMC performance. The system designer must consult the following applications notes, available on **nxp.com** for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers

Where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts - chip internal power

$P_{I/O}$ = Power dissipation on input and output pins - user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$P_D = K \div (T_J + 273\ °C)$

Solving the equations above for K gives:

$K = P_D \times (T_A + 273\ °C) + \theta_{JA} \times (P_D)^2$

where K is a constant pertaining to the particular part. K can be determined by measuring P_D (at equilibrium) for an known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving the above equations iteratively for any value of T_A.

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 SWD electricals

Table 11. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	5.5	V
J1	SWD_CLK frequency of operation • Serial wire debug	0	20	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	3	—	ns

Table continues on the next page...

Table 12. OSC and ICS specifications (temperature range = -40 to 105 °C ambient) (continued)

Num	C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
2	D	Load capacitors		C1, C2	See Note[2]			
3	D	Feedback resistor	Low Frequency, Low-Power Mode[3]	R_F	—	—	—	MΩ
			Low Frequency, High-Gain Mode		—	10	—	MΩ
			High Frequency, Low-Power Mode		—	1	—	MΩ
			High Frequency, High-Gain Mode		—	1	—	MΩ
4	D	Series resistor - Low Frequency	Low-Power Mode [3]	R_S	—	0	—	kΩ
			High-Gain Mode		—	200	—	kΩ
5	D	Series resistor - High Frequency	Low-Power Mode[3]	R_S	—	0	—	kΩ
	D	Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
	D		8 MHz		—	0	—	kΩ
	D		16 MHz		—	0	—	kΩ
6	C	Crystal start-up time low range = 32.768 kHz crystal; High range = 20 MHz crystal[4,5]	Low range, low power	t_{CSTL}	—	1000	—	ms
	C		Low range, high gain		—	800	—	ms
	C		High range, low power	t_{CSTH}	—	3	—	ms
	C		High range, high gain		—	1.5	—	ms
7	T	Internal reference start-up time		t_{IRST}	—	20	50	µs
8	P	Internal reference clock (IRC) frequency trim range		f_{int_t}	31.25	—	39.0625	kHz
9	P	Internal reference clock frequency, factory trimmed	T = 25 °C, V_{DD} = 5 V	f_{int_ft}	—	31.25	—	kHz
10	P	DCO output frequency range	FLL reference = fint_t, flo, or fhi/RDIV	f_{dco}	32	—	40	MHz
11	P	Factory trimmed internal oscillator accuracy	T = 25 °C, V_{DD} = 5 V	Δf_{int_ft}	-0.5	—	0.5	%
12	C	Deviation of IRC over temperature when trimmed at T = 25 °C, V_{DD} = 5 V	Over temperature range from -40 °C to 105°C	Δf_{int_t}	-1	—	0.5	%
			Over temperature range from 0 °C to 105°C	Δf_{int_t}	-0.5	—	0.5	
13	C	Frequency accuracy of DCO output using factory trim value	Over temperature range from -40 °C to 105°C	Δf_{dco_ft}	-1.5	—	1	%
			Over temperature range from 0 °C to 105°C	Δf_{dco_ft}	-1	—	1	

Table continues on the next page...

Table 12. OSC and ICS specifications (temperature range = -40 to 105 °C ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
14	C	FLL acquisition time[4,6]	$t_{Acquire}$	—	—	2	ms
15	C	Long term jitter of DCO output clock (averaged over 2 ms interval)[7]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. See crystal or resonator manufacturer's recommendation.
3. Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.
4. This parameter is characterized and not tested on each device.
5. Proper PC board layout procedures must be followed to achieve specifications.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

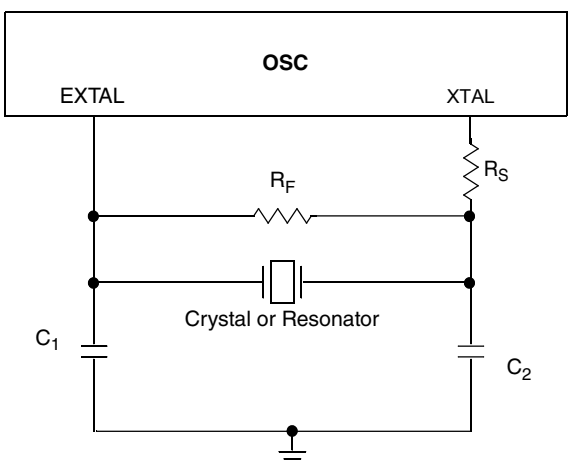


Figure 15. Typical crystal or resonator circuit

6.3 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash and EEPROM memories.

Table 13. Flash and EEPROM characteristics

C	Characteristic	Symbol	Min[1]	Typical[2]	Max[3]	Unit[4]
D	Supply voltage for program/erase –40 °C to 105 °C	$V_{prog/erase}$	2.7	—	5.5	V
D	Supply voltage for read operation	V_{Read}	2.7	—	5.5	V

Table continues on the next page...

6.4 Analog

6.4.1 ADC characteristics

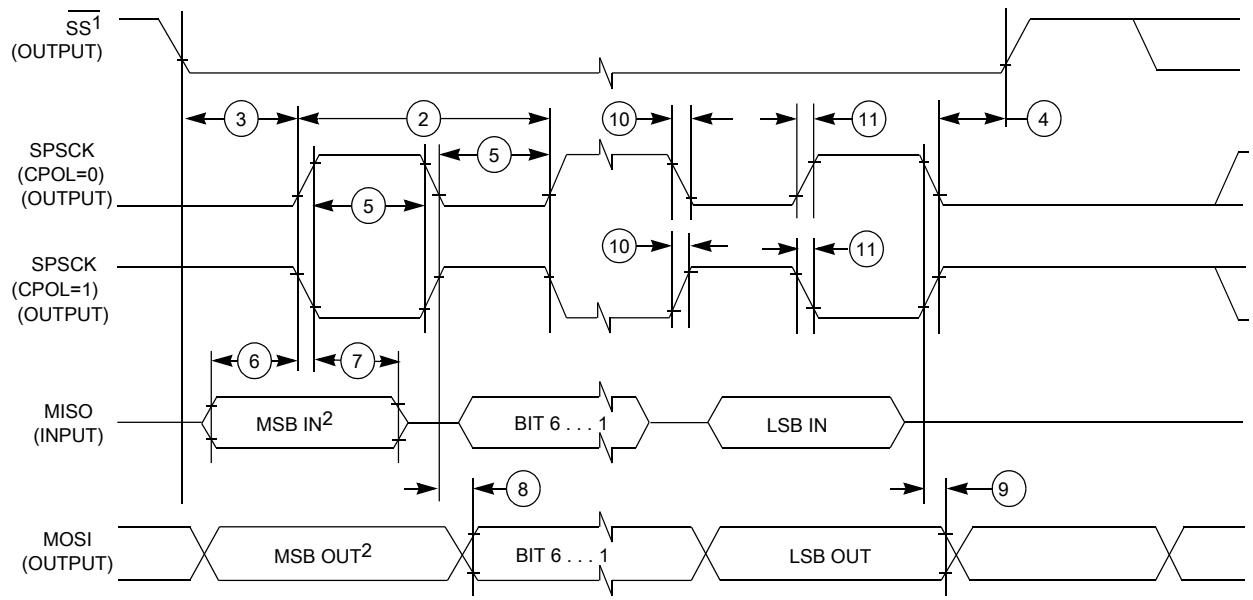
Table 14. 5 V 12-bit ADC operating conditions

Characteristic	Conditions	Symbol	Min	Typ[1]	Max	Unit	Comment
Reference potential	• Low • High	V_{REFL} V_{REFH}	V_{SSA} V_{DDA}	— —	V_{SSA} V_{DDA}	V	—
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	—
	Delta to V_{DD} (V_{DD}-V_{DDA})	ΔV_{DDA}	-100	0	+100	mV	—
Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSA})	ΔV_{SSA}	-100	0	+100	mV	—
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	—
Input resistance		R_{ADIN}	—	3	5	kΩ	—
Analog source resistance	12-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz	R_{AS}	— —	— —	2 5	kΩ	External to MCU
	10-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz		— —	— —	5 10		
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock frequency	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

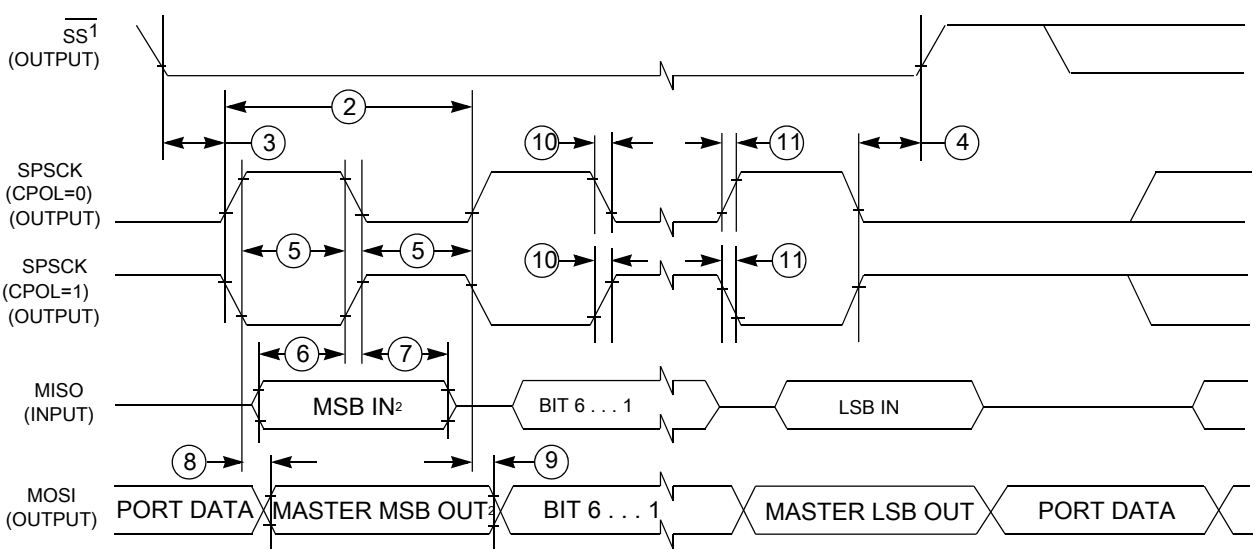
Table 17. SPI master mode timing (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Comment
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 17. SPI master mode timing (CPHA=0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. SPI master mode timing (CPHA=1)

Table 18. SPI slave mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	0	$f_{Bus}/4$	Hz	f_{Bus} is the bus clock as defined in Control timing.
2	t_{SPSCK}	SPSCK period	4 x t_{Bus}	—	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1	—	t_{Bus}	—
4	t_{Lag}	Enable lag time	1	—	t_{Bus}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{Bus} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	25	—	ns	—
8	t_a	Slave access time	—	t_{Bus}	ns	Time to data active from high-impedance state
9	t_{dis}	Slave MISO disable time	—	t_{Bus}	ns	Hold time to high-impedance state
10	t_v	Data valid (after SPSCK edge)	—	25	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{Bus} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

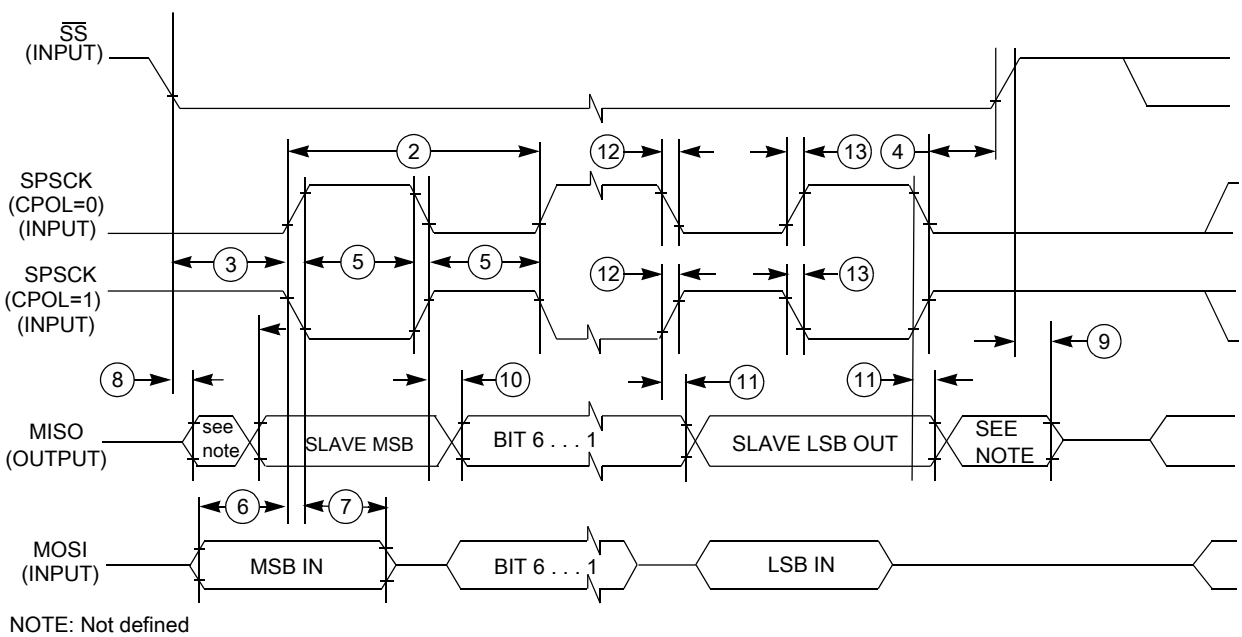


Figure 19. SPI slave mode timing (CPHA = 0)

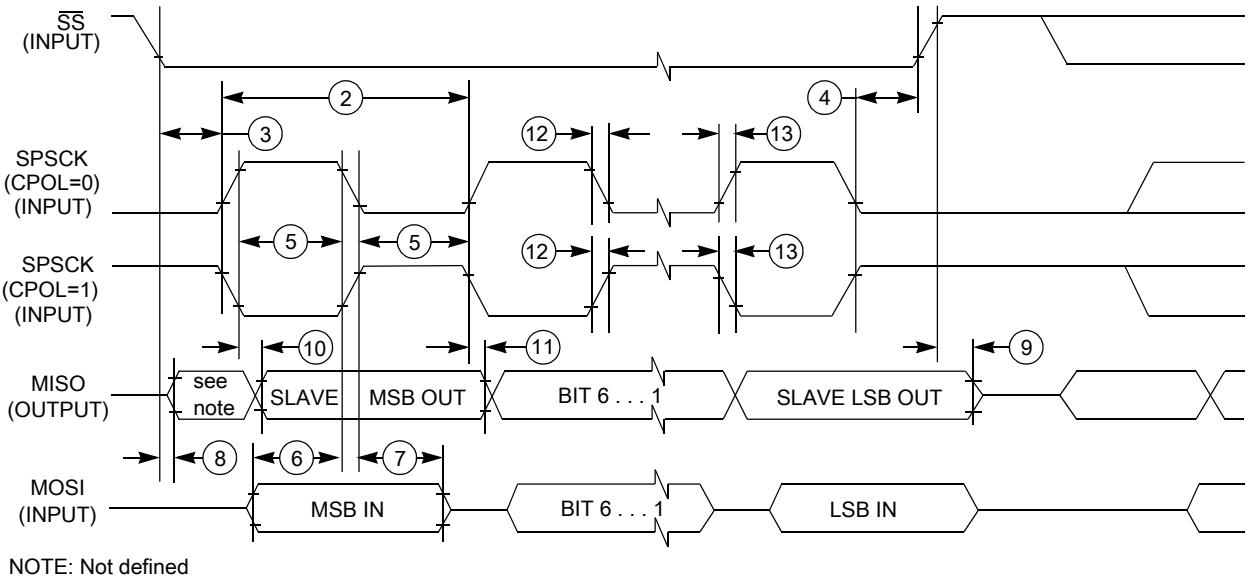


Figure 20. SPI slave mode timing (CPHA=1)

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to **nxp.com** and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
32-pin LQFP	98ASH70029A
32-pin QFN	98ASA00473D
44-pin LQFP	98ASS23225W
64-pin QFP	98ASB42844B
64-pin LQFP	98ASS23234W

8 Pinout

8.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

Table 19. Pin availability by package pin-count

Pin Number			Lowest Priority <-- --> Highest				
64-QFP/ LQFP	44-LQFP	32-LQFP/QFN	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	1	1	PTD1[1]	KBI1_P1	FTM2_CH3	SPI1_MOSI	—
2	2	2	PTD0[1]	KBI1_P0	FTM2_CH2	SPI1_SCK	—
3	—	—	PTH7	—	—	—	—
4	—	—	PTH6	—	—	—	—
5	3	—	PTE7	—	FTM2_CLK	—	FTM1_CH1
6	4	—	PTH2	—	BUSOUT	—	FTM1_CH0
7	5	3	—	—	—	—	VDD
8	6	4	—	—	—	VDDA	VREFH[2]
9	7	5	—	—	—	—	VREFL
10	8	6	—	—	—	VSSA	VSS[3]
11	9	7	PTB7	—	I2C0_SCL	—	EXTAL
12	10	8	PTB6	—	I2C0_SDA	—	XTAL
13	11	—	—	—	—	—	VSS
14	—	—	PTH1[1]	—	FTM2_CH1	—	—
15	—	—	PTH0[1]	—	FTM2_CH0	—	—
16	—	—	PTE6	—	—	—	—
17	—	—	PTE5	—	—	—	—
18	12	9	PTB5[1]	FTM2_CH5	SPI0_PCS0	ACMP1_OUT	—
19	13	10	PTB4[1]	FTM2_CH4	SPI0_MISO	$\overline{\text{NMI}}$	ACMP1_IN2
20	14	11	PTC3	FTM2_CH3	—	—	ADC0_SE11
21	15	12	PTC2	FTM2_CH2	—	—	ADC0_SE10
22	16	—	PTD7	KBI1_P7	UART2_TX	—	—
23	17	—	PTD6	KBI1_P6	UART2_RX	—	—
24	18	—	PTD5	KBI1_P5	—	—	—
25	19	13	PTC1	—	FTM2_CH1	—	ADC0_SE9
26	20	14	PTC0	—	FTM2_CH0	—	ADC0_SE8
27	—	—	PTF7	—	—	—	ADC0_SE15

Table continues on the next page...

Table 19. Pin availability by package pin-count (continued)

Pin Number			Lowest Priority <-- --> Highest				
64-QFP/ LQFP	44-LQFP	32-LQFP/QFN	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
28	—	—	PTF6	—	—	—	ADC0_SE14
29	—	—	PTF5	—	—	—	ADC0_SE13
30	—	—	PTF4	—	—	—	ADC0_SE12
31	21	15	PTB3	KBI0_P7	SPI0_MOSI	FTM0_CH1	ADC0_SE7
32	22	16	PTB2	KBI0_P6	SPI0_SCK	FTM0_CH0	ADC0_SE6
33	23	17	PTB1	KBI0_P5	UART0_TX	—	ADC0_SE5
34	24	18	PTB0	KBI0_P4	UART0_RX	—	ADC0_SE4
35	—	—	PTF3	—	—	—	—
36	—	—	PTF2	—	—	—	—
37	25	19	PTA7	—	FTM2_FLT2	ACMP1_IN1	ADC0_SE3
38	26	20	PTA6	—	FTM2_FLT1	ACMP1_IN0	ADC0_SE2
39	—	—	PTE4	—	—	—	—
40	27	—	—	—	—	—	VSS
41	28	—	—	—	—	—	VDD
42	—	—	PTF1	—	—	—	—
43	—	—	PTF0	—	—	—	—
44	29	—	PTD4	KBI1_P4	—	—	—
45	30	21	PTD3	KBI1_P3	SPI1_PCS0	—	—
46	31	22	PTD2	KBI1_P2	SPI1_MISO	—	—
47	32	23	PTA3[4]	KBI0_P3	UART0_TX	I2C0_SCL	—
48	33	24	PTA2[4]	KBI0_P2	UART0_RX	I2C0_SDA	—
49	34	25	PTA1	KBI0_P1	FTM0_CH1	ACMP0_IN1	ADC0_SE1
50	35	26	PTA0	KBI0_P0	FTM0_CH0	ACMP0_IN0	ADC0_SE0
51	36	27	PTC7	—	UART1_TX	—	—
52	37	28	PTC6	—	UART1_RX	—	—
53	—	—	PTE3	—	SPI0_PCS0	—	—
54	38	—	PTE2	—	SPI0_MISO	—	—
55	—	—	PTG3	—	—	—	—
56	—	—	PTG2	—	—	—	—
57	—	—	PTG1	—	—	—	—
58	—	—	PTG0	—	—	—	—
59	39	—	PTE1[1]	—	SPI0_MOSI	—	—
60	40	—	PTE0[1]	—	SPI0_SCK	FTM1_CLK	—
61	41	29	PTC5	—	FTM1_CH1	—	RTCO
62	42	30	PTC4	RTCO	FTM1_CH0	ACMP0_IN2	SWD_CLK
63	43	31	PTA5	IRQ	FTM0_CLK	—	$\overline{\text{RESET}}$
64	44	32	PTA4	—	ACMP0_OUT	—	SWD_DIO

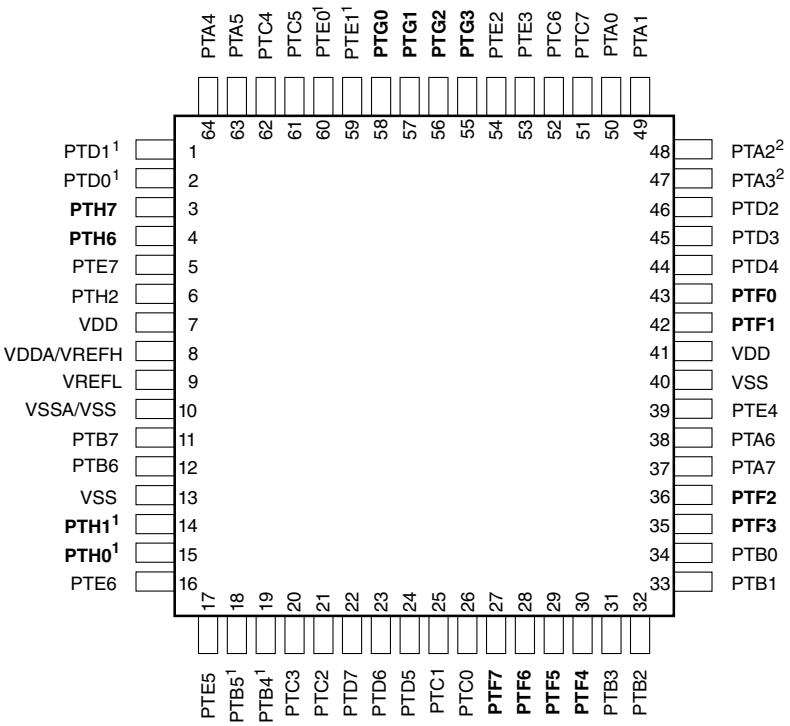
1. This is a high-current drive pin when operated as output.

2. VREFH and VDDA are internally connected.
3. VSSA and VSS are internally connected.
4. This is a true open-drain pin when operated as output.

Note

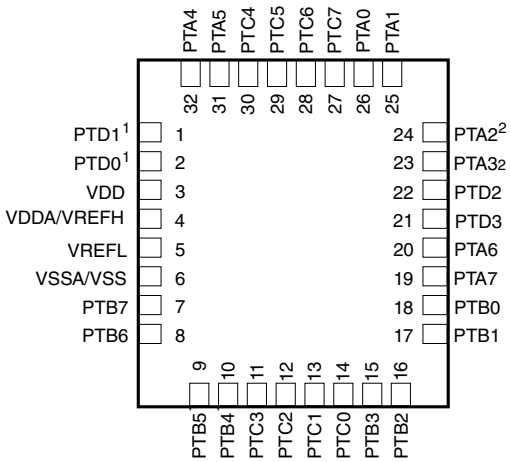
When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear any associated flags before interrupts are enabled. Table 19 illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

8.2 Device pin assignment



Pins in **bold** are not available on less pin-count packages.
1. High source/sink current pins
2. True open drain pins

Figure 21. 64-pin QFP/LQFP packages



1. High source/sink current pins
2. True open drain pins

Figure 24. 32-pin QFN package

9 Revision history

The following table provides a revision history for this document.

Table 20. Revision history

Rev. No.	Date	Substantial Changes
2	3/2014	Initial public release.
3	10/2014	• Added new package of 32-pin QFN information • Updated pin-out • Updated key features of UART, KBI and ADC in the front page • Added a note to the Max. in Supply current characteristics • Updated footnote f_{OSC} = 10 MHz (crystal) in EMC radiated emissions operating behaviors • Added a new section of Thermal operating requirements • Updated NVM specifications • Added reference potential in ADC characteristics • Updated to "All timing assumes high-drive strength is enabled for SPI output pins." in SPI switching specifications
4	07/2016	• Updated the Typical value of E_{TUE} in 12-bit mode and added a note to the 12-bit mode of E_{TUE} and INL in the ADC characteristics.