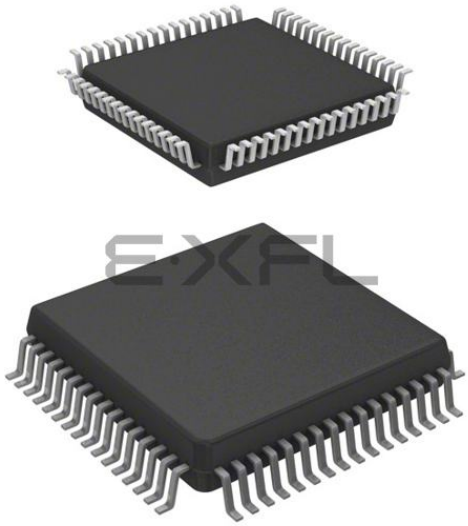

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LVD, PWM, WDT
Number of I/O	57
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x6b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-QFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mke02z64vqh4

4.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Table 2. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	6.0	V
I_{DD}	Maximum current into V_{DD}	—	120	mA
V_{IN}	Input voltage except true open drain pins	–0.3	V_{DD} + 0.3[1]	V
	Input voltage of true open drain pins	–0.3	6	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V

1. Maximum rating of V_{DD} also applies to V_{IN}.

5 General

5.1 Nonswitching electrical specifications

5.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 3. DC characteristics

Symbol	C	Descriptions		Min	Typical[1]	Max	Unit
—	—	Operating voltage	—	2.7	—	5.5	V

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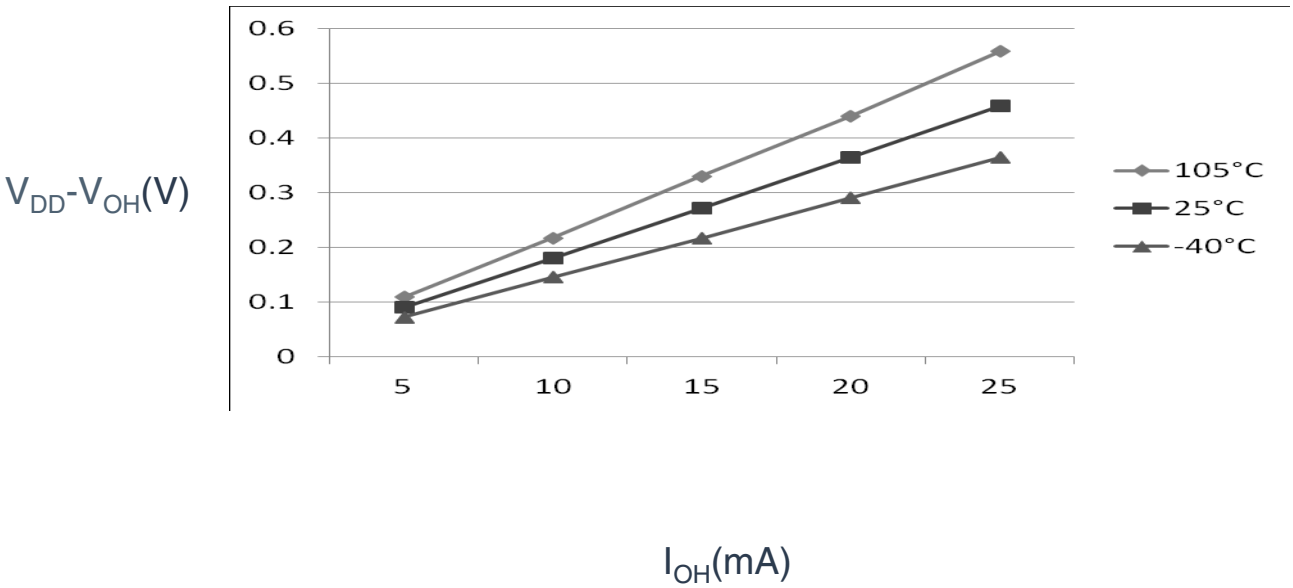


Figure 3. Typical V_{DD}-V_{OH} Vs. I_{OH} (high drive strength) (V_{DD} = 5 V)

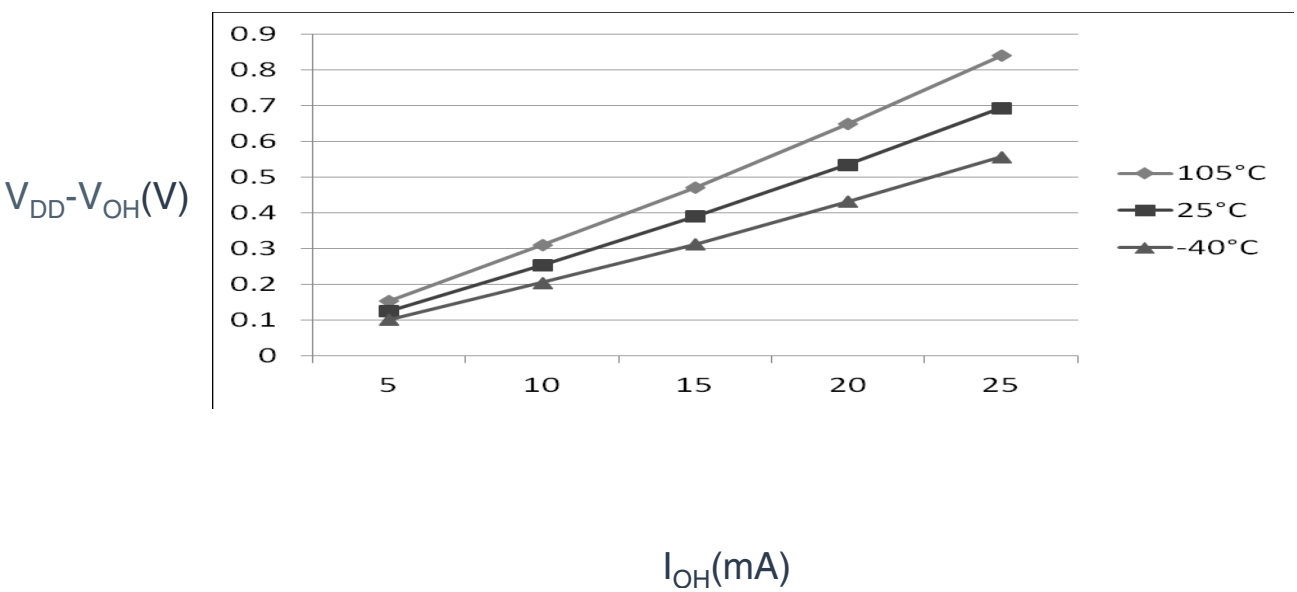


Figure 4. Typical V_{DD}-V_{OH} Vs. I_{OH} (high drive strength) (V_{DD} = 3 V)

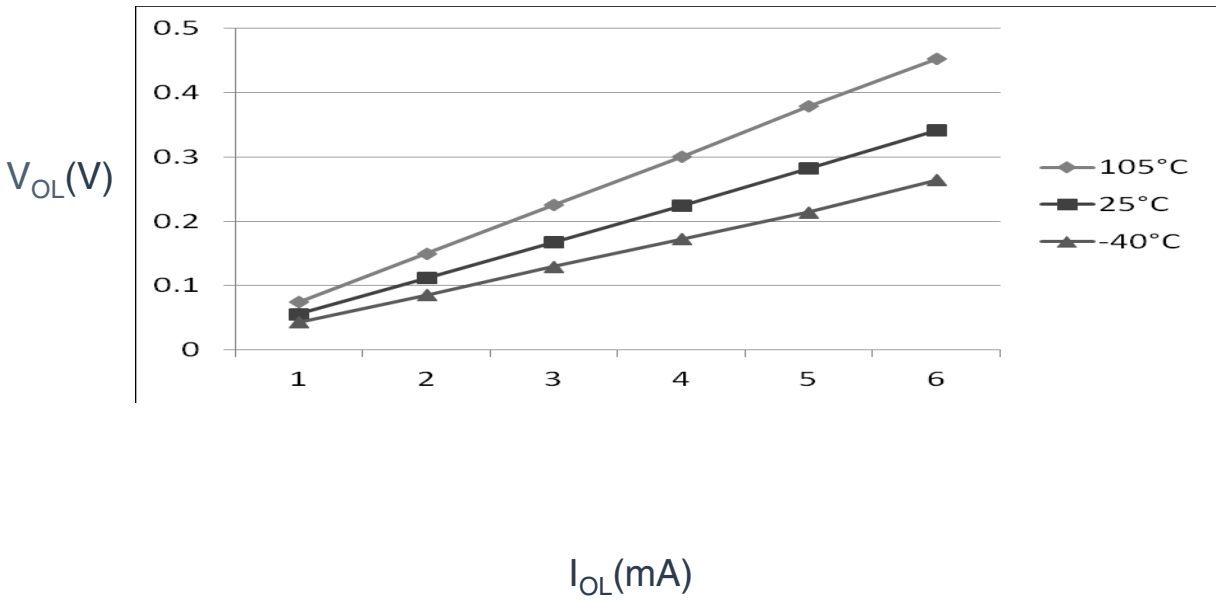


Figure 5. Typical V_{OL} Vs. I_{OL} (standard drive strength) (V_{DD} = 5 V)

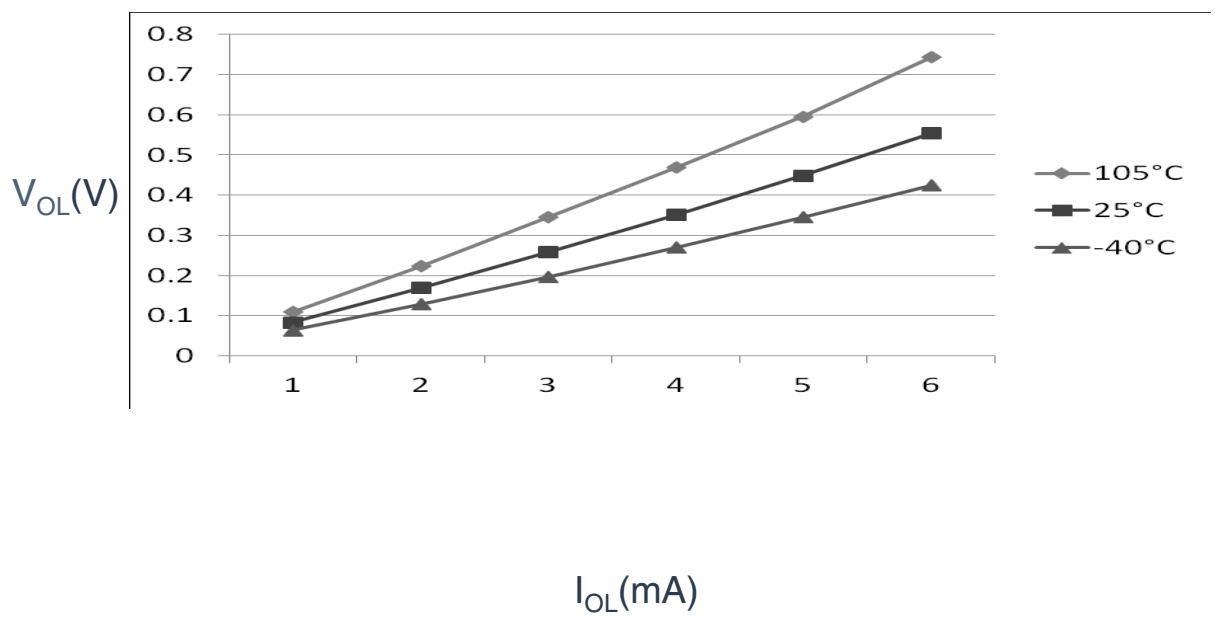


Figure 6. Typical V_{OL} Vs. I_{OL} (standard drive strength) (V_{DD} = 3 V)

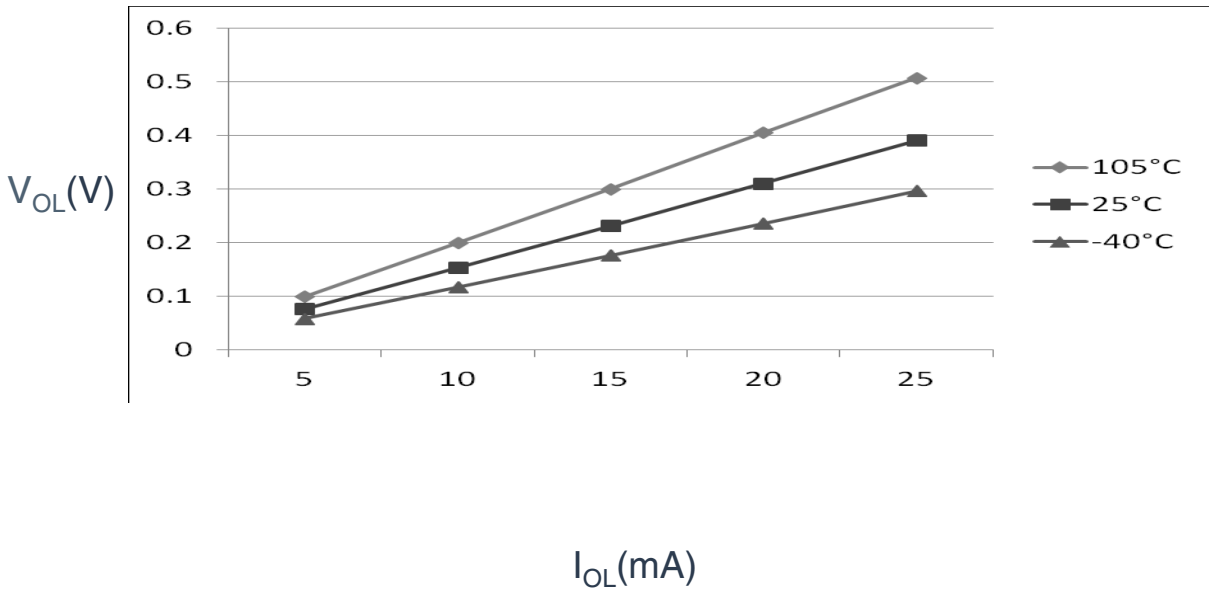


Figure 7. Typical V_{OL} Vs. I_{OL} (high drive strength) (V_{DD} = 5 V)

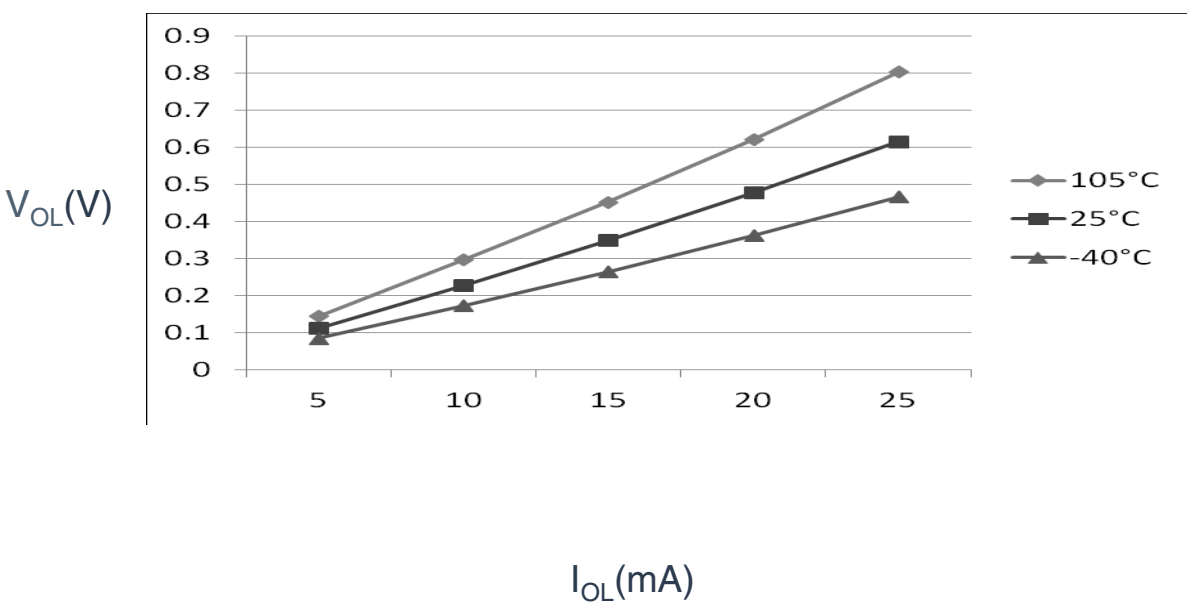


Figure 8. Typical V_{OL} Vs. I_{OL} (high drive strength) (V_{DD} = 3 V)

5.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 5. Supply current characteristics

C	Parameter	Symbol	Core/Bus Freq	V_{DD} (V)	Typical[1]	Max[2]	Unit	Temp
C	Run supply current FEI mode, all modules clocks enabled; run from flash	RI_{DD}	40/20 MHz	5	7.8	—	mA	–40 to 105 °C
C			20/20 MHz		6.7	—		
C			10/10 MHz		4.5	—		
			1/1 MHz		1.5	—		
C			40/20 MHz	3	7.7	—		
C			20/20 MHz		6.6	—		
C			10/10 MHz		4.4	—		
			1/1 MHz		1.45	—		
C	Run supply current FEI mode, all modules clocks disabled; run from flash	RI_{DD}	40/20 MHz	5	6.3	—	mA	–40 to 105 °C
C			20/20 MHz		5.3	—		
C			10/10 MHz		3.7	—		
			1/1 MHz		1.5	—		
C			40/20 MHz	3	6.2	—		
C			20/20 MHz		5.3	—		
C			10/10 MHz		3.7	—		
			1/1 MHz		1.4	—		
C	Run supply current FBE mode, all modules clocks enabled; run from RAM	RI_{DD}	40/20 MHz	5	10.3	—	mA	–40 to 105 °C
P			20/20 MHz		9	14.8		
C			10/10 MHz		5.2	—		
			1/1 MHz		1.45	—		
C			40/20 MHz	3	10.2	—		
P			20/20 MHz		8.8	11.8		
C			10/10 MHz		5.1	—		
			1/1 MHz		1.4	—		
C	Run supply current FBE mode, all modules clocks disabled; run from RAM	RI_{DD}	40/20 MHz	5	8.9	—	mA	–40 to 105 °C
P			20/20 MHz		8	12.3		
C			10/10 MHz		4.4	—		
			1/1 MHz		1.35	—		
C			40/20 MHz	3	8.8	—		
P			20/20 MHz		7.8	9.2		
C			10/10 MHz		4.2	—		
			1/1 MHz		1.3	—		

Table continues on the next page...

Table 5. Supply current characteristics (continued)

C	Parameter	Symbol	Core/Bus Freq	V_{DD} (V)	Typical[1]	Max[2]	Unit	Temp
C	Wait mode current FEI mode, all modules clocks enabled	WI_{DD}	40/20 MHz	5	6.4	—	mA	–40 to 105 °C
P			20/20 MHz		5.5	—		
C			20/10 MHz		3.5	—		
			1/1 MHz		1.4	—		
C			40/20 MHz	3	6.3	—		
C			20/20 MHz		5.4	—		
			10/10 MHz		3.4	—		
			1/1 MHz		1.4	—		
P	Stop mode supply current no clocks active (except 1 kHz LPO clock)[3]	SI_{DD}	—	5	2	85	µA	–40 to 105 °C
P			—	3	1.9	80		–40 to 105 °C
C	ADC adder to Stop ADLPC = 1 ADLSMP = 1 ADCO = 1	—	—	5	86 (64-, 44-pin packages) 42 (32-pin package)	—	µA	–40 to 105 °C
C	MODE = 10B ADICLK = 11B			3	82 (64-, 44-pin packages) 41 (32-pin package)	—		
C	ACMP adder to Stop	—	—	5	12	—	µA	–40 to 105 °C
C				3	12	—		
C	LVD adder to stop[4]	—	—	5	128	—	µA	–40 to 105 °C
C				3	124	—		

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. The Max current is observed at high temperature of 105 °C.
3. RTC adder causes I_{DD} to increase typically by less than 1 µA; RTC clock source is 1 kHz LPO clock.
4. LVD is periodically woken up from Stop by 5% duty cycle. The period is equal to or less than 2 ms.

5.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation play a significant role in EMC performance. The system designer must consult the following applications notes, available on **nxp.com** for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers

- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers
- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

5.1.3.1 EMC radiated emissions operating behaviors

Table 6. EMC radiated emissions operating behaviors for 64-pin QFP package

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	14	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	15	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	3	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	4	dBµV	
V_{RE_IEC}	IEC level	0.15–1000	M	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V_{DD} = 5.0 V, T_A = 25 °C, f_{OSC} = 10 MHz (crystal), f_{BUS} = 20 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

5.2 Switching specifications

5.2.1 Control timing

Table 7. Control timing

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
1	D	System and core clock		f_{Sys}	DC	—	40	MHz
2	P	Bus frequency (t_{cyc} = 1/f_{Bus})		f_{Bus}	DC	—	20	MHz
3	P	Internal low power oscillator frequency		f_{LPO}	0.67	1.0	1.25	KHz
4	D	External reset pulse width[2]		t_{extrst}	1.5 × t_{cyc}	—	—	ns
5	D	Reset low drive		t_{rstdrv}	34 × t_{cyc}	—	—	ns
6	D	IRQ pulse width	Asynchronous path[2]	t_{ILIH}	100	—	—	ns
	D		Synchronous path[3]	t_{IHIL}	1.5 × t_{cyc}	—	—	ns

Table continues on the next page...

Table 7. Control timing (continued)

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
7	D	Keyboard interrupt pulse width	Asynchronous path[2]	t_{ILIH}	100	—	—	ns
	D		Synchronous path	t_{IHIL}	$1.5 \times t_{cyc}$	—	—	ns
8	C	Port rise and fall time - Normal drive strength (load = 50 pF)[4]	—	t_{Rise}	—	10.2	—	ns
	C			t_{Fall}	—	9.5	—	ns
	C	Port rise and fall time - high drive strength (load = 50 pF)[4]	—	t_{Rise}	—	5.4	—	ns
	C			t_{Fall}	—	4.6	—	ns

1. Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a $\overline{\text{RESET}}$ pin request.
3. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.
4. Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range -40 °C to 105 °C.

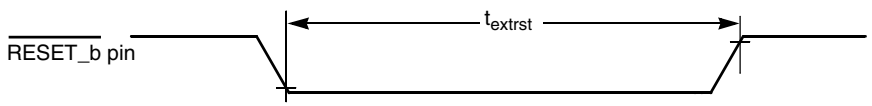


Figure 9. Reset timing

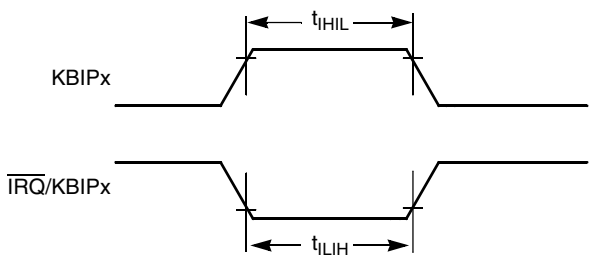


Figure 10. KBIPx timing

5.2.2 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 8. FTM input timing

C	Function	Symbol	Min	Max	Unit
D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
D	External clock period	t_{TCLK}	4	—	t_{cyc}

Table continues on the next page...

Table 8. FTM input timing (continued)

C	Function	Symbol	Min	Max	Unit
D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

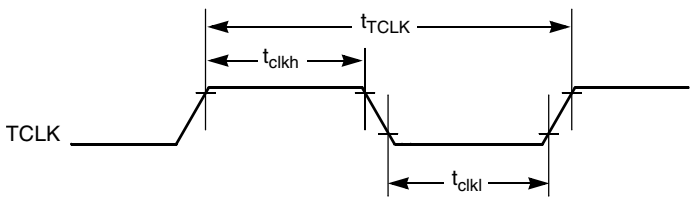


Figure 11. Timer external clock

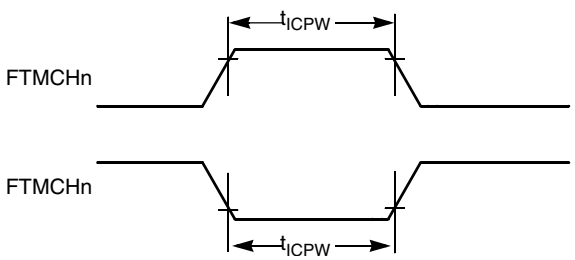


Figure 12. Timer input capture pulse

5.3 Thermal specifications

5.3.1 Thermal operating requirements

Table 9. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is: $T_J = T_A + \theta_{JA}$ x chip power dissipation

5.3.2 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 10. Thermal attributes

Board type	Symbol	Description	64 LQFP	64 QFP	44 LQFP	32 LQFP	32 QFN	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	71	61	75	86	97	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	53	47	53	57	33	°C/W	1, 3
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	59	50	62	72	81	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	46	41	47	51	27	°C/W	1, 3
—	$R_{\theta JB}$	Thermal resistance, junction to board	35	32	34	33	12	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	20	23	20	24	1.3	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	5	8	5	6	3	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts - chip internal power

$P_{I/O}$ = Power dissipation on input and output pins - user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$P_D = K \div (T_J + 273\ °C)$

Solving the equations above for K gives:

$K = P_D \times (T_A + 273\ °C) + \theta_{JA} \times (P_D)^2$

where K is a constant pertaining to the particular part. K can be determined by measuring P_D (at equilibrium) for an known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving the above equations iteratively for any value of T_A.

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 SWD electricals

Table 11. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	5.5	V
J1	SWD_CLK frequency of operation • Serial wire debug	0	20	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	3	—	ns

Table continues on the next page...

Table 12. OSC and ICS specifications (temperature range = -40 to 105 °C ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
14	C	FLL acquisition time[4,6]	$t_{Acquire}$	—	—	2	ms
15	C	Long term jitter of DCO output clock (averaged over 2 ms interval)[7]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. See crystal or resonator manufacturer's recommendation.
3. Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.
4. This parameter is characterized and not tested on each device.
5. Proper PC board layout procedures must be followed to achieve specifications.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

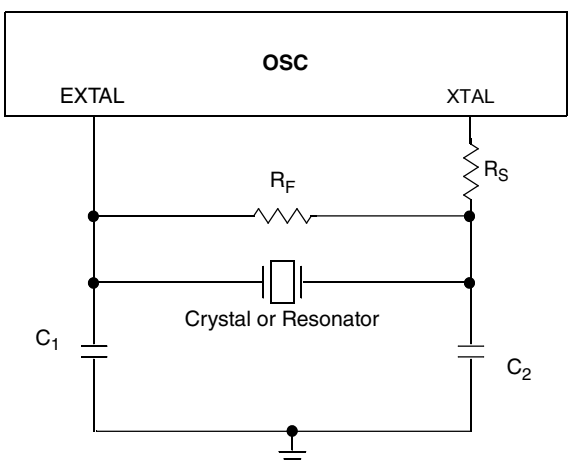


Figure 15. Typical crystal or resonator circuit

6.3 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash and EEPROM memories.

Table 13. Flash and EEPROM characteristics

C	Characteristic	Symbol	Min[1]	Typical[2]	Max[3]	Unit[4]
D	Supply voltage for program/erase –40 °C to 105 °C	$V_{prog/erase}$	2.7	—	5.5	V
D	Supply voltage for read operation	V_{Read}	2.7	—	5.5	V

Table continues on the next page...

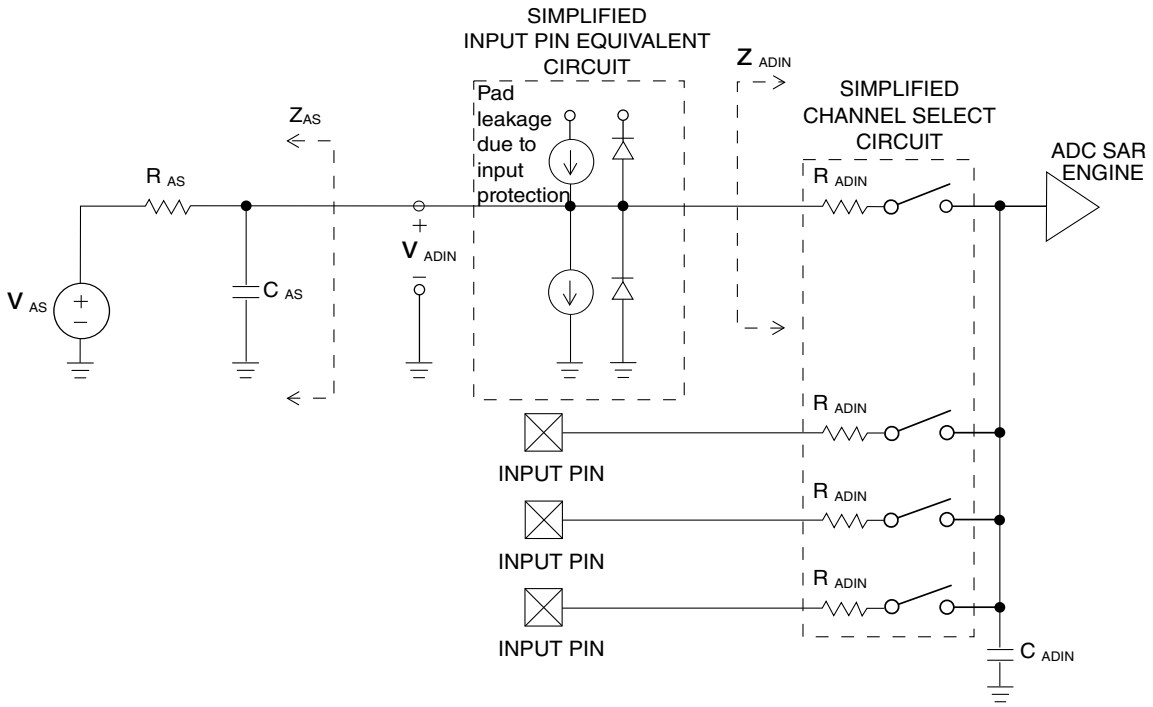


Figure 16. ADC input impedance equivalency diagram

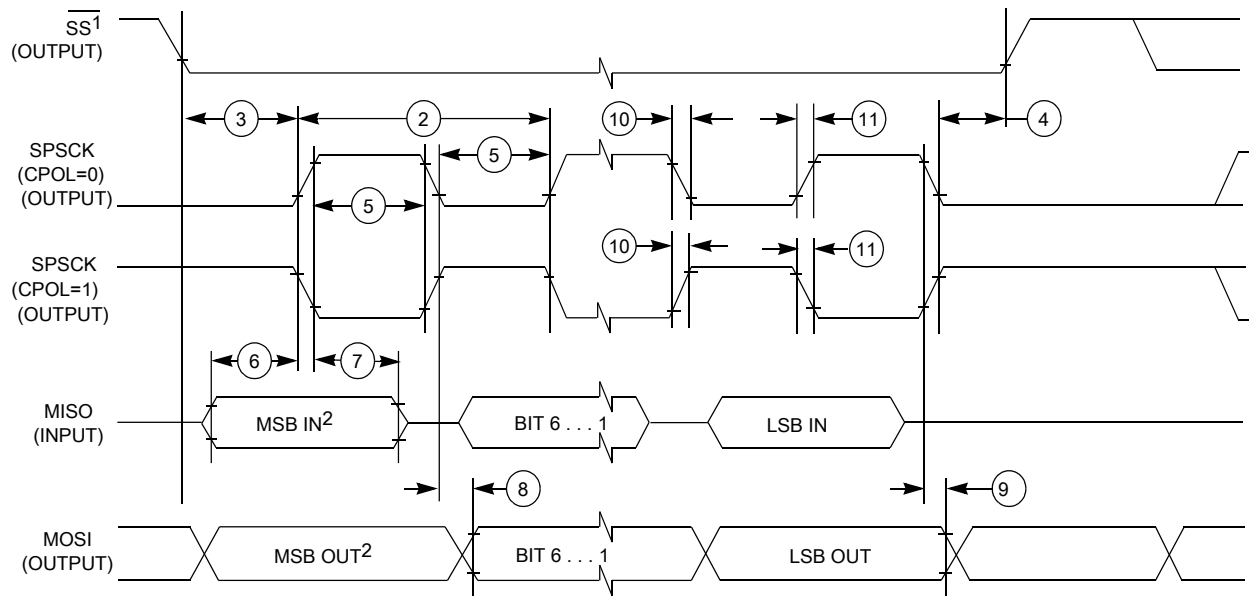
Table 15. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Characteristic	Conditions	C	Symbol	Min	Typ[1]	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	133	—	µA
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	218	—	µA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	327	—	µA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	582	990	µA
Supply current	Stop, reset, module off	T	I_{DDA}	—	0.011	1	µA
ADC asynchronous clock source	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz

Table continues on the next page...

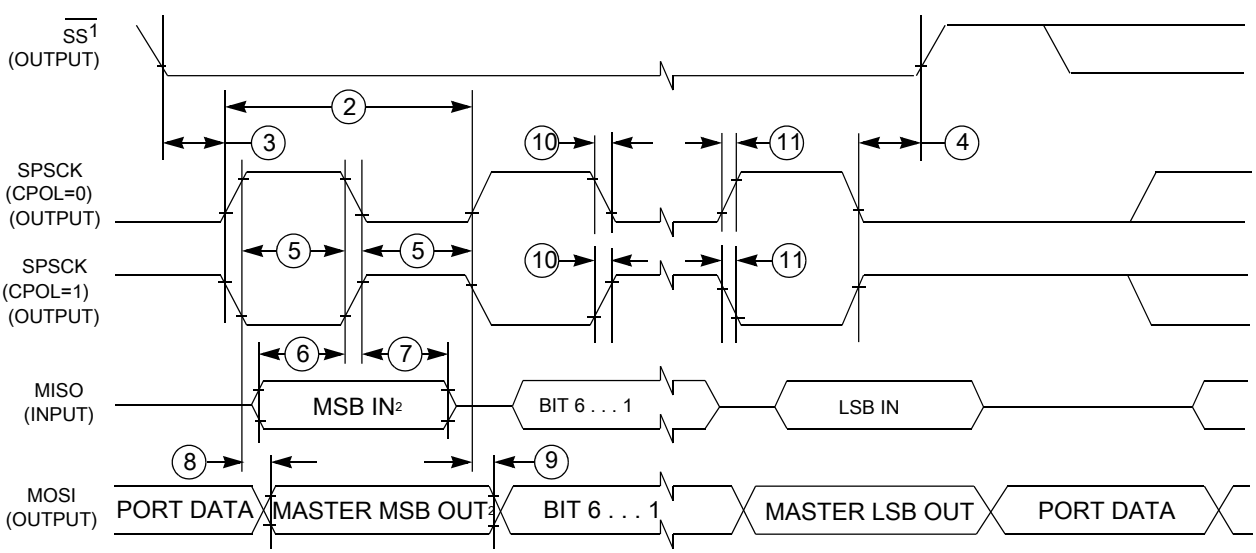
Table 17. SPI master mode timing (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Comment
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 17. SPI master mode timing (CPHA=0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. SPI master mode timing (CPHA=1)

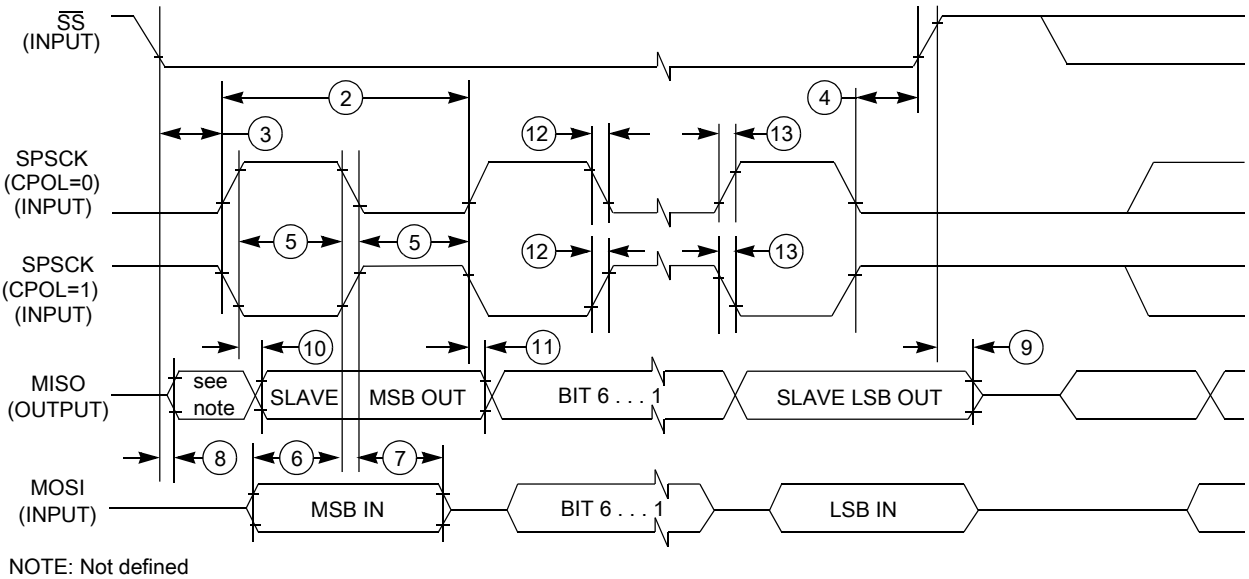


Figure 20. SPI slave mode timing (CPHA=1)

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to **nxp.com** and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
32-pin LQFP	98ASH70029A
32-pin QFN	98ASA00473D
44-pin LQFP	98ASS23225W
64-pin QFP	98ASB42844B
64-pin LQFP	98ASS23234W

8 Pinout

8.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

Table 19. Pin availability by package pin-count

Pin Number			Lowest Priority <-- --> Highest				
64-QFP/ LQFP	44-LQFP	32-LQFP/QFN	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	1	1	PTD1[1]	KBI1_P1	FTM2_CH3	SPI1_MOSI	—
2	2	2	PTD0[1]	KBI1_P0	FTM2_CH2	SPI1_SCK	—
3	—	—	PTH7	—	—	—	—
4	—	—	PTH6	—	—	—	—
5	3	—	PTE7	—	FTM2_CLK	—	FTM1_CH1
6	4	—	PTH2	—	BUSOUT	—	FTM1_CH0
7	5	3	—	—	—	—	VDD
8	6	4	—	—	—	VDDA	VREFH[2]
9	7	5	—	—	—	—	VREFL
10	8	6	—	—	—	VSSA	VSS[3]
11	9	7	PTB7	—	I2C0_SCL	—	EXTAL
12	10	8	PTB6	—	I2C0_SDA	—	XTAL
13	11	—	—	—	—	—	VSS
14	—	—	PTH1[1]	—	FTM2_CH1	—	—
15	—	—	PTH0[1]	—	FTM2_CH0	—	—
16	—	—	PTE6	—	—	—	—
17	—	—	PTE5	—	—	—	—
18	12	9	PTB5[1]	FTM2_CH5	SPI0_PCS0	ACMP1_OUT	—
19	13	10	PTB4[1]	FTM2_CH4	SPI0_MISO	$\overline{\text{NMI}}$	ACMP1_IN2
20	14	11	PTC3	FTM2_CH3	—	—	ADC0_SE11
21	15	12	PTC2	FTM2_CH2	—	—	ADC0_SE10
22	16	—	PTD7	KBI1_P7	UART2_TX	—	—
23	17	—	PTD6	KBI1_P6	UART2_RX	—	—
24	18	—	PTD5	KBI1_P5	—	—	—
25	19	13	PTC1	—	FTM2_CH1	—	ADC0_SE9
26	20	14	PTC0	—	FTM2_CH0	—	ADC0_SE8
27	—	—	PTF7	—	—	—	ADC0_SE15

Table continues on the next page...

Table 19. Pin availability by package pin-count (continued)

Pin Number			Lowest Priority <-- --> Highest				
64-QFP/ LQFP	44-LQFP	32-LQFP/QFN	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
28	—	—	PTF6	—	—	—	ADC0_SE14
29	—	—	PTF5	—	—	—	ADC0_SE13
30	—	—	PTF4	—	—	—	ADC0_SE12
31	21	15	PTB3	KBI0_P7	SPI0_MOSI	FTM0_CH1	ADC0_SE7
32	22	16	PTB2	KBI0_P6	SPI0_SCK	FTM0_CH0	ADC0_SE6
33	23	17	PTB1	KBI0_P5	UART0_TX	—	ADC0_SE5
34	24	18	PTB0	KBI0_P4	UART0_RX	—	ADC0_SE4
35	—	—	PTF3	—	—	—	—
36	—	—	PTF2	—	—	—	—
37	25	19	PTA7	—	FTM2_FLT2	ACMP1_IN1	ADC0_SE3
38	26	20	PTA6	—	FTM2_FLT1	ACMP1_IN0	ADC0_SE2
39	—	—	PTE4	—	—	—	—
40	27	—	—	—	—	—	VSS
41	28	—	—	—	—	—	VDD
42	—	—	PTF1	—	—	—	—
43	—	—	PTF0	—	—	—	—
44	29	—	PTD4	KBI1_P4	—	—	—
45	30	21	PTD3	KBI1_P3	SPI1_PCS0	—	—
46	31	22	PTD2	KBI1_P2	SPI1_MISO	—	—
47	32	23	PTA3[4]	KBI0_P3	UART0_TX	I2C0_SCL	—
48	33	24	PTA2[4]	KBI0_P2	UART0_RX	I2C0_SDA	—
49	34	25	PTA1	KBI0_P1	FTM0_CH1	ACMP0_IN1	ADC0_SE1
50	35	26	PTA0	KBI0_P0	FTM0_CH0	ACMP0_IN0	ADC0_SE0
51	36	27	PTC7	—	UART1_TX	—	—
52	37	28	PTC6	—	UART1_RX	—	—
53	—	—	PTE3	—	SPI0_PCS0	—	—
54	38	—	PTE2	—	SPI0_MISO	—	—
55	—	—	PTG3	—	—	—	—
56	—	—	PTG2	—	—	—	—
57	—	—	PTG1	—	—	—	—
58	—	—	PTG0	—	—	—	—
59	39	—	PTE1[1]	—	SPI0_MOSI	—	—
60	40	—	PTE0[1]	—	SPI0_SCK	FTM1_CLK	—
61	41	29	PTC5	—	FTM1_CH1	—	RTCO
62	42	30	PTC4	RTCO	FTM1_CH0	ACMP0_IN2	SWD_CLK
63	43	31	PTA5	IRQ	FTM0_CLK	—	$\overline{\text{RESET}}$
64	44	32	PTA4	—	ACMP0_OUT	—	SWD_DIO

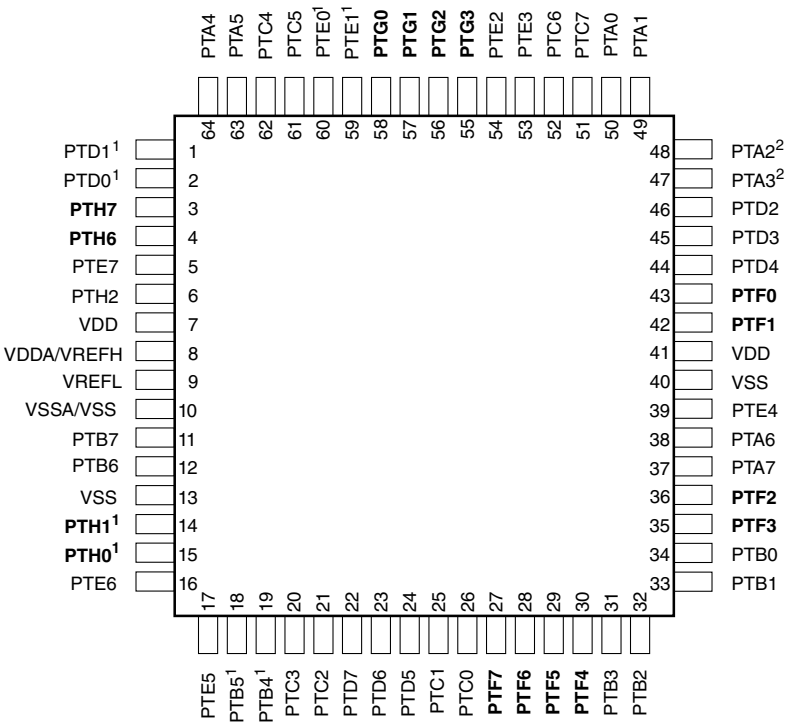
1. This is a high-current drive pin when operated as output.

2. VREFH and VDDA are internally connected.
3. VSSA and VSS are internally connected.
4. This is a true open-drain pin when operated as output.

Note

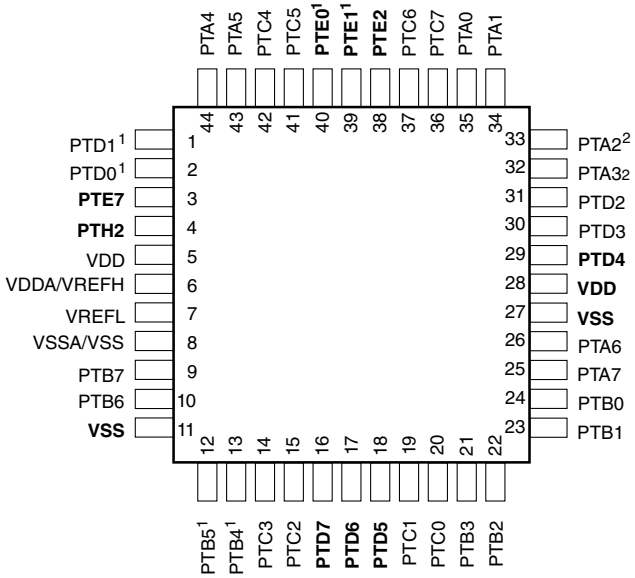
When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear any associated flags before interrupts are enabled. Table 19 illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

8.2 Device pin assignment



Pins in **bold** are not available on less pin-count packages.
1. High source/sink current pins
2. True open drain pins

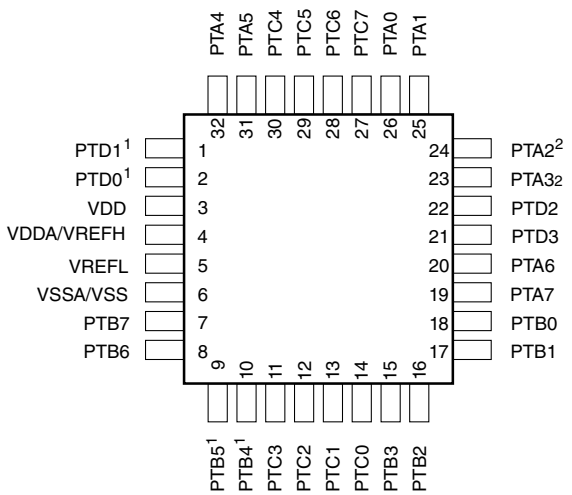
Figure 21. 64-pin QFP/LQFP packages



Pins in **bold** are not available on less pin-count packages.

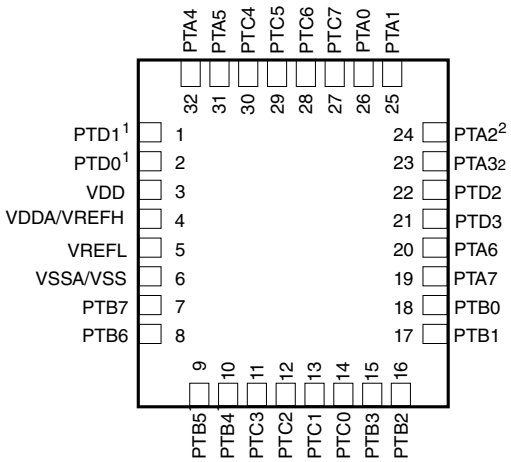
1. High source/sink current pins
2. True open drain pins

Figure 22. 44-pin LQFP package



1. High source/sink current pins
2. True open drain pins

Figure 23. 32-pin LQFP package



1. High source/sink current pins
2. True open drain pins

Figure 24. 32-pin QFN package

9 Revision history

The following table provides a revision history for this document.

Table 20. Revision history

Rev. No.	Date	Substantial Changes
2	3/2014	Initial public release.
3	10/2014	• Added new package of 32-pin QFN information • Updated pin-out • Updated key features of UART, KBI and ADC in the front page • Added a note to the Max. in Supply current characteristics • Updated footnote f_{OSC} = 10 MHz (crystal) in EMC radiated emissions operating behaviors • Added a new section of Thermal operating requirements • Updated NVM specifications • Added reference potential in ADC characteristics • Updated to "All timing assumes high-drive strength is enabled for SPI output pins." in SPI switching specifications
4	07/2016	• Updated the Typical value of E_{TUE} in 12-bit mode and added a note to the 12-bit mode of E_{TUE} and INL in the ADC characteristics.