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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS-I
Number of Cores/Bus Width	1 Core, 64-Bit
Speed	175MHz
Co-Processors/DSP	System Control; CP0
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 85°C (TC)
Security Features	-
Package / Case	208-BFQFP Exposed Pad
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79rv4700-175dp

This data sheet provides an overview of the R4700's CPU features and architecture. A more detailed description of this processor is provided in the *IDT79R4700 RISC Processor Hardware User's Manual*, available from Integrated Device Technology (IDT). Information on development support, applications notes and complementary products is available on the IDT Web site **www.idt.com** or through your local IDT sales representative.

Note: Throughout this data sheet and any other IDT materials for this device, the R4700 indicates a 5V part; RV4700 designates a reduced voltage (3V) part; and the RC4700 reflects either.

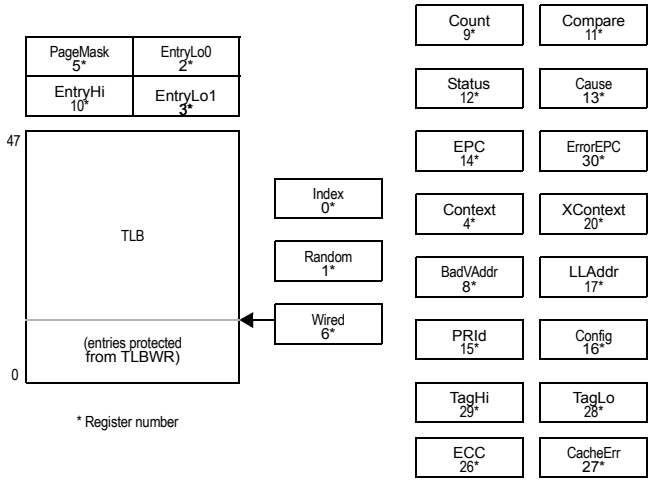


Figure 1 The RC4700 CPO Registers

Hardware Overview

The RC4700 processor family brings a high-level of integration designed for high-performance computing. The R4700's key elements are briefly described below. A more detailed explanation of each subsystem is available in the user's manual.

Pipeline

The RC4700 uses a simple 5-stage pipeline, similar to the pipeline structure implemented in the IDT79R32364. This pipeline's simplicity allows the RC4700 to be lower cost and lower power than super-scalar or super-pipelined processors. The pipeline stages are shown in Figure 3 on page 3.

Integer Execution Engine

The R4700 implements the MIPS-III Instruction Set architecture and is upwardly compatible with applications that run on earlier generation parts.

Implementation of the MIPS-III architecture results in 64-bit operations, better code density, greater multi-processing support, improved performance for commonly used code sequences in operating system kernels and faster execution of floating-point intensive applications. All resource dependencies are made transparent to the programmer, insuring transportability among implementations of the MIPS instruction set architecture.

The MIPS integer unit implements a load/store architecture with single cycle ALU operations (logical, shift, add, sub) and an autonomous multiply/divide unit. Register resources include:

- **32 general-purpose orthogonal integer registers**
- **HI/LO result registers, for the integer multiply/divide unit**
- **Program counter**

Also, the on-chip floating-point co-processor adds 32 floating-point registers and a floating-point control/status register.

Register File

The R4700 has 32 general-purpose registers (shown in Figure 2). These registers are used for scalar integer operations and address calculation. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

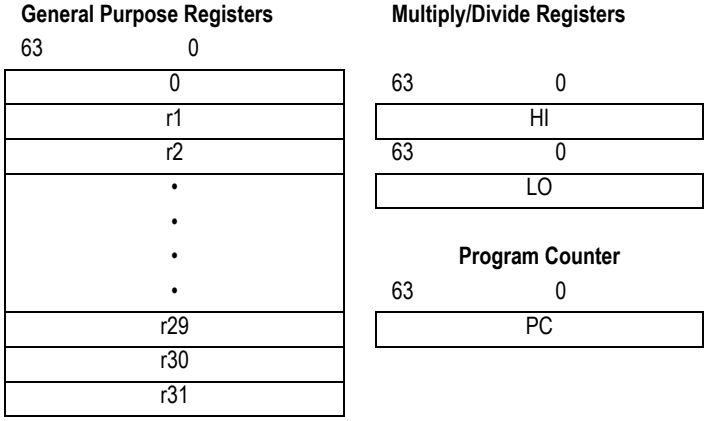


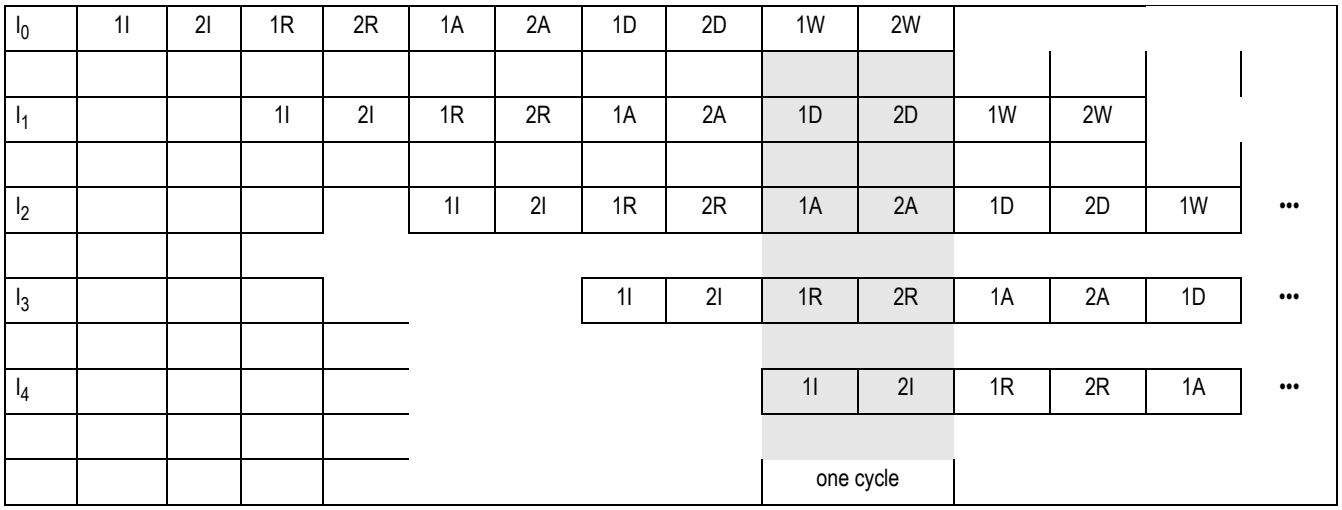
Figure 2 R4700 CPU Registers

ALU

The RC4700 ALU consists of the integer adder and logic unit. The adder performs address calculations in addition to arithmetic operations, and the logic unit performs all logical and shift operations. Each of these units is highly optimized and can perform an operation in a single pipeline cycle.

Integer Multiply/Divide

To perform integer multiply and divide operations, the RC4700 uses the floating-point unit. The results of the operation are placed in the *HI* and *LO* registers. The values can then be transferred to the general purpose register file using the MFHI/MFLO instructions. To prevent the



Key to Figure

1I-1R	Instruction cache access
2I	Instruction virtual-to-physical address translation in ITLB
2A-2D	Data cache access and load align
1D	Data virtual-to-physical address translation in DTLB
1D-2D	Virtual-to-physical address translation in JTLB
2R	Register file read
2R	Bypass calculation
2R	Instruction decode
2R	Branch address calculation
1A	Issue or slip decision
1A-2A	Integer add, logical, shift
1A	Data virtual address calculation
2A	Store align
1A	Branch decision
2W	Register file write

Figure 3 RC4700 Pipeline Stages

occurrence of an interlock or stall, a required number of processor internal cycles must occur between an integer multiply or divide and a subsequent MFHI or MFLO operation.

Operation	32-bit	64-bit
MULT	6 - 9	7 - 10
DIV	42	74

Floating-Point Co-Processor

The RC4700 incorporates a complete floating-point co-processor on chip and includes a floating-point register file and execution units. The floating-point co-processor forms a “seamless” interface with the integer unit, decoding and executing instructions in parallel with the integer unit.

Floating-Point Units

The RC4700 floating-point execution units support single and double precision arithmetic, as specified in the IEEE Standard 754. The execution unit is separated into a multiply unit and a combined add/convert/divide/square root unit. Overlap of multiplies and add/subtract is supported. The multiplier is partially pipelined, allowing a new multiply to begin every four cycles.

The RC4700 maintains fully precise floating-point exceptions while allowing both overlapped and pipelined operations. Precise exceptions are extremely important in mission-critical environments and highly desirable for debugging in any environment.

The floating-point unit operation’s set includes floating-point add, subtract, multiply, divide, square root, conversion between fixed-point and floating-point format, conversion among floating-point formats and floating-point compare. These operations comply with the IEEE Standard 754.

Table 1 lists the latencies of some of the floating-point instructions in internal processor cycles. Note that multiplies are pipelined so that a new multiply can be initiated every four pipeline cycles

Floating-Point General Register File

The floating-point register file is made up of thirty-two 64-bit registers. With the LDC1 and SDC1 instructions the floating-point unit can take advantage of the 64-bit wide data cache and issue a co-processor load or store doubleword instruction in every cycle.

The floating-point control register space contains two registers: one for determining configuration and revision information for the coprocessor and one for control and status information. These are primarily involved with diagnostic software, exception handling, state saving and restoring, and control of rounding modes.

Operation	Single Precision	Double Precision
ADD	4	4
SUB	4	4
MUL	4	5
DIV	32	61
SQRT	31	60
CMP	3	3
FIX	4	4
FLOAT	6	6
ABS	1	1
MOV	1	1
NEG	1	1
LWC1, LDC1	2	2
SWC1, SDC1	1	1

Table 1 RC4700 Instruction Latencies

System Control Co-processor (CP0)

The system control co-processor in the MIPS architecture is responsible for the virtual memory sub-system, the exception control system and the diagnostics capability of the processor. In the MIPS architecture, the system control co-processor (and thus the kernel software) is implementation dependent.

System Control Co-Processor Registers

The RC4700 incorporates all system control co-processor (CP0) registers, on-chip. These registers (shown in Figure 1 on page 2) provide the path through which the virtual memory system’s page mapping is examined and changed, exceptions are handled and operating modes are controlled (kernel vs. user mode, interrupts enabled or disabled, cache features). In addition, to aid in cache diagnostic testing and assist in data error detection, the RC4700 includes registers to implement a real-time cycle counting facility.

Virtual-to-Physical Address Mapping

To establish a secure environment for user processing, the RC4700 provides the user, supervisor, and kernel modes of virtual addressing, available to system software. Bits in a status register determine which virtual addressing mode is used.

While in user mode, the RC4700 provides a single, uniform virtual address space of 256GB (2GB for 32-bit address mode). When operating in the kernel mode, four distinct virtual address spaces—totalling 1024GB (4GB in 32-bit address mode)—are simultaneously available and are differentiated by the high-order bits of the virtual address.

The RC4700 processor also supports a supervisor mode in which the virtual address space is 256.5GB (2.5GB in 32-bit address mode), divided into three regions that are based on the high-order bits of the virtual address. If the RC4700 is configured for 64-bit virtual addressing, the virtual address space layout is an upwardly compatible extension of the 32-bit virtual address space layout. Figure 4 on page 5 shows the address space layout for the 32-bit virtual address operation.

Memory Management Unit (MMU)

The Memory management unit controls the virtual memory system page mapping. It consists of an instruction address translation buffer (the ITLB), a data address translation buffer (the DTLB), a Joint TLB (the JTLB), and co-processor registers used for the virtual memory mapping sub-system.

Instruction TLB (ITLB)

The RC4700 also incorporates a two-entry instruction TLB. Each entry maps a 4KB page. The instruction TLB improves performance by allowing instruction address translation to occur in parallel with data address translation. When a miss occurs on an instruction address translation, the least-recently used ITLB entry is filled from the JTLB. The operation of the ITLB is invisible to the user.

Data TLB (DTLB)

The RC4700 also incorporates a four-entry data TLB. Each entry maps a 4KB page. The data TLB improves performance by allowing data address translation to occur in parallel with instruction address translation. When a miss occurs on a data address translation, the DTLB is filled from the JTLB. The DTLB refill is pseudo-LRU: the least recently used entry of the least recently used half is filled. The operation of the DTLB is invisible to the user.

Joint TLB (JTLB)

For fast virtual-to-physical address decoding, the RC4700 uses a large, fully associative TLB that maps 96 virtual pages to their corresponding physical addresses. The TLB is organized as 48 pairs of even-odd entries and maps a virtual address and address space identifier into the large, 64GB physical address space.

Two mechanisms are provided to assist in controlling the amount of mapped space and the replacement characteristics of various memory regions. First, the page size can be configured, on a per-entry basis, to map a page size of 4KB to 16MB (in multiples of 4). A CP0 register is loaded with the page size of a mapping, and that size is entered into the TLB when a new entry is written. Thus, operating systems can provide special purpose maps; for example, a typical frame buffer can be memory mapped using only one TLB entry.

The second mechanism controls the replacement algorithm, when a TLB miss occurs. The RC4700 provides a random replacement algorithm to select a TLB entry to be written with a new mapping; however, the processor provides a mechanism whereby a system specific number of mappings can be locked into the TLB and avoid being randomly replaced. This facilitates the design of real-time systems, by allowing deterministic access to critical software.

The joint TLB also contains information to control the cache coherency protocol for each page. Specifically, each page has attribute bits to determine whether the coherency algorithm is uncached, non-coherent write-back, non-coherent write-through write-allocate or non-coherent write-through no write-allocate. Non-coherent write-back is typically used for both code and data on the RC4700; however, hardware-based cache coherency is not supported.

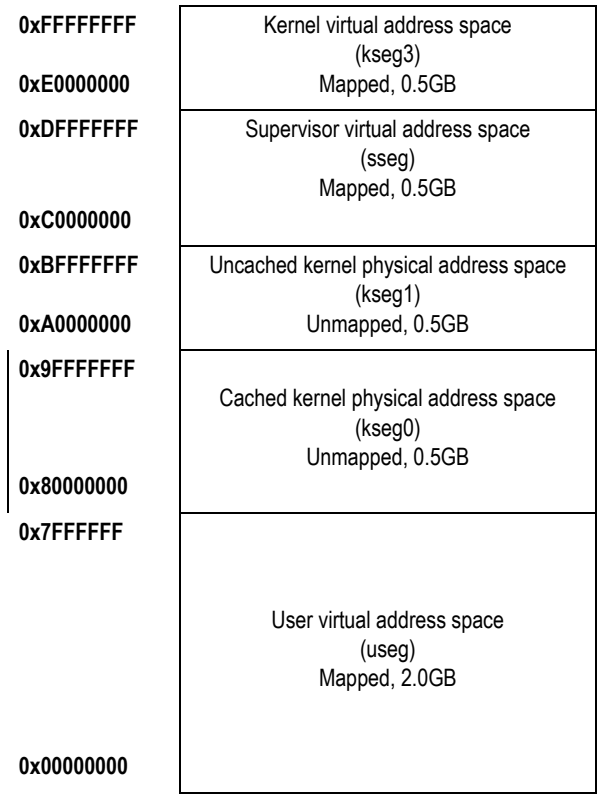


Figure 4 Kernel Mode Virtual Addressing (32-bit Mode)

Cache Memory

To keep the RC4700's high-performance pipeline full and operating efficiently, the RC4700 incorporates on-chip instruction and data caches that can be accessed in a single processor cycle. Each cache has its own 64-bit data path and can be accessed in parallel.

Instruction Cache

The RC4700 incorporates a two-way set associative on-chip instruction cache. This virtually indexed, physically tagged cache is 16KB in size and is protected with word parity.

ValidOut* and ValidIn* are used by the RC4700 and the external device respectively to indicate that there is a valid command or data on the SysAD and SysCmd buses. The RC4700 asserts ValidOut* when it is driving these buses with a valid command or data, and the external device drives ValidIn* when it has control of the buses and is driving a valid command or data.

Non-overlapping System Interface

The RC4700 bus uses a non-overlapping system interface. This means that only one processor request may be outstanding at a time and that the request must be serviced by an external device before the RC4700 issues another request. The RC4700 can issue read and write requests to an external device, and an external device can issue read and write requests to the RC4700.

For processor read transaction the RC4700 asserts ValidOut* and simultaneously drives the address and read command on the SysAD and SysCmd buses. If the system interface has RdRdy* asserted, then the processor tristates its drivers and releases the system interface to slave state by asserting Release*. The external device can then begin sending the data.

Figure 5 on page 10 shows a processor block read request and the external agent read response. The read latency is four cycles (ValidOut* to ValidIn*), and the response data pattern is DDxxDD. Figure 6 on page 10 shows a processor block write.

Write Reissue and Pipeline Write

The RC4700 implements additional write protocols that have been designed to improve performance. This implementation doubles the effective write bandwidth. The write re-issue has a high repeat rate of two cycles per write. A write issues if WrRdy* is asserted two cycles earlier and is still asserted at the issue cycle. If it is not still asserted, the last write re-issues again. Pipelined writes have the same two cycle per write repeat rate but can issue one additional write after WrRdy* de-asserts. They still follow the issue rule as R4x00 mode for other writes.

External Requests

The RC4700 responds to requests issued by an external device. The requests can take several forms. An external device may need to supply data in response to an RC4700 read request or it may need to gain control over the system interface bus to access other resources which may be on that bus. It also may issue requests to the processor, such as a request for the RC4700 to write to the RC4700 interrupt register. The RC4700 supports Write, Null, and Read Response external requests.

Boot-Time Options

Fundamental operational modes for the processor are initialized by the boot-time mode control interface. The boot-time mode control interface is a serial interface operating at a very low frequency (MasterClock divided by 256). The low-frequency operation allows the initialization information to be kept in a low-cost serial EEPROM; alternatively, the 20-or-so bits could be generated by the system interface ASIC or a simple PAL.

Immediately after the V_{CCOK} signal is asserted, the processor reads a bit stream of 256 bits to initialize all fundamental operational modes. After initialization is complete, the processor continues to drive the serial clock output, but no further initialization bits are read.

JTAG Interface

The RC4700 supports the JTAG interface pins, with the serial input connected to serial output. Boundary scan is not supported.

Boot-Time Modes

The boot-time serial mode stream is defined in Table 3. Bit 0 is the first bit presented to the processor when V_{CCOK} is asserted; bit 255 is the last.

Power Management[1]

CP0 is also used to control the power management for the RC4700. This is the standby mode and can be used to reduce the power consumption of the internal core of the CPU. Standby mode is entered by executing the WAIT instruction with the SysAD bus idle and is exited by an interrupt.

Standby Mode Operations

The RC4700 provides a means to reduce the amount of power consumed by the internal core when the CPU would otherwise not be performing any useful operations. This is known as “Standby Mode.”

Entering Standby Mode

Executing the WAIT instruction enables interrupts and enters Standby mode. When the WAIT instruction finishes the W pipe-stage, if the SysAd bus is currently idle, the internal clocks will shut down, thus freezing the pipeline. The PLL, internal timer, some of the input pin clocks (Int[5:0]*, NMI*, ExtReq*, Reset*, and ColdReset*), and the output clocks—TClock[1:0], RClock[1:0] SyncOut, Modeclock and MasterOut—will continue to run. If the conditions are not correct when the WAIT instruction finishes the W pipe-stage (such as the SysAd bus is not idle), the WAIT is treated as a NOP.

Once the CPU is in Standby Mode, any interrupt— including the internally generated timer interrupt—will cause the CPU to exit Standby Mode.

1. The R4700 implements advanced power management, to substantially reduce the average power dissipation of the device. This operation is described in the *R4700 Microprocessor Hardware User’s Manual*.

Thermal Considerations

The RC4700 uses special packaging techniques to improve the thermal properties of high-speed processors. The RC4700 is packaged using cavity down packaging in a 179-pin PGA package, and a 208-lead QFP package. These packages effectively dissipate the power of the CPU, increasing device reliability.

The R4700 is guaranteed in a case temperature range of 0° to +85° C. The type of package, speed (power) of the device, and airflow conditions affect the equivalent ambient temperature conditions that will meet this specification.

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient ($\varnothing_{CA}$) of the given package. The following equation relates ambient and case temperatures:

$T_A = T_C - P * \varnothing_{CA}$

where P is the maximum power consumption at hot temperature, calculated by using the maximum I_{CC} specification for the device.

Typical values for $\varnothing_{CA}$ at various airflows are shown in Table 2:.

	$\varnothing_{CA}$					
Airflow (ft/min)	0	200	400	600	800	1000
PGA	16	7	5	3	2.5	2
QFP	21	13	10	9	8	7

Table 2: Thermal Resistance ($\varnothing_{CA}$) at Various Airflows

Revision History

January 1996: Initial draft.

March 1997: Deleted data on 150MHz speed for 5V part only.

August 1997: Upgraded 80 to 175 MHz speed specs from “Preliminary” to “Final.”

June 1999: Upgraded speed to 200MHz on 3V part specs. Package change to DP.

June 29, 2000: Added back 175 and 200 MHz speeds.

April 10, 2001: In the Data Output category of the System Interface Parameters tables, changed values in the Min column for all speeds from 1.0 to 0.

December 5, 2008: Removed IDT from ordering codes on Ordering Information page.

Mode bit	Description	Mode bit	Description
0	reserved (must be zero)	14:13	Output driver strength 10 → 100% strength (fastest), 11 → 83% strength, 00 → 67% strength, 01 → 50% strength (slowest)
4:1	Writeback data rate 0 → Δ, 1 → DDx, 2 → DDxx, 3 → DxDx, 4 → DDxxx, 5 → DDxxxx, 6 → DxxDxx, 7 → DDxxxxxx, 8 → DxxxDxxx, 9-→ reserved	bit 15	0 → TClock[0] enabled 1 → TClock[0] disabled
7:5	Clock divisor 0 → 2, 1 → 3, 2 → 4, 3 → 5, 4 → 6, 5 → 7, 6 → 8, 7 reserved	bit 16	0 → TClock[1] enabled 1 → TClock[1] disabled
8	0 → Little endian, 1 → Big endian	bit 17	0 →RClock[0] enabled 1 → RClock[0] disabled
10:9	00 → R4000 compatible, 01 → reserved, 10 → pipelined writes, 11 → write re-issue	bit 18	0 → RClock[1] enabled 1 →RClock[1] disabled
11	Disable the timer interrupt on Int[5]. 0 → Enabled 1 → Disabled	255:19	Reserved (must be zero)
12	reserved (must be zero)		

Table 3 Boot-time Serial Mode Stream

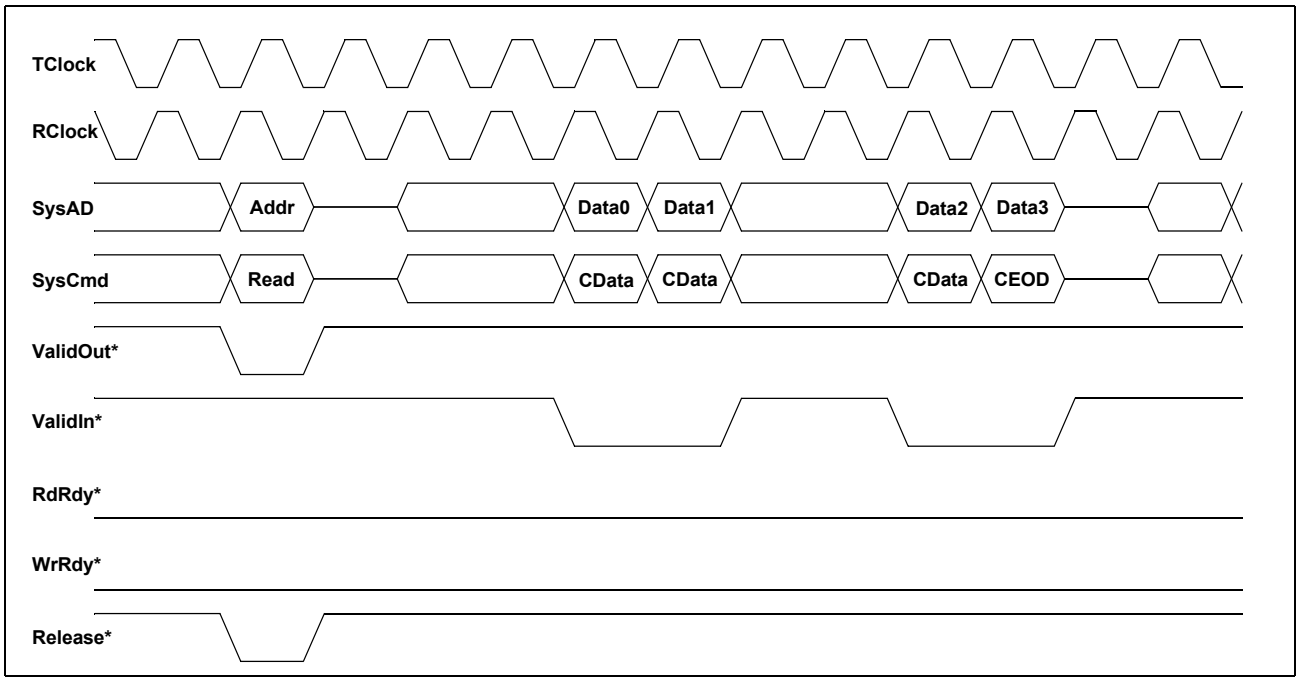


Figure 5 Processor Block Read

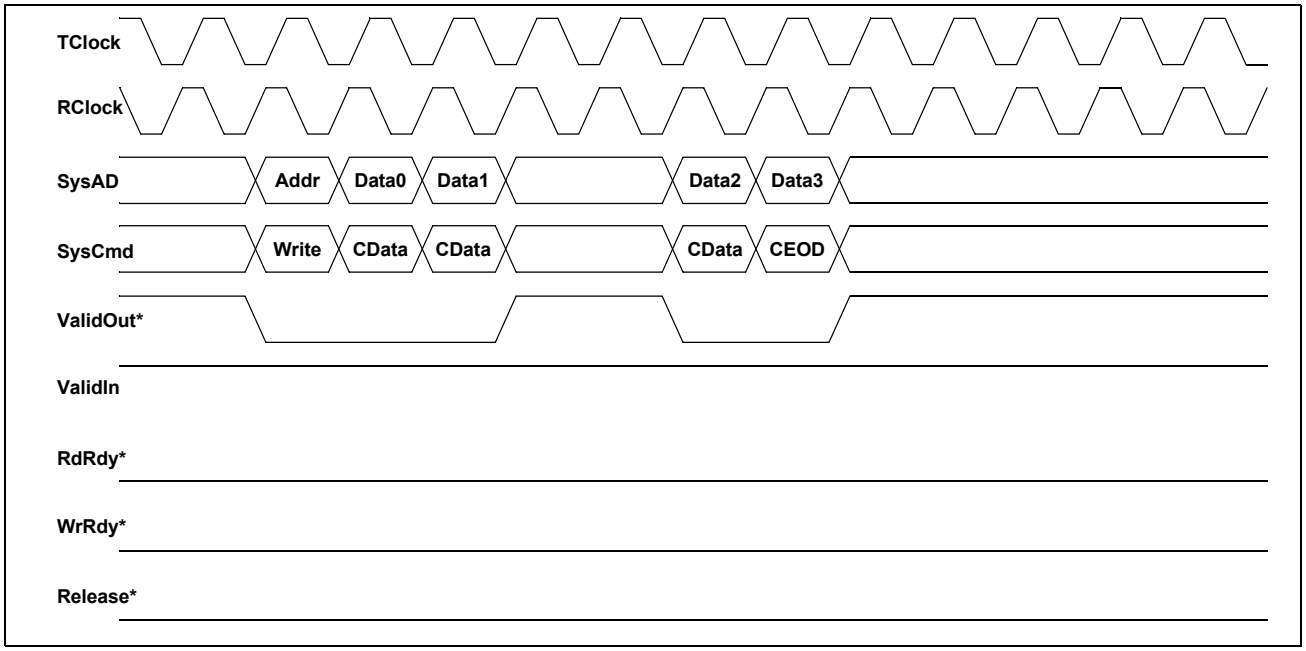


Figure 6 Processor Block Write

Pin Description

The table below provides a list of interface, interrupt and miscellaneous pins that are available on the RC4700. Note that signals marked with an asterisk are active when low. Boundary scan is not supported.

Pin Name	Type	Description
System Interface		
ExtRqst*	I	**External request** Signals that the system interface needs to submit an external request.
Release*	O	**Release interface** Signals that the processor is releasing the system interface to slave state.
RdRdy*	I	**Read Ready** Signals that an external agent can now accept a processor read.
WrRdy*	I	**Write Ready** Signals that an external agent can now accept a processor write request.
ValidIn*	I	**Valid Input** Signals that an external agent is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
ValidOut*	O	**Valid output** Signals that the processor is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
SysAD(63:0)	I/O	**System address/data bus** A 64-bit address and data bus for communication between the processor and an external agent.
SysADC(7:0)	I/O	**System address/data check bus** An 8-bit bus containing parity check bits for the SysAD bus during data bus cycles.
SysCmd(8:0)	I/O	**System command/data identifier bus** A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP	I/O	**Reserved system command/data identifier bus parity** for the R4700 unused on input and zero on output.
Clock/Control Interface		
MasterClock	I	**Master clock** Master clock input at one half the processor operating frequency.
MasterOut	O	**Master clock out** Master clock output aligned with MasterClock.
RClock(1:0)	O	**Receive clocks** Two identical receive clocks at the system interface frequency.
TClock(1:0)	O	**Transmit clocks** Two identical transmit clocks at the system interface frequency.
IOOut	O	**Reserved for future output** Always HIGH.
IOIn	I	**Reserved for future input** Should be driven HIGH.
SyncOut	O	**Synchronization clock out** Must be connected to SyncIn through an interconnect that models the interconnect between MasterOut, TClock, RClock, and the external agent.
SyncIn	I	**Synchronization clock in** Synchronization clock input. See SyncOut.
Fault*	O	**Fault** Always HIGH.

AC Electrical Characteristics—R4700

(V_{CC}=5.0V ± 5%; T_{CASE} = 0°C to +85°C)

Clock Parameters—R4700

Parameter	Symbol	Test Conditions	R4700 80MHz		R4700 100MHz		R4700 133MHz		Units
			Min	Max	Min	Max	Min	Max	
MasterClock HIGH	t_{MCHIGH}	Transition ≤ t_{MCRise}	4	—	4	—	3	—	ns
MasterClock LOW	t_{MCLOW}	Transition ≤ t_{MCFall}	4	—	4	—	3	—	ns
MasterClock Frequency[1]	_	—	25	40	25	50	25	67	MHz
MasterClock Period	t_{MCP}	—	25	40	20	40	15	40	ns
Clock Jitter for MasterClock	$t_{JitterIn}$[2]	—	—	±250	—	±250	—	±250	ps
Clock Jitter for MasterOut, SyncOut, TClock, RClock	$t_{JitterOut}$[2]	—	—	±500	—	±500	—	±500	ps
MasterClock Rise Time	t_{MCRise}[2]	—	—	5.5	—	5	—	4	ns
MasterClock Fall Time	t_{MCFall}[2]	—	—	5.5	—	5	—	4	ns
ModeClock Period	$t_{ModeCKP}$[2]	—	—	256*t_{MCP}	—	256*t_{MCP}	—	256*t_{MCP}	ns
JTAG Clock Period	$t_{JTAGCKP}$[2]	—	—	4*t_{MCP}	—	4*t_{MCP}	—	4*t_{MCP}	ns
SyncOut to SyncIn Delay	t_{Sync}[2,3]	—	—	2*t_{MCP}	—	2*t_{MCP}	—	2*t_{MCP}	ns

1. Operation of the R4700 is only guaranteed with the Phase Lock Loop enabled.

2. Guaranteed by design.

3. Rise and fall times of the SyncIn signal must match those of MasterClock to avoid the introduction of additional clock skew.

System Interface Parameters—R4700

Note: Timings are measured from 1.5V of the clock to 1.5V of the signal.

Parameter	Symbol	Test Conditions	R4700 80MHz		R4700 100MHz		R4700 133MHz		Units
			Min	Max	Min	Max	Min	Max	
Data Output	t_{DO}	$mode_{14..13}$ = 10 (fastest)	0[1]	9	0[1]	9	0[1]	9	ns
		$mode_{14..13}$ = 01 (slowest)	0[1]	15	0[1]	15	0[1]	12	ns
Input Data Setup	t_{DS}	t_{rise} = 5ns t_{fall} = 5ns	3.5	—	3.5	—	3.5	—	ns
Input Data Hold	t_{DH}		1.5	—	1.5	—	1.5	—	ns

1. Guaranteed by design.

Boot-Time Interface Parameters—R4700

Parameter	Symbol	Test Conditions	R4700 80MHz		R4700 100MHz		R4700 133MHz		Units
			Min	Max	Min	Max	Min	Max	
Mode Data Setup	t_{DS}	—	3	—	3	—	3	—	Master ClockCycle
Mode Data Hold	t_{DH}	—	0	—	0	—	0	—	Master ClockCycle

Capacitive Load Deration—R4700

Parameter	Symbol	R4700 80MHz		R4700 100MHz		R4700 133MHz		Units
		Min	Max	Min	Max	Min	Max	
Load Derate	C_{LD}	—	2	—	2	—	2	ns/25pF

AC Electrical Characteristics — RV4700

(V_{CC}=3.3V ± 5%; T_{CASE} = 0°C to +85°C)

Clock Parameters

Parameter	Symbol	Test Conditions	RV4700 100MHz		RV4700 133MHz		RV4700 150MHz		Units
			Min	Max	Min	Max	Min	Max	
MasterClock HIGH	t_{MCHIGH}	Transition ≤ $t_{MCRise/Fall}$	4	—	3	—	3	—	ns
MasterClock LOW	t_{MCLOW}	Transition ≤ $t_{MCRise/Fall}$	4	—	3	—	3	—	ns
MasterClock Frequency[1]	_	—	25	50	25	67	25	75	MHz
MasterClock Period	t_{MCP}	—	20	40	15	40	13.3	40	ns
Clock Jitter for MasterClock	$t_{JitterIn}$[2]	—	—	±250	—	±250	—	±250	ps
Clock Jitter for MasterOut, SyncOut, TClock, RClock	$t_{JitterOut}$[2]	—	—	±500	—	±500	—	±500	ps
MasterClock Rise Time	t_{MCRise}[2]	—	—	5	—	4	—	3.5	ns
MasterClock Fall Time	t_{MCFall}[2]	—	—	5	—	4	—	3.5	ns
ModeClock Period	$t_{ModeCKP}$	—	—	256*t_{MCP}	—	256*t_{MCP}	—	256*t_{MCP}	ns
SyncOut to SyncIn Delay	t_{Sync}[2, 3]	—	—	2*t_{MCP}	—	2*t_{MCP}	—	2*t_{MCP}	ns

1. Typical integer instruction mix and cache miss rates.
2. Guaranteed by Design.
3. Rise and fall times of the SyncIn signal must match those of MasterClock to avoid the introduction of additional clock skew.

Parameter	Symbol	Test Conditions	RV4700 175MHz[1]		RV4700 200MHz[1]		Units
			Min	Max	Min	Max	
MasterClock HIGH	t_{MCHIGH}	Transition ≤ $t_{MCRise/Fall}$	3	—	3	—	ns
MasterClock LOW	t_{MCLOW}	Transition ≤ $t_{MCRise/Fall}$	3	—	3	—	ns
MasterClock Frequency[2]	_	—	25	87.5	25	100	MHz
MasterClock Period	t_{MCP}	—	11.4	40	10	40	ns
Clock Jitter for MasterClock	$t_{JitterIn}$[3]	—	—	±250	—	±250	ps
Clock Jitter for MasterOut, SyncOut, TClock, RClock	$t_{JitterOu}$[3]	—	—	±500	—	±500	ps
MasterClock Rise Time	t_{MCRise}[3]	—	—	3.5	—	3.5	ns
MasterClock Fall Time	t_{MCFall}[3]	—	—	3.5	—	3.5	ns
ModeClock Period	$t_{ModeCKP}$	—	—	256*t_{MCP}	—	256*t_{MCP}	ns
SyncOut to SyncIn Delay	t_{Sync}[3, 4]	—	—	2*t_{MCP}	—	2*t_{MCP}	—

1. Operation of the R4700 is only guaranteed with the Phase Lock Loop enabled.
2. Typical integer instruction mix and cache miss rates.
3. Guaranteed by design.
4. Rise and fall times of the SyncIn signal must match those of MasterClock to avoid the introduction of additional clock skew.

DC Electrical Characteristics—RV4700

(V_{CC} = 3.3±5%, T_{CASE} = 0°C to +85°C)

Parameter	RV4700 100MHz		RV4700 133MHz		Conditions
	Min	Max	Min	Max	
V_{OL}	—	0.1V	—	0.1V	$\|I_{OUT}\|$= 20uA
V_{OH}	V_{CC} - 0.1V	—	V_{CC} - 0.1V	—	
V_{OL}	—	0.4V	—	0.4V	$\|I_{OUT}\|$= 4mA
V_{OH}	2.4V	—	2.4V	—	
V_{IL}	–0.5V	$0.2V_{CC}$	–0.5V	$0.2V_{CC}$	—
V_{IH}	$0.7V_{CC}$	V_{CC} + 0.5V	$0.7V_{CC}$	V_{CC} + 0.5V	—
I_{IN}	—	±10uA	—	±10uA	$0 \le V_{IN} \le V_{CC}$
C_{IN}	—	15pF	—	15pF	—
C_{OUT}	—	15pF	—	15pF	—
I/O_{LEAK}	—	20uA	—	20uA	Input/Output Leakage

Parameter	RV4700 150MHz		RV4700 175MHz		RV4700 200MHz		Conditions
	Min	Max	Min	Max	Min	Max	
V_{OL}	—	0.1V	—	0.1V	—	0.1V	$\|I_{OUT}\|$= 20uA
V_{OH}	V_{CC}- 0.1V	—	V_{CC} - 0.1V	—	V_{CC} - 0.1V	—	
V_{OL}	—	0.4V	—	0.4V	—	0.4V	$\|I_{OUT}\|$= 4mA
V_{OH}	2.4V	—	2.4V	—	2.4V	—	
V_{IL}	–0.5V	$0.2V_{CC}$	–0.5V	$0.2V_{CC}$	–0.5V	$0.2V_{CC}$	—
V_{IH}	$0.7V_{CC}$	V_{CC} + 0.5V	$0.7V_{CC}$	V_{CC} + 0.5V	$0.7V_{CC}$	V_{CC} + 0.5V	—
I_{IN}	—	±10uA	—	±10uA	—	±10uA	$0 \le V_{IN} \le V_{CC}$
C_{IN}	—	15pF	—	15pF	—	15pF	—
C_{OUT}	—	15pF	—	15pF	—	15pF	—
I/O_{LEAK}	—	20uA	—	20uA	—	20uA	Input/Output Leakage

System Interface Parameters—RV4700

Note: Operation of the R4700 is only guaranteed with the Phase Lock Loop enabled.

Parameter	Symbol	Test Conditions	RV4700 100MHz		RV4700 133MHz		RV4700 150MHz		Units
			Min	Max	Min	Max	Min	Max	
Data Output[1]	t_{DM}= Min t_{DO} = Max	$mode_{14..13}$ = 10 (fastest)	0	9	0	9	0	8	ns
		$mode_{14..13}$ = 01 (slowest)	0	15	0	12	0	12	ns
Input Data Setup	t_{DS}	t_{rise} = 3ns t_{fall} = 3ns	3.5	—	3.5	—	3.5	—	ns
Input Data Hold	t_{DH}		1.5	—	1.5	—	1.5	—	ns

1. Timings are measured from 1.5V of the clock to 1.5V of the signal.

Parameter	Symbol	Test Conditions	RV4700 175MHz		RV4700 200MHz		Units
			Min	Max	Min	Max	
Data Output[1]	t_{DM}= Min t_{DO} = Max	$mode_{14..13}$ = 10 (fastest)	0	8	0	8	ns
		$mode_{14..13}$ = 01 (slowest)	0	12	0	12	ns
Input ata Setup	t_{DS}	t_{rise} = 3ns t_{fall} = 3ns	3.5	—	3.5	—	ns
Input Data Hold	t_{DH}		1.5	—	1.5	—	ns

1. Capacitive load for all output timings is 50pF.

Boot-Time Interface Parameters—RV4700

Parameter	Symbol	Test Conditions	RV4700 100MHz		RV4700 133MHz		RV4700 150MHz		Units
			Min	Max	Min	Max	Min	Max	
Mode Data Setup	t_{DS}	—	3	—	3	—	3	—	Master Clock Cycle
Mode Data Hold	t_{DH}	—	0	—	0	—	0	—	Master Clock Cycle

Parameter	Symbol	Test Conditions	RV4700 175MHz		RV4700 200MHz		Units
			Min	Max	Min	Max	
Mode Data Setup	t_{DS}	—	3	—	3	—	Master Clock Cycle
Mode Data Hold	t_{DH}	—	0	—	0	—	Master Clock Cycle

Power Consumption—RV4700

Parameter		RV4700 100MHz		RV4700 133MHz		RV4700 150MHz		Conditions
		Typical[1]	Max	Typical[1]	Max	Typical[1]	Max	
System Condition		100/25MHz		133/33MHz		150/38MHz		—
I_{CC}	standby	—	125mA[2]	—	175mA[2]	—	200mA[2]	C_L = 0pF[3]
		—	175mA[2]	—	225mA[2]	—	250mA[2]	C_L = 50pF
	active	575mA[2]	875mA[2]	775mA[2]	1150mA[2]	875mA[2]	1300mA[2]	C_L = 0pF, No SysAd activity[3]
		650mA[2]	1100mA[2]	850mA[2]	1375mA[2]	950mA[2]	1550mA[2]	C_L = 50pF R4x00 compatible writes, T_C = 25°C[3]
		650mA[2]	1275mA[4]	850mA[2]	1525mA[4]	950mA[2]	1725mA[2]	C_L = 50pF Pipelined writes or write re-issue, T_C = 25°C

1. Typical integer instruction mix and cache miss rates.
2. These are not tested. They are the result of engineering analysis and are provided for reference only.
3. Guaranteed by design.
4. These are the specifications IDT tests to insure compliance.

Parameter		RV4700 175MHz		RV4700 200MHz		Conditions
		Typical[1]	Max	Typical[1]	Max	
System Condition		175/44MHz		200/50MHz		—
I_{CC}	standby	—	200mA[2]	—	200mA[2]	C_L = 0pF[3]
		—	250mA[2]	—	250mA[2]	C_L = 50pF
	active	1025mA[2]	1500mA[2]	1025mA[2]	1500mA[2]	C_L = 0pF, No SysAd activity[3]
		1200mA[2]	1800mA[2]	1200mA[2]	1800mA[2]	C_L = 50pF R4x00 compatible writes, T_C = 25°C[3]
		1200mA[2]	2000mA[4]	1200mA[2]	2000mA[4]	C_L = 50pF Pipelined writes or write re-issue, T_C = 25°C

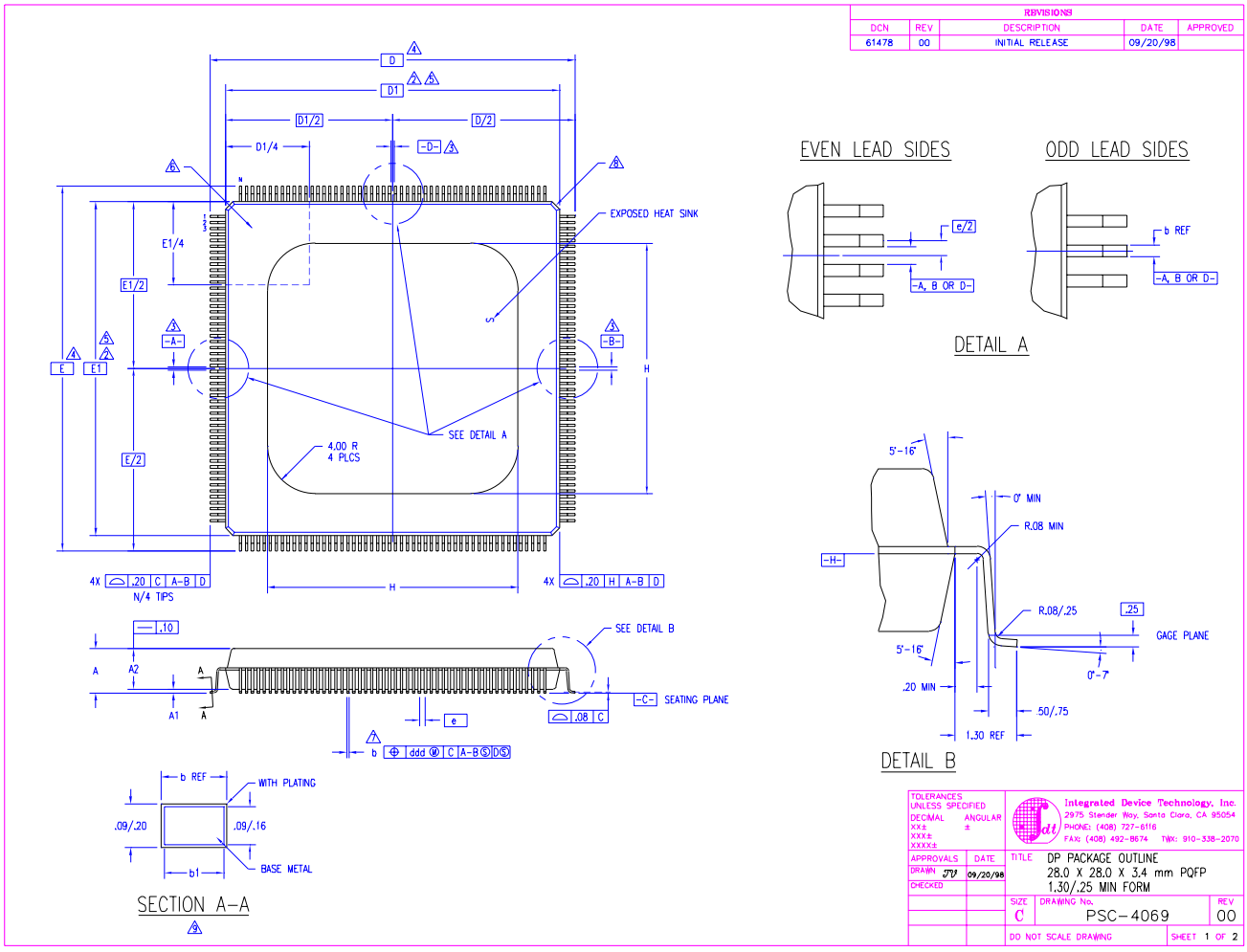
1. Typical integer instruction mix and cache miss rates.
2. These are not tested. They are the result of engineering analysis and are provided for reference only.
3. Guaranteed by design.
4. These are the specifications IDT tests to insure compliance.

RC4700 QFP Package Pin-Out

Note: N.C. pins should be left floating for maximum flexibility and compatibility with future designs.

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	N.C.	53	N.C.	105	N.C.	157	N.C.
2	N.C.	54	N.C.	106	N.C.	158	N.C.
3	VSS	55	SysCmd2	107	N.C.	159	RClock0
4	VCC	56	SysAD36	108	N.C.	160	RClock1
5	SysAD45	57	SysAD4	109	VCC	161	SyncOut
6	SysAD13	58	SysCmd1	110	VSS	162	SysAD30
7	Fault*	59	VSS	111	SysAD21	163	VCC
8	SysAD44	60	VCC	112	SysAD53	164	VSS
9	VSS	61	SysAD35	113	RdRdy*	165	SysAD62
10	VCC	62	SysAD3	114	ModeIn	166	MasterOut
11	SysAD12	63	SysCmd0	115	SysAD22	167	SysAD31
12	SysCmdP	64	SysAD34	116	SysAD54	168	SysAD63
13	SysAD43	65	VSS	117	VCC	169	VCC
14	SysAD11	66	VCC	118	VSS	170	VSS
15	VSS	67	N.C.	119	Release*	171	VCCOK
16	VCC	68	N.C.	120	SysAD23	172	SysADC3
17	SysCmd8	69	SysAD2	121	SysAD55	173	SysADC7
18	SysAD42	70	Int5*	122	NMI*	174	VCC
19	SysAD10	71	SysAD33	123	VCC	175	VSS
20	SysCmd7	72	SysAD1	124	VSS	176	N.C.
21	VSS	73	VSS	125	SysADC2	177	N.C.
22	VCC	74	VCC	126	SysADC6	178	N.C.
23	SysAD41	75	Int4*	127	VCC	179	N.C.
24	SysAD9	76	SysAD32	128	SysAD24	180	N.C.
25	SysCmd6	77	SysAD0	129	VCC	181	VCCP
26	SysAD40	78	Int3*	130	VSS	182	VSSP
27	N.C.	79	VSS	131	SysAD56	183	N.C.
28	N.C.	80	VCC	132	N.C.	184	N.C.
29	VSS	81	Int2*	133	SysAD25	185	MasterClock
30	VCC	82	SysAD16	134	SysAD57	186	VCC
31	SysAD8	83	SysAD48	135	VCC	187	VSS
32	SysCmd5	84	Int1*	136	VSS	188	SyncIn
33	SysADC4	85	VSS	137	IOOut	189	VCC
34	SysADC0	86	VCC	138	SysAD26	190	VSS
35	VSS	87	SysAD17	139	SysAD58	191	N.C.
36	VCC	88	SysAD49	140	IOIn	192	SysADC5
37	SysCmd4	89	Int0*	141	VCC	193	SysADC1
38	SysAD39	90	SysAD18	142	VSS	194	JTDI
39	SysAD7	91	VSS	143	SysAD27	195	VCC
40	SysCMD3	92	VCC	144	SysAD59	196	VSS
41	VSS	93	SysAD50	145	ColdReset*	197	SysAD47
42	VCC	94	ValidIn*	146	SysAD28	198	SysAD15
43	SysAD38	95	SysAD19	147	VCC	199	JTDO
44	SysAD6	96	SysAD51	148	VSS	200	SysAD46
45	ModeClock	97	VSS	149	SysAD60	201	VCC
46	WrRdy*	98	VCC	150	Reset*	202	VSS
47	SysAD37	99	ValidOut*	151	SysAD29	203	SysAD14
48	SysAD5	100	SysAD20	152	SysAD61	204	N.C.
49	VSS	101	SysAD52	153	VCC	205	TClock0
50	VCC	102	ExtRqst*	154	VSS	206	TClock1
51	N.C.	103	N.C.	155	N.C.	207	N.C.
52	N.C.	104	N.C.	156	N.C.	208	N.C.

Physical Specifications — 208-pin QFP



Physical Specifications - page 2

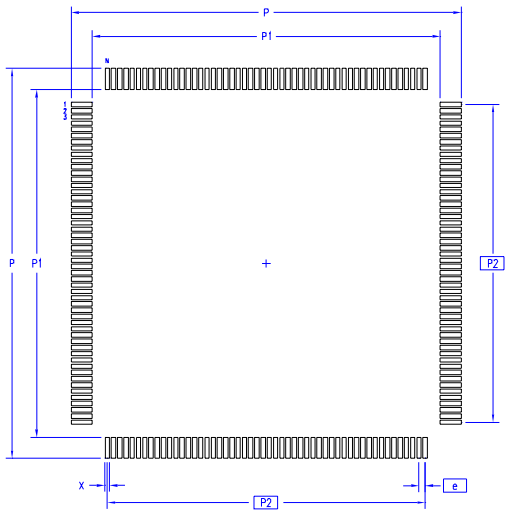
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
61478	00	INITIAL RELEASE	09/20/98	

SYMBOL	JEDEC VARIATION FA-1 MIN	NOM	MAX	NOTE
A	–	–	4.10	
A1	.25	–	–	
A2	3.20	3.40	3.60	
D		30.60 BSC		4
D1		28.00 BSC		5,2
E		30.60 BSC		4
E1		28.00 BSC		5,2
H		21.00 REF		
N		208		
e		.50 BSC		
b	.17	–	.27	7
b1	.17	.20	.23	
ddd	–	–	.08	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
2. TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
3. DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]
4. DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [-C-]
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
6. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-143, VARIATION FA-1

LAND PATTERN DIMENSIONS



	MIN	MAX
P	31.20	31.40
P1	27.80	28.00
P2	25.50 BSC	
X	.30	.40
e	.50 BSC	
N	208	

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

APPROVALS DATE
DRAWN JTV 09/20/98
CHECKED

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

TITLE: DP PACKAGE OUTLINE
28.0 X 28.0 X 3.4 mm PQFP
1.30/.25 MIN FORM

SIZE C | DRAWING No. PSC-4069 | REV 00

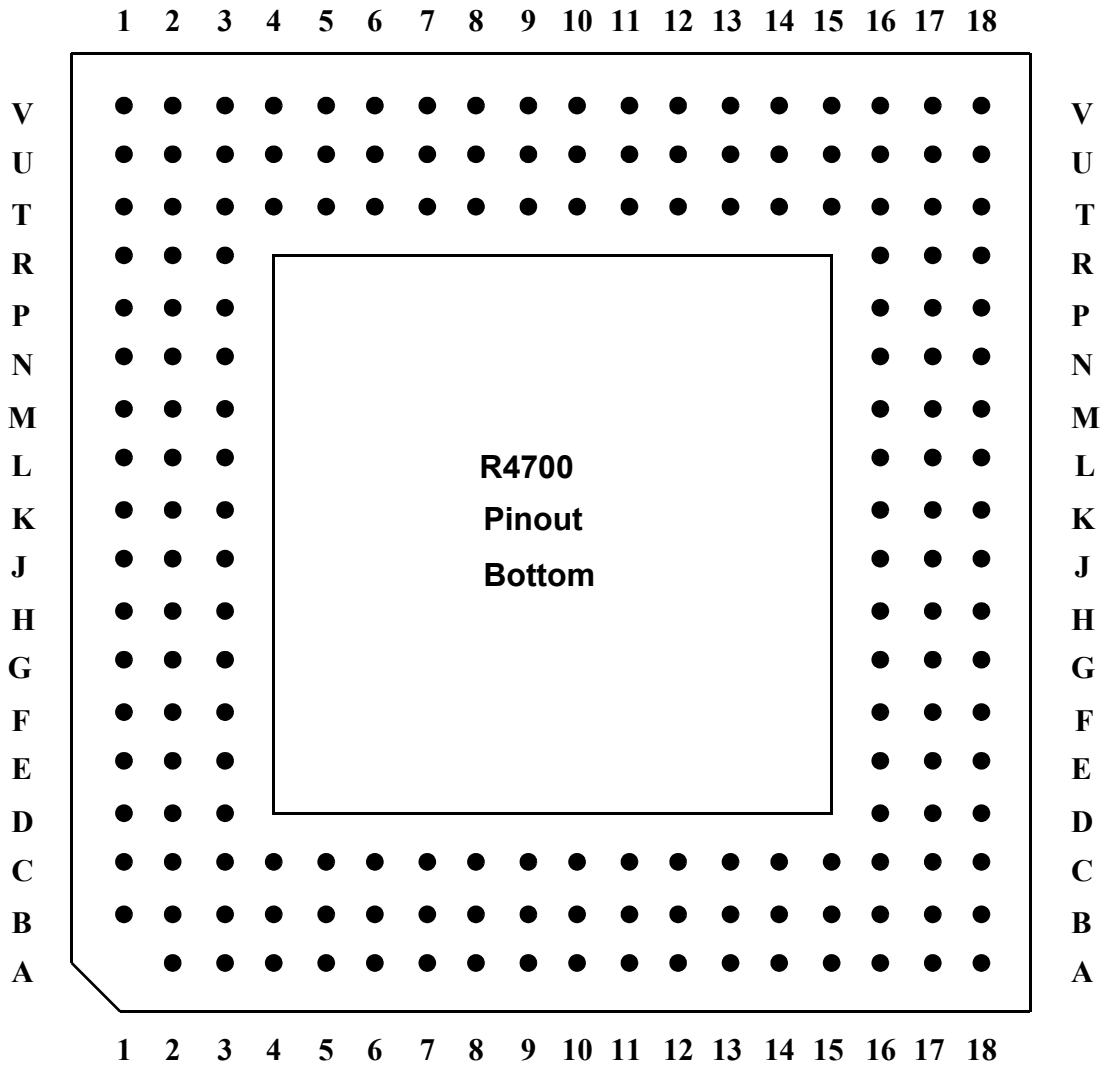
DO NOT SCALE DRAWING | SHEET 2 OF 2

RC4700 PGA Package Pin-Out

Note: N.C. pins should be left floating for maximum flexibility and compatibility with future designs.

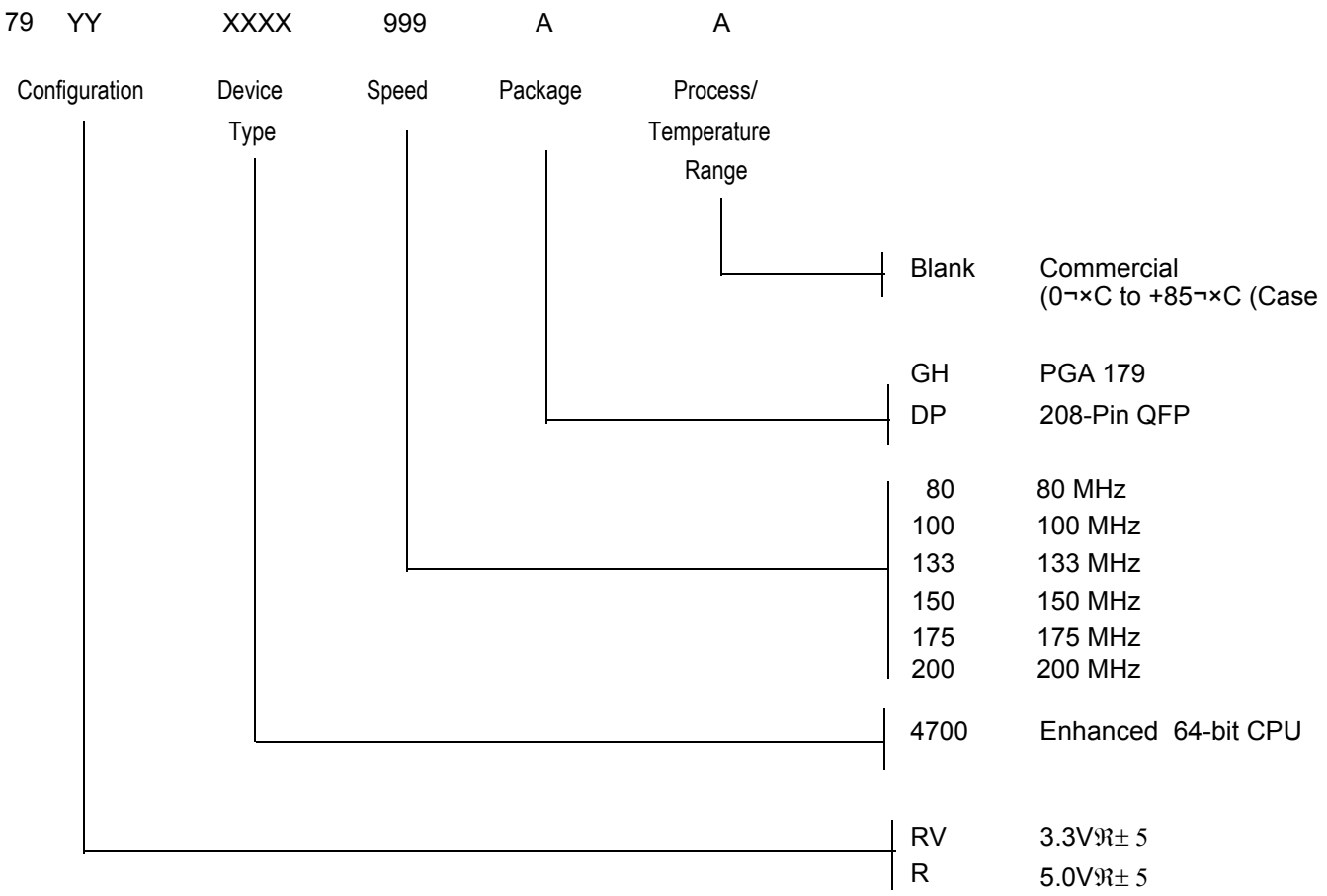
Function	Pin	Function	Pin	Function	Pin
ColdReset*	T14	SysAD36	C3	VCC	B18
ExtRqst*	U2	SysAD37	B3	VCC	C1
Fault*	B16	SysAD38	C6	VCC	D18
Reserved O (NC)	U10	SysAD39	C7	VCC	F1
Reserved I (Vcc)	T9	SysAD40	C10	VCC	G18
IOIn	T13	SysAD41	C11	VCC	H1
IOOut	U12	SysAD42	B13	VCC	J18
Int0	N2	SysAD43	A15	VCC	K1
Int1	L3	SysAD44	C15	VCC	L18
Int2	K3	SysAD45	B17	VCC	M1
Int3	J3	SysAD46	E17	VCC	N18
Int4	H3	SysAD47	F17	VCC	R1
Int5	F2	SysAD48	L2	VCC	T18
MasterClock	J17	SysAD49	M3	VCC	U1
MasterOut	P17	SysAD50	N3	VCC	V3
ModeClock	B4	SysAD51	R2	VCC	V6
ModeIn	U4	SysAD52	T3	VCC	V8
NMI	U7	SysAD53	U3	VCC	V10
RClock0	T17	SysAD54	T6	VCC	V12
RClock1	R16	SysAD55	T7	VCC	V14
RdRdy*	T5	SysAD56	T10	VCC	V17
Release	V5	SysAD57	T11	VSS	A3
Reset*	U16	SysAD58	U13	VSS	A6
SyncIn	J16	SysAD59	V15	VSS	A8
SyncOut	P16	SysAD60	T15	VSS	A10
SysAD0	J2	SysAD61	U17	VSS	A12
SysAD1	G2	SysAD62	N16	VSS	A14
SysAD2	E1	SysAD63	N17	VSS	A17
SysAD3	E3	SysADC0	C8	VSS	A18
SysAD4	C2	SysADC1	G17	VSS	B1
SysAD5	C4	SysADC2	T8	VSS	C18
SysAD6	B5	SysADC3	L16	VSS	D1
SysAD7	B6	SysADC4	B8	VSS	F18
SysAD8	B9	SysADC5	H16	VSS	G1
SysAD9	B11	SysADC6	U8	VSS	H18
SysAD10	C12	SysADC7	L17	VSS	J1
SysAD11	B14	SysCmd0	E2	VSS	K18
SysAD12	B15	SysCmd1	D3	VSS	L1
SysAD13	C16	SysCmd2	B2	VSS	M18
SysAD14	D17	SysCmd3	A5	VSS	N1
SysAD15	E18	SysCmd4	B7	VSS	P18
SysAD16	K2	SysCmd5	C9	VSS	R18
SysAD17	M2	SysCmd6	B10	VSS	T1
SysAD18	P1	SysCmd7	B12	VSS	U18
SysAD19	P3	SysCmd8	C13	VSS	V1
SysAD20	T2	SysCmdP	C14	VSS	V2

Physical Specifications — PGA



2884 drw 12

Ordering Information



Valid Combinations

79R4700 - 80, 100, 133 - GH, DP	PGA, QFP Package
79RV4700 -100, 133, 150, 175, 200 - GH, DP	PGA, QFP Package

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