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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	24
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 11x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1783-e-sp

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

28-Pin 8-Bit Advanced Analog Flash Microcontroller Product Brief

High-Performance RISC CPU:

- Only 49 Instructions
- Operating Speed:
 - DC 32 MHz clock input
 - DC 125 ns instruction cycle
- Interrupt Capability with Automatic Context Saving
- 16-Level Deep Hardware Stack with optional Overflow/Underflow Reset
- Direct, Indirect and Relative Addressing modes:
- Two full 16-bit File Select Registers (FSRs)
- FSRs can read program and data memory

Extreme Low-Power (XLP) Management:

- Standby Current (PIC16LF1782/1783):
 - 50 nA @ 1.8V, typical
- Watchdog Timer Current (PIC16LF1782/1783):
 500 nA @ 1.8V, typical
- Timer1 (32.768 kHz Real-Time Clock) Oscillator Current (PIC16LF1782/1783):
 - 500 nA @ 1.8V, typical
- Operating Current (PIC16LF1782/1783):
 4 μA @ 32 kHz, 1.8V, typical
- Operating Current (PIC16LF1782/1783):
 - 150 μA @ 1 MHz, 1.8V, typical

Memory Features:

- Up to 4 KW Flash Program Memory:
 - Self-programmable under software control
 - Programmable code protection
 - Programmable write protection
- 256 Bytes of Data EEPROM
- Up to 512 Bytes of RAM

High-Performance PWM Controller:

- Two Programmable Switch Mode Controller (PSMC) modules:
 - Digital and/or analog feedback control of PWM frequency and pulse begin/end times
 - 16-bit Period, Duty Cycle and Phase
 - 16 ns clock resolution
 - Supports single PWM, complimentary, pushpull and three-phase modes of operation
 - Dead-band control with 8-bit counter
 - Auto-shutdown and restart
 - Leading and falling edge blanking
 - Burst mode

Analog Peripheral Features:

- Analog-to-Digital Converter (ADC):
 - Fully differential 12-bit converter
 - 100 ksps conversion rate
 - 11 single-ended channels
 - 5 differential channels
 - Positive and negative reference selection
- 8-bit Digital-to-Analog Converter (DAC):
 - Output available externally
 - Positive and negative reference selection
 - Internal connections to comparators, op amps, Fixed Voltage Reference (FVR) and ADC
- Three High-Speed Comparators:
 - 30 ns response time
 - Rail-to-rail inputs
 - Software selectable hysteresis
 - Internal connection to op amps, FVR and DAC
- Two Operational Amplifiers:
 - Rail-to-rail inputs/outputs
 - High/Low selectable Gain Bandwidth Product
 - Internal connection to DAC and FVR
- Fixed Voltage Reference (FVR):
 - 1.024V, 2.048V and 4.096V output levels
 - Internal connection to ADC, Comparators and DAC

Digital Peripheral Features:

- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Enhanced Timer1:
 - 16-bit timer/counter with prescaler
 - External Gate Input mode
 - Dedicated low-power 32 kHz oscillator driver
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture/Compare/PWM modules (CCP):
 - 16-bit Capture, maximum resolution 12.5 ns
 - 16-bit Compare, max resolution 31.25 ns
 - 10-bit PWM, max frequency 32 kHz
- Master Synchronous Serial Port (SSP) with SPI and I²C[™] with:
 - 7-bit address masking
 - SMBus/PMBus™ compatibility
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART):
 - RS-232, RS-485 and LIN compatible
 - Auto-baud detect
 - Auto-wake-up on start

Oscillator Features:

- Operate up to 32 MHz from Precision Internal Oscillator:
 - Factory calibrated to ±1%, typical
 - Software selectable frequency range from 32 MHz to 31 kHz
- 31 kHz Low-Power Internal Oscillator
- 32.768 kHz Timer1 Oscillator:
 - available as system clockLow power RTC
- External Oscillator Block with:
 - 4 crystal/resonator modes up to 32 MHz using 4x PLL
- 3 external clock modes up to 32 MHz
- 4x Phase-Locked Loop (PLL)
- Fail-Safe Clock Monitor:
 - Detect and recover from external oscillator failure
- Two-Speed Start-up:
- Minimize latency between code execution and external oscillator start-up

I/O Features:

- Up to 24 I/O Pins and 1 Input-only Pin:
 - High current sink/source for LED drivers
 - Individually programmable interrupt-onchange pins
 - Individually programmable weak pull-ups
 - Individual input level selection
 - Slew rate control on selected output pins
 - Open drain outputs on selected output pins

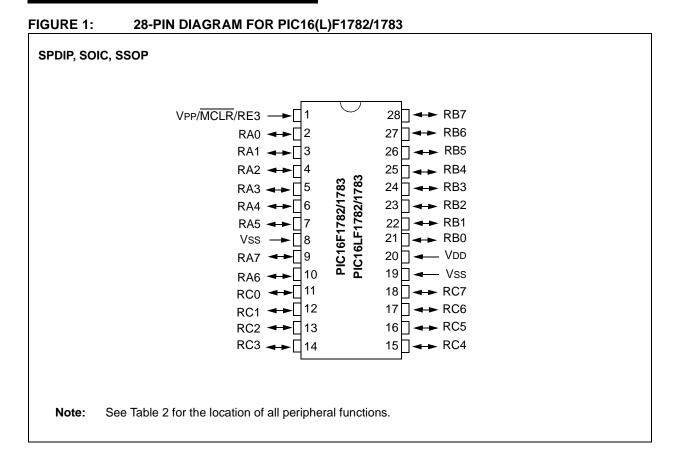
General Microcontroller Features:

- Power-Saving Sleep mode
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR) with Selectable Trip Point
- Extended Watchdog Timer (WDT)
- In-Circuit Serial Programming[™] (ICSP[™])
- In-Circuit Debug (ICD)
- Enhanced Low-Voltage Programming (LVP)
- Operating Voltage Range:
 - 1.8V to 3.6V (PIC16LF1782/1783)
 - 2.3V to 5.5V (PIC16F1782/1783)

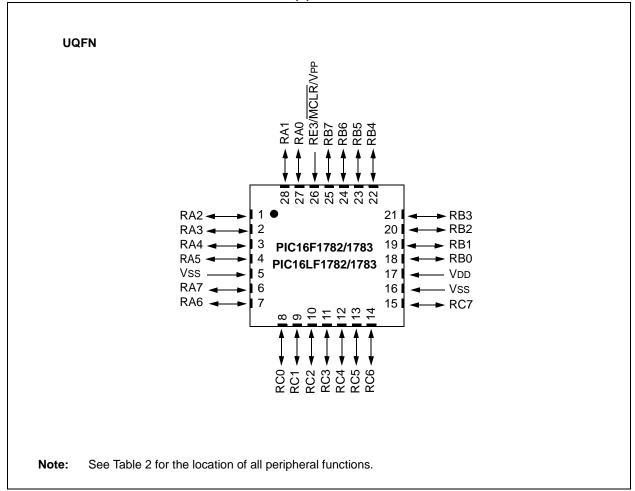
Device	Program Memory Flash (words)	Data EEPROM (bytes)	SRAM (bytes)	s0/I	12-bit A/D (ch)	Comparators	Operational Amplifiers	8-bit DAC	Timers 8/16-bit	Programmable Switch Mode Controllers (PSMC)	ССР	EUSART	MSSP (I²C™/SPI)	
PIC16F1782	2048	256	256	25	11	3	2	1	2/1	2	2	1	1	
PIC16LF1782	2048	256	256	25	11	3	2	1	2/1	2	2	1	1	
PIC16F1783	4096	256	512	25	11	3	2	1	2/1	2	2	1	1	
PIC16LF1783	4096	256	512	25	11	3	2	1	2/1	2	2	1	1	

TABLE 1: PIC16(L)F1782/1783 FAMILY TYPES

Note: Pin details are subject to change.







No. No. <th></th> <th></th> <th></th> <th></th> <th></th> <th></th> <th></th> <th> (</th> <th><u>(</u>-)</th> <th>02/11/00)</th> <th></th> <th></th> <th></th> <th></th> <th></th> <th></th>								(<u>(</u> -)	02/11/00)						
RA1 3 28 AN1- AN1 C2IN1- C2IN1- C2IN1- C3IN1- OPATOUT C2IN1- C3IN1- IOC Y RA2 4 1 AN2- NA2- CIIN1- C2IN1- C2IN1- C3IN1- DAC10UT1 DAC1VREP IOC Y RA3 5 2 AN3- VREF40 CIIN1+ C2IN1- DAC1VREP IOC Y RA4 6 3 C1OUT OPATIN+ IOC Y RA5 7 4 AN4+ C2OUT10 IOC Y OSC22 RA5 7 4 AN4+ C2OUT10 IOC Y OSC22 RA7 8 6 - VREF40 <	0/I	28-Pin SPDIP, SOIC, SSOP	28-Pin QFN	ADC	Reference	Comparator	Operation Amplifiers	8-bit DAC	Timers	PSMC	ССР	EUSART	dSSM	Interrupt	dn-IIn4	Basic
RA2 AN1- CCIN1- CSIN1- DACTOUTS 10C Y RA3 5 2 AN3- AN3- VREF-0 CIUIT DACTVREF 10C Y RA5 7 4 AN4- AN4- COUTO OPATIN TOCKI ICC Y RA6 10 7 4 AN4+ COUTO OPATIN DCC Y CLUIN RA3 S	RA0	2	27		_	C2IN0-	_	_		_	—		—	IOC	Y	—
ANZ- C2100+ C31N0+ DAC1VREF- Image: Case of the case	RA1	3	28		—	C2IN1-	OPA1OUT	_		-		-		IOC	Y	_
RAM 6 3 - C OPA11N - TOCKI - <t< td=""><td>RA2</td><td>4</td><td>1</td><td></td><td>VREF-</td><td>C2IN0+</td><td>_</td><td>DAC1OUT1 DAC1VREF-</td><td>_</td><td>_</td><td>—</td><td>_</td><td>—</td><td>IOC</td><td>Y</td><td>—</td></t<>	RA2	4	1		VREF-	C2IN0+	_	DAC1OUT1 DAC1VREF-	_	_	—	_	—	IOC	Y	—
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$					V _{REF+} (1)			DAC1VREF+			_		_			—
RA6 10 7 - - C20UT ⁽¹⁾ - <	RA4	6	3	—				_	T0CKI	_	—		—			
RA7 9 6 — Merf ⁽¹⁾ — — — PSMC1CLK PSMC2CLK — — ICC VI OSCI1 PSMC2CLK — — ICC VI PSMC2CLK Y OSCI1 OSCI1 PSMC2IN CCPI ⁽⁰⁾ — — ICC VI PSMC2IN Y — INT/ PSMC2IN Y — INT/ OSCI1 PSMC2IN Y — INT/ PSMC2IN Y — INT/ OSCI1 PSMC2IN Y — INT/ PSMC2IN Y — INT/ PSMC2IN Y — INT/ OSCI1 PSMC2IN Y … INT/ PSMC2IN Y … INT/ PSMC2IN Y … <t< td=""><td></td><td></td><td></td><td></td><td>_</td><td></td><td>OPA1IN-</td><td>_</td><td>_</td><td>_</td><td>_</td><td>_</td><td>SS</td><td></td><td></td><td>_</td></t<>					_		OPA1IN-	_	_	_	_	_	SS			_
RB0 21 18 AN12+ AN12+ - CLKN RB0 21 18 AN12+ AN10+ - C2IN1+ - - PSMC1IN PSMC2IN CCP1 ⁽¹⁾ - - INT/ PSMC2IN Y - RB1 22 19 AN10+ AN10+ - C1IN3- C2IN3- C3IN3- OPA2UT - - - - - - IOC Y - RB2 23 20 AN8+ - - OPA2IN+ - - - - - - IOC Y CLKR RB3 24 21 AN8+ - - OPA2IN+ - - - - - IOC Y - RB4 25 22 AN11+ - C3IN1+ - - - - - - IOC Y - RB5 26 23 AN13+ - C3OUT - - -					-	C2OUT'''	_	-	_	_	—		—			CLKOUT
RBI 22 19 AN12- AN10- AN10- C2103- C3102- C3102- C4104 <	RA7	9	6		VREF+ ⁽¹⁾	_	-	_	_	PSMC1CLK PSMC2CLK	—		_	IOC		OSC1/ CLKIN
Image: Normal and the	RB0	21	18		—	C2IN1+	_	_			CCP1 ⁽¹⁾		—		Y	—
RB3 24 21 AN9+ AN9+ C (1M2- C3IN2+ C3IN2+ OPA2IN+ C3IN2+ C3IN2+ - - - CCP2(1) - - IOC Y - RB4 25 22 AN11+ AN11+ - C3IN1+ - - - - - - IOC Y - RB5 26 23 AN13+ AN13- - C3OUT - - - - - SD0(1) IOC Y - RB6 27 24 - - - - - - TX(1) SD1(1) IOC Y ICSPCLK RB7 28 25 - - - - DAC1OUT2 - - RX(1) SCK(1) IOC Y ICSPCLK RC0 11 8 - - - - T10S0 PSMC1B CCP2(1) - IOC Y - RC1 12 9 -<	RB1	22	19		_	C2IN3-	OPA2OUT	_		-		-		IOC	Y	_
AN9- C2IN2- C3IN2- C3IN2- C3IN2+ C2IN2- C3IN2+ C3IN2+ C2IN2- C3IN2+ C2IN2+ C3IN1+ - C CINC Y - RB5 26 23 AN13+ - C3OUT - - T1G - - SD(f) IOC Y - RB6 27 24 - - - - - T1G - - SD(f) IOC Y ICSPDLK RB7 28 25 - - - DAC10UT2 - - RX(f) SC(f) IOC Y ICSPDLK RC0 11 8 - - - T1OSI PSMC18 CCP2(f) - - IOC Y - RC1 12 9 - -	RB2	23	20		—	—	OPA2IN-	—	-	—	—	_	—	IOC	Y	CLKR
AN11- An11- <th< td=""><td>RB3</td><td>24</td><td>21</td><td></td><td>—</td><td>C2IN2-</td><td>OPA2IN+</td><td>_</td><td> </td><td>_</td><td>CCP2⁽¹⁾</td><td>_</td><td> </td><td>IOC</td><td>Y</td><td>—</td></th<>	RB3	24	21		—	C2IN2-	OPA2IN+	_		_	CCP2 ⁽¹⁾	_		IOC	Y	—
RB6 27 24 — — — — — — — TX(1) SD(1) IOC Y ICSPCLK RB7 28 25 — — — — — — — — TX(1) SD(1) IOC Y ICSPCLK RB7 28 25 — — — — DAC10UT2 — — RX(1) SC(1) IOC Y ICSPCLK RC0 11 8 — — — — DAC10UT2 — — RX(1) SC(1) IOC Y ICSPDAT RC1 12 9 — — — — T1OSI PSMC18 CCP2(1) — — IOC Y — RC2 13 10 — — — — TOSI PSMC10 CCP1(1) — — IOC Y — RC3 14 11 <td>RB4</td> <td>25</td> <td>22</td> <td></td> <td>—</td> <td>C3IN1+</td> <td>_</td> <td>—</td> <td>_</td> <td>-</td> <td>—</td> <td>_</td> <td>—</td> <td>IOC</td> <td>Y</td> <td>—</td>	RB4	25	22		—	C3IN1+	_	—	_	-	—	_	—	IOC	Y	—
RB7 28 25 DAC1OUT2 RX(1) SCK(1) IOC Y ICSPDAT RC0 11 8 RC0 PSMC1A RC1 SCK(1) IOC Y ICSPDAT RC1 12 9 RC1 CCP2(1) IOC Y RC2 13 10 PSMC1C CCP2(1) IOC Y RC3 14 11 PSMC1D IOC Y RC3 14 11 PSMC1D IOC Y RC4 15 12 - PSMC1F SD(1) IO	RB5	26	23		—	C3OUT			T1G		—			IOC	Y	—
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RC1 12 9 T1CKI IOC Y RC2 13 10 T1OSI PSMC1B CCP2 ⁽¹⁾ IOC Y RC2 13 10 PSMC1C CCP2 ⁽¹⁾ IOC Y RC3 14 11 PSMC1D IOC Y RC4 15 12 PSMC1E SDI ⁽¹⁾ IOC Y RC4 15 12 PSMC1E SDI ⁽¹⁾ IOC Y RC5 16 13 PSMC1F SDI ⁽¹⁾ IOC Y RC6 17 14			25	—	—	—	_	DAC1OUT2	_	_	—	RX ⁽¹⁾ DT ⁽¹⁾	SCK ⁽¹⁾ SCL ⁽¹⁾			ICSPDAT
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	RC0	11	8	—	—	—	—	_	T1CKI	PSMC1A	—	_	—	IOC		—
RC3 14 11 - - - - - PSMC1D - - SCK ⁽¹⁾ SCL ⁽¹⁾ IOC Y - RC4 15 12 - - - - - PSMC1D - - SCK ⁽¹⁾ SCL ⁽¹⁾ IOC Y - RC4 15 12 - - - - - PSMC1E - - SDI ⁽¹⁾ SDA ⁽¹⁾ IOC Y - RC5 16 13 - - - - PSMC1F - - SDI ⁽¹⁾ SDA ⁽¹⁾ IOC Y - RC6 17 14 - - - - PSMC2A - TX ⁽¹⁾ SDA ⁽¹⁾ - IOC Y - RC7 18 15 - - - - - PSMC2B - RX ⁽¹⁾ SDC Y - RE3 1 26 - - - - - - - - VDD VPP VDD 20 1	RC1	12	9	—	—	—		_	T1OSI	PSMC1B			—	IOC	Y	—
RC4 15 12 PSMC1E SCL ⁽¹⁾ IOC Y RC5 16 13 PSMC1F SDI ⁽¹⁾ IOC Y RC6 17 14 PSMC2A TX ⁽¹⁾ IOC Y RC6 17 14 PSMC2A TX ⁽¹⁾ IOC Y RC7 18 15 PSMC2B RX ⁽¹⁾ IOC Y RE3 1 26 VDD VDD 20 17 VDD VDD VDD 16 VDD VDD VDD VDD VDD <	RC2	13	10	—	—	—	—	_	_	PSMC1C	CCP1 ⁽¹⁾	—		IOC	Y	—
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$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$				—	—	—	—	_	_		—	—	SDA ⁽¹⁾			—
RC7 18 15 - - - - - - PSMC2B - RX ⁽¹⁾ DT ⁽¹⁾ - IOC Y - RE3 1 26 - - - - - - PSMC2B - RX ⁽¹⁾ DT ⁽¹⁾ - IOC Y - RE3 1 26 - - - - - - - IOC Y MCLR/ VPP VDD 20 17 - - - - - - - VDD VSS 8, 5, - - - - - - - - VDD Vss 8, 5, - - - - - - - - VSs	RC5	16	13	—	—	—		_		PSMC1F	—		SDO ⁽¹⁾	IOC	Y	—
RE3 1 26 - - - - - - - - IOC Y MCLR/ VPP VDD 20 17 - - - - - - - VDD VSS 8, 5, 19 16 - - - - - - - VSS				—	—	—	—	—	—		_	CK ⁽¹⁾	_			—
VDD 20 17 - - - - - - - VDD VDD 20 17 - - - - - - VDD - - - VDD - - - VDD - - - - VDD - - - - VDD - - - - - - - - - - - - - - - - - - VDD - - - - - - - <td></td> <td></td> <td></td> <td>—</td> <td>—</td> <td>—</td> <td>—</td> <td>_</td> <td>_</td> <td>PSMC2B</td> <td>—</td> <td>DT⁽¹⁾</td> <td></td> <td></td> <td></td> <td></td>				—	—	—	—	_	_	PSMC2B	—	DT ⁽¹⁾				
Vss 8, 5, Vss				_	_	_	_	_	_	_	_	_	_	IOC	Y	VPP
				—	—	—	—	_	—	_	_	—	_	—	—	
Note 1. Dis functions can be applicated to one of two pin logations via poftware		19	16		—	_	_	_		—	—	—	—	—	_	Vss

TABLE 2: 28-PIN ALLOCATION TABLE (PIC16(L)F1782/1783)

Note 1: Pin functions can be assigned to one of two pin locations via software.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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ISBN: 978-1-60932-881-8

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