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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I ² C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	79
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5602bk0mll6

1 Introduction

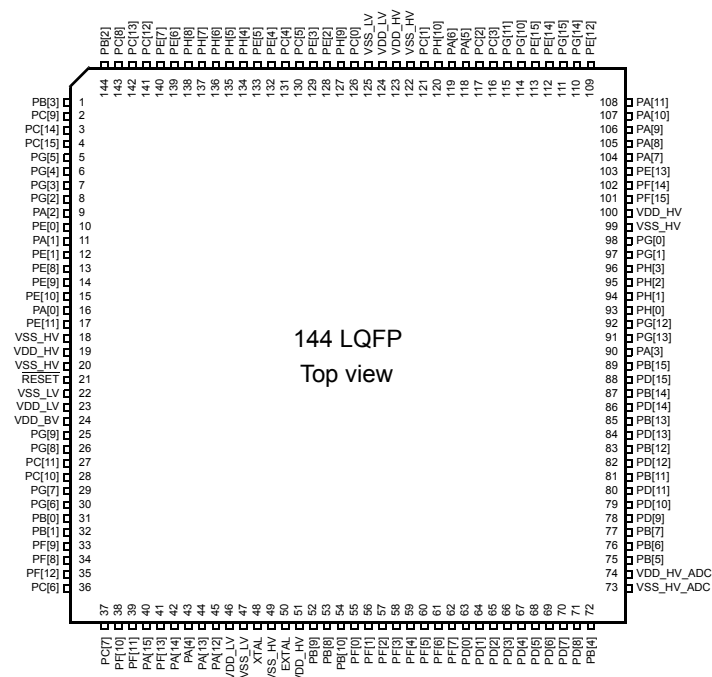
1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device. To ensure a complete understanding of the device functionality, refer also to the device reference manual and errata sheet.

1.2 Description

The MPC5604B/C is a family of next generation microcontrollers built on the Power Architecture® embedded category.

The MPC5604B/C family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding family of automotive-focused products designed to address the next wave of body electronics applications within the vehicle. The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category and only implements the VLE (variable-length encoding) APU, providing improved code density. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.



Note:

Availability of port pin alternate functions depends on product selection.

Figure 5. LQFP 144-pin configuration

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA ³
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 —	GPIO[2] E0UC[2] — — WKPU[3] ⁴	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	3	3	5	9	F2
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 —	GPIO[3] E0UC[3] — — EIRQ[0]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	43	39	68	90	K15
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 —	GPIO[4] E0UC[4] — — WKPU[9] ⁴	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	20	20	29	43	N6
PA[5]	PCR[5]	AF0 AF1 AF2 AF3	GPIO[5] E0UC[5] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	51	51	79	118	C11
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 —	GPIO[6] E0UC[6] — — EIRQ[1]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	52	52	80	119	D11
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 —	GPIO[7] E0UC[7] LIN3TX — EIRQ[2]	SIUL eMIOS_0 LINFlex_3 — SIUL	I/O I/O O — I	S	Tristate	44	44	71	104	D16
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — N/A ⁶ —	GPIO[8] E0UC[8] — — EIRQ[3] ABS[0] LIN3RX	SIUL eMIOS_0 — — SIUL BAM LINFlex_3	I/O I/O — — I I I	S	Input, weak pull-up	45	45	72	105	C16
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 N/A ⁶	GPIO[9] E0UC[9] — — FAB	SIUL eMIOS_0 — — BAM	I/O I/O — — I	S	Pull-down	46	46	73	106	C15

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA ³
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — —	GPIO[26] — — — ANS[2] WKPU[8] ⁴	SIUL — — — ADC WKPU	I/O — — — I I	J	Tristate	31	31	40	54	P9
PB[11] ⁸	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ANS[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — I/O I	J	Tristate	38	36	59	81	N13
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ANX[0]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	39	—	61	83	M16
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ANX[1]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	40	—	63	85	M13
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ANX[2]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	41	37	65	87	L16
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ANX[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	42	38	67	89	L13
PC[0] ⁹	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M	Input, weak pull-up	59	59	87	126	A8
PC[1] ⁹	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO ¹⁰ —	SIUL — JTAGC —	I/O — O —	M	Tristate	54	54	82	121	C9

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA ³
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — — — LIN2RX WKPU[13] ⁴	SIUL — — — LINFlex_2 WKPU	I/O — — — I I	S	Tristate	2	2	2	2	B1
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] CAN1TX CAN4TX ¹¹ MA[1]	SIUL FlexCAN_1 FlexCAN_4 ADC	I/O O O O	M	Tristate	13	13	22	28	M3
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — — — CAN1RX CAN4RX ¹¹ WKPU[5] ⁴	SIUL — — — FlexCAN_1 FlexCAN_4 WKPU	I/O — — — I I I	S	Tristate	—	—	21	27	M4
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 —	GPIO[44] E0UC[12] — — SIN_2	SIUL eMIOS_0 — — DSPI_2	I/O I/O — — I	M	Tristate	—	—	97	141	B4
PC[13]	PCR[45]	AF0 AF1 AF2 AF3	GPIO[45] E0UC[13] SOUT_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O O —	S	Tristate	—	—	98	142	A2
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 —	GPIO[46] E0UC[14] SCK_2 — EIRQ[8]	SIUL eMIOS_0 DSPI_2 — SIUL	I/O I/O I/O — I	S	Tristate	—	—	3	3	C1
PC[15]	PCR[47]	AF0 AF1 AF2 AF3	GPIO[47] E0UC[15] CS0_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O I/O —	M	Tristate	—	—	4	4	D3
PD[0]	PCR[48]	AF0 AF1 AF2 AF3 —	GPIO[48] — — — GPI[4]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	41	63	P12

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA ³
PF[10]	PCR[90]	AF0	GPIO[90]	SIUL	I/O	M	Tristate	—	—	—	38	R3
		AF1	—	—	—							
		AF2	—	—	—							
		AF3	—	—	—							
PF[11]	PCR[91]	AF0	GPIO[91]	SIUL	I/O	S	Tristate	—	—	—	39	R4
		AF1	—	—	—							
		AF2	—	—	—							
		AF3	—	—	—							
		—	WKPU[15] ⁴	WKPU	I							
PF[12]	PCR[92]	AF0	GPIO[92]	SIUL	I/O	M	Tristate	—	—	—	35	R1
		AF1	E1UC[25]	eMIOS_1	I/O							
		AF2	—	—	—							
		AF3	—	—	—							
PF[13]	PCR[93]	AF0	GPIO[93]	SIUL	I/O	S	Tristate	—	—	—	41	T6
		AF1	E1UC[26]	eMIOS_1	I/O							
		AF2	—	—	—							
		AF3	—	—	—							
		—	WKPU[16] ⁴	WKPU	I							
PF[14]	PCR[94]	AF0	GPIO[94]	SIUL	I/O	M	Tristate	—	43	—	102	D14
		AF1	CAN4TX ¹¹	FlexCAN_4	O							
		AF2	E1UC[27]	eMIOS_1	I/O							
		AF3	CAN1TX	FlexCAN_4	O							
PF[15]	PCR[95]	AF0	GPIO[95]	SIUL	I/O	S	Tristate	—	42	—	101	E15
		AF1	—	—	—							
		AF2	—	—	—							
		AF3	—	—	—							
		—	CAN1RX	FlexCAN_1	I							
		—	CAN4RX ¹¹	FlexCAN_4	I							
		—	EIRQ[13]	SIUL	I							
PG[0]	PCR[96]	AF0	GPIO[96]	SIUL	I/O	M	Tristate	—	41	—	98	E14
		AF1	CAN5TX ¹¹	FlexCAN_5	O							
		AF2	E1UC[23]	eMIOS_1	I/O							
		AF3	—	—	—							
PG[1]	PCR[97]	AF0	GPIO[97]	SIUL	I/O	S	Tristate	—	40	—	97	E13
		AF1	—	—	—							
		AF2	E1UC[24]	eMIOS_1	I/O							
		AF3	—	—	—							
		—	CAN5RX ¹¹	FlexCAN_5	I							
		—	EIRQ[14]	SIUL	I							

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA ³
PG[11]	PCR[107]	AF0 AF1 AF2 AF3	GPIO[107] E0UC[25] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	—	—	115	B12
PG[12]	PCR[108]	AF0 AF1 AF2 AF3	GPIO[108] E0UC[26] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	—	—	92	K14
PG[13]	PCR[109]	AF0 AF1 AF2 AF3	GPIO[109] E0UC[27] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	—	—	91	K16
PG[14]	PCR[110]	AF0 AF1 AF2 AF3	GPIO[110] E1UC[0] — —	SIUL eMIOS_1 — —	I/O I/O — —	S	Tristate	—	—	—	110	B14
PG[15]	PCR[111]	AF0 AF1 AF2 AF3	GPIO[111] E1UC[1] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	—	—	111	B13
PH[0]	PCR[112]	AF0 AF1 AF2 AF3 —	GPIO[112] E1UC[2] — — SIN1	SIUL eMIOS_1 — — DSPI_1	I/O I/O — — I	M	Tristate	—	—	—	93	F13
PH[1]	PCR[113]	AF0 AF1 AF2 AF3	GPIO[113] E1UC[3] SOUT1 —	SIUL eMIOS_1 DSPI_1 —	I/O I/O O —	M	Tristate	—	—	—	94	F14
PH[2]	PCR[114]	AF0 AF1 AF2 AF3	GPIO[114] E1UC[4] SCK_1 —	SIUL eMIOS_1 DSPI_1 —	I/O I/O I/O —	M	Tristate	—	—	—	95	F16
PH[3]	PCR[115]	AF0 AF1 AF2 AF3	GPIO[115] E1UC[5] CS0_1 —	SIUL eMIOS_1 DSPI_1 —	I/O I/O I/O —	M	Tristate	—	—	—	96	F15

Table 14. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V _{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V _{DD} ¹	SR	Voltage on VDD_HV pins with respect to ground (V _{SS})	—	4.5	5.5	V
			Voltage drop ²	3.0	5.5	
V _{SS_LV} ³	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V _{SS})	—	V _{SS} –0.1	V _{SS} +0.1	V
V _{DD_BV} ⁴	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V _{SS})	—	4.5	5.5	V
			Voltage drop ²	3.0	5.5	
			Relative to V _{DD}	V _{DD} –0.1	V _{DD} +0.1	
V _{SS_ADC}	SR	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V _{SS})	—	V _{SS} –0.1	V _{SS} +0.1	V
V _{DD_ADC} ⁵	SR	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V _{SS})	—	4.5	5.5	V
			Voltage drop ²	3.0	5.5	
			Relative to V _{DD}	V _{DD} –0.1	V _{DD} +0.1	
V _{IN}	SR	Voltage on any GPIO pin with respect to ground (V _{SS})	—	V _{SS} –0.1	—	V
			Relative to V _{DD}	—	V _{DD} +0.1	
I _{INJPAD}	SR	Injected input current on any pin during overload condition	—	–5	5	mA
I _{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
TV _{DD}	SR	V _{DD} slope to ensure correct power up ⁶	—	—	0.25	V/μs
T _A C-Grade Part	SR	Ambient temperature under bias	f _{CPU} ≤ 64 MHz	–40	85	°C
T _J C-Grade Part	SR	Junction temperature under bias		–40	110	
T _A V-Grade Part	SR	Ambient temperature under bias		–40	105	
T _J V-Grade Part	SR	Junction temperature under bias		–40	130	
T _A M-Grade Part	SR	Ambient temperature under bias		–40	125	
T _J M-Grade Part	SR	Junction temperature under bias		–40	150	

¹ 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.

² Full device operation is guaranteed by design when the voltage drops below 4.5 V down to 3.0 V. However, certain analog electrical characteristics will not be guaranteed to stay within the stated limits.

³ 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.

⁴ 100 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics).

⁵ 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.

⁶ Guaranteed by device validation

NOTE

RAM data retention is guaranteed with V_{DD_LV} not below 1.08 V.

3.15.2 I/O input DC characteristics

Table 16 provides input DC electrical characteristics as described in Figure 7.

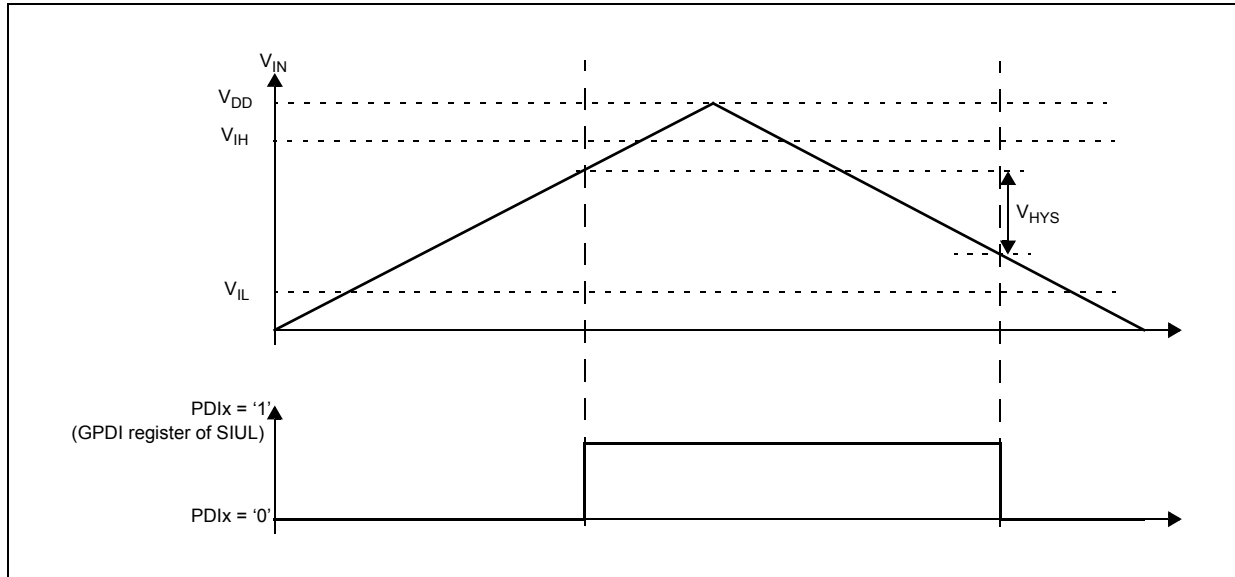


Figure 7. I/O input DC electrical characteristics definition

Table 16. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions ¹		Value			Unit
						Min	Typ	Max	
V _{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	—		0.65V _{DD}	—	V _{DD} +0.4	V
V _{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	—		−0.4	—	0.35V _{DD}	
V _{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—		0.1V _{DD}	—	—	
I _{LKG}	CC	D	Digital input leakage	No injection on adjacent pin	T _A = −40 °C	—	2	200	nA
		T _A = 25 °C			—	2	200		
		T _A = 85 °C			—	5	300		
		T _A = 105 °C			—	12	500		
		T _A = 125 °C			—	70	1000		
W _{FI} ²	SR	P	Wakeup input filtered pulse	—		—	—	40	ns
W _{NFI} ²	SR	P	Wakeup input not filtered pulse	—		1000	—	—	ns

¹ $V_{DD} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$, $T_A = -40$ to 125 °C , unless otherwise specified

² In the range from 40 to 1000 ns, pulses can be filtered or not filtered, according to operating temperature and voltage.

Table 19. MEDIUM configuration output buffer electrical characteristics

Symbol	C	Parameter	Conditions ¹	Value			Unit
				Min	Typ	Max	
V _{OH}	CC	C Output high level MEDIUM configuration	Push Pull	I _{OH} = -3.8 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	0.8V _{DD}	—	V
				I _{OH} = -2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	0.8V _{DD}	—	
				I _{OH} = -1 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ²	0.8V _{DD}	—	
				I _{OH} = -1 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V _{DD} -0.8	—	
				I _{OH} = -100 µA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	0.8V _{DD}	—	
V _{OL}	CC	C Output low level MEDIUM configuration	Push Pull	I _{OL} = 3.8 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	V
				I _{OL} = 2 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	0.2V _{DD}
				I _{OL} = 1 mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ²	—	—	0.1V _{DD}
				I _{OL} = 1 mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5
				I _{OL} = 100 µA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	0.1V _{DD}

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 20. FAST configuration output buffer electrical characteristics

Symbol	C	Parameter	Conditions ¹	Value			Unit
				Min	Typ	Max	
V _{OH}	CC	P Output high level FAST configuration	Push Pull	I _{OH} = -14mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	0.8V _{DD}	—	V
				I _{OH} = -7mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ²	0.8V _{DD}	—	
				I _{OH} = -11mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V _{DD} -0.8	—	

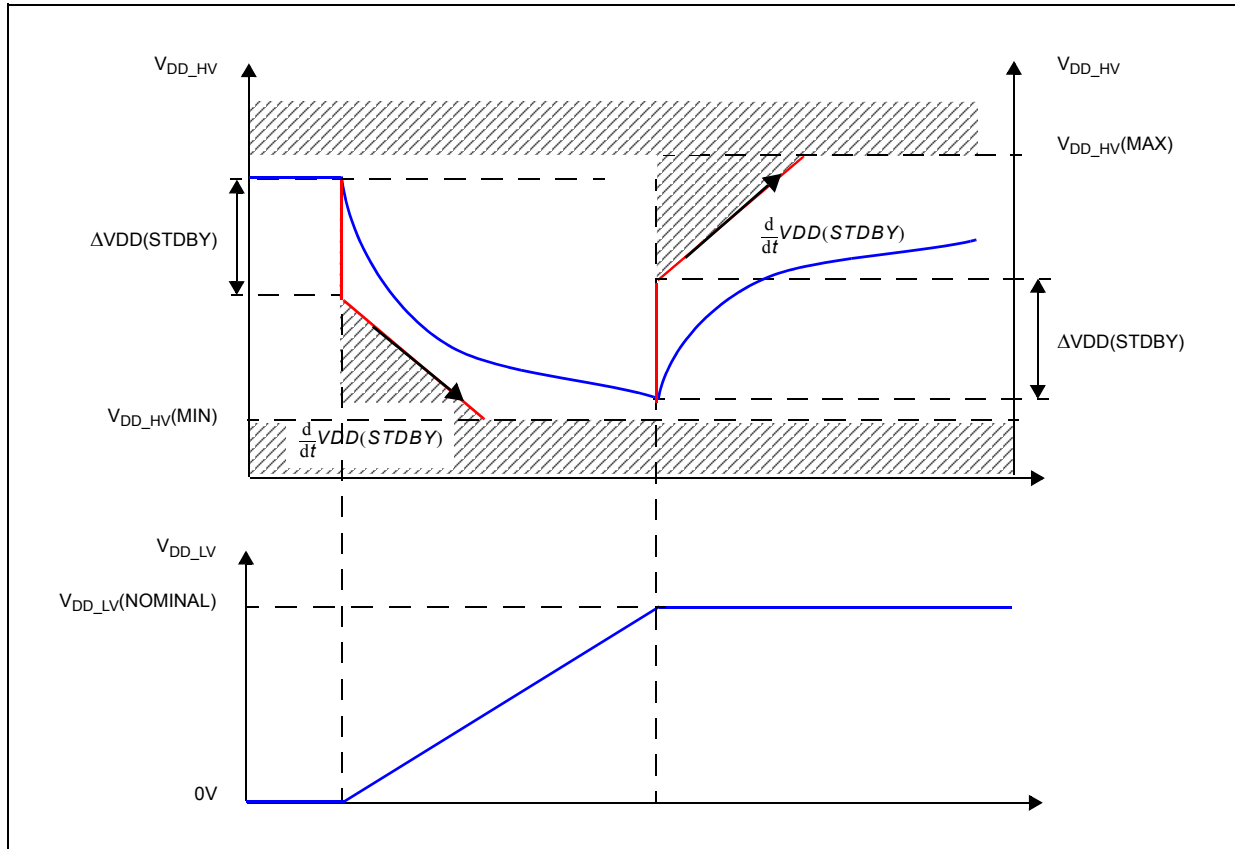
Figure 12. V_{DD_HV} and V_{DD_BV} supply constraints during STANDBY mode exit

Table 26. Voltage regulator electrical characteristics

Symbol	C	Parameter	Conditions ¹	Value			Unit
				Min	Typ	Max	
C_{REGn}	SR	Internal voltage regulator external capacitance	—	200	—	500	nF
R_{REG}	SR	Stability capacitor equivalent serial resistance	Range: 10 kHz to 20 MHz	—	—	0.2	Ω
C_{DEC1}	SR	Decoupling capacitance ² ballast	V_{DD_BV}/V_{SS_LV} pair: $V_{DD_BV} = 4.5\text{ V to }5.5\text{ V}$	100 ³	470 ⁴	—	nF
			V_{DD_BV}/V_{SS_LV} pair: $V_{DD_BV} = 3\text{ V to }3.6\text{ V}$	400		—	
C_{DEC2}	SR	Decoupling capacitance regulator supply	V_{DD}/V_{SS} pair	10	100	—	nF
$\left \frac{dV_{DD}}{dt} \right $	SR	Maximum slope on V_{DD}		—	—	250	mV/ μ s
$ \Delta V_{DD}(STDBY) $	SR	Maximum instant variation on V_{DD} during standby exit		—	—	30	mV

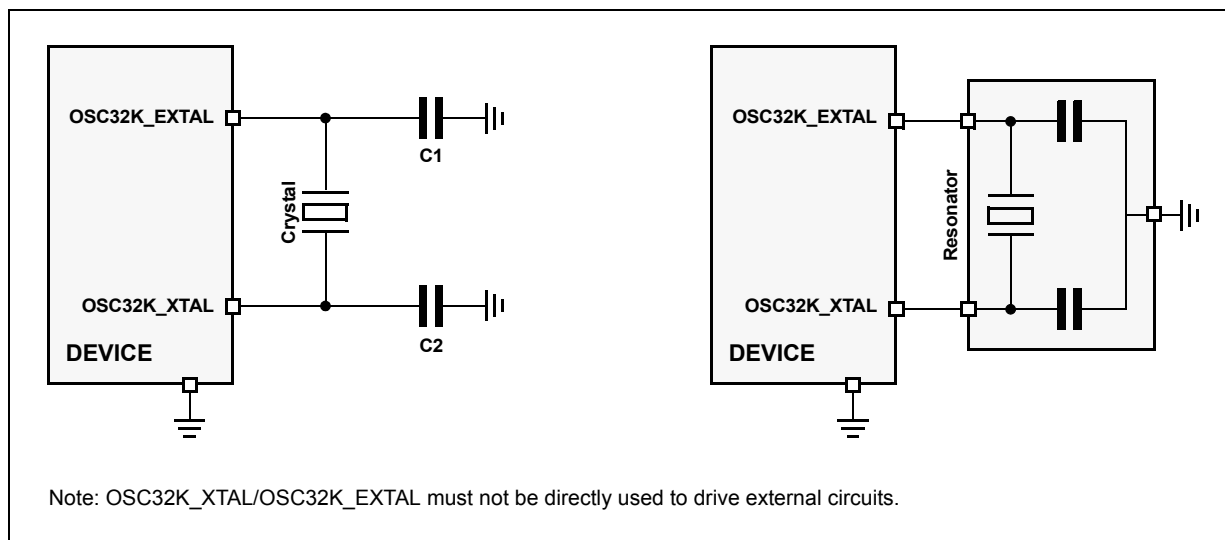


Figure 16. Crystal oscillator and resonator connection scheme

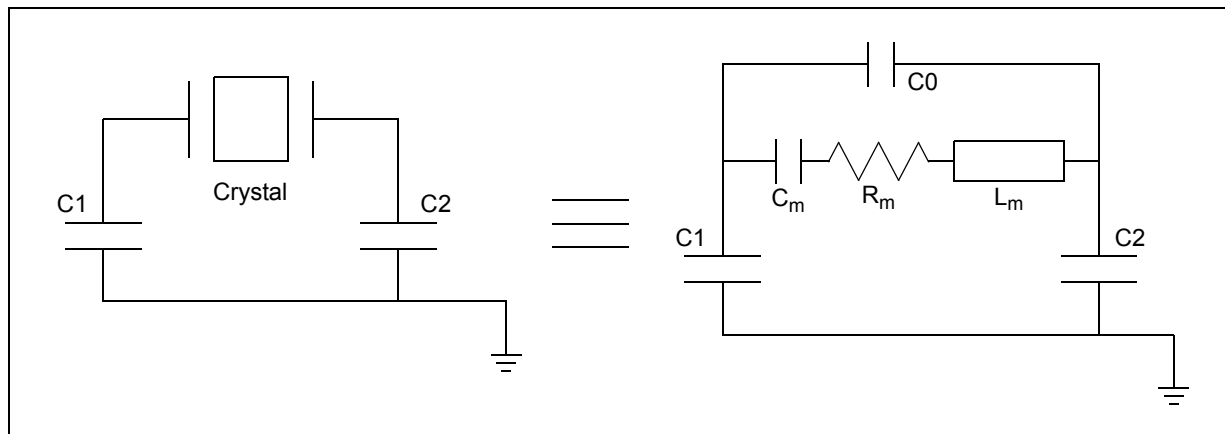


Figure 17. Equivalent circuit of a quartz crystal

Table 39. Crystal motional characteristics¹

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
L_m	Motional inductance	—	—	11.796	—	KH
C_m	Motional capacitance	—	—	2	—	fF
C1/C2	Load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground ²	—	18	—	28	pF
R_m ³	Motional resistance	AC coupled @ $C_0 = 2.85 \text{ pF}^4$	—	—	65	$k\Omega$
		AC coupled @ $C_0 = 4.9 \text{ pF}^4$	—	—	50	
		AC coupled @ $C_0 = 7.0 \text{ pF}^4$	—	—	35	
		AC coupled @ $C_0 = 9.0 \text{ pF}^4$	—	—	30	

¹ Crystal used: Epson Toyocom MC306

- ² This is the recommended range of load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground. It includes all the parasitics due to board traces, crystal and package.
- ³ Maximum ESR (R_m) of the crystal is 50 k Ω
- ⁴ C0 includes a parasitic capacitance of 2.0 pF between OSC32K_XTAL and OSC32K_EXTAL pins

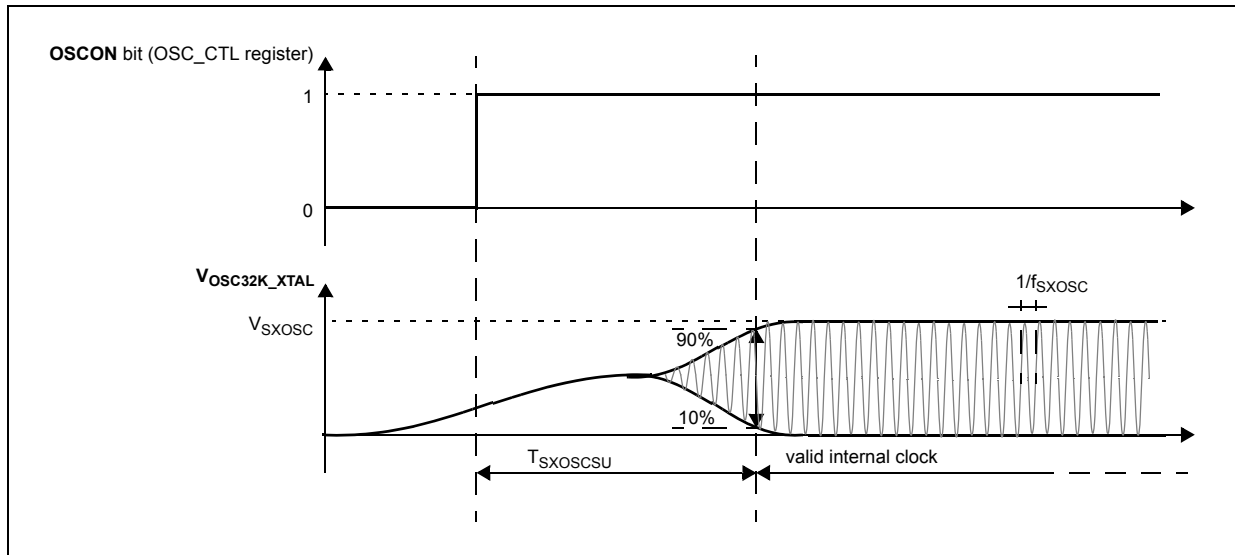


Figure 18. Slow external crystal oscillator (32 kHz) timing diagram

Table 40. Slow external crystal oscillator (32 kHz) electrical characteristics

Symbol	C	Parameter	Conditions ¹	Value			Unit
				Min	Typ	Max	
f_{SXOSC}	SR	—	Slow external crystal oscillator frequency	32	32.768	40	kHz
V_{SXOSC}	CC	T	Oscillation amplitude	—	2.1	—	V
$I_{SXOSCBias}$	CC	T	Oscillation bias current	—	2.5	—	μ A
I_{SXOSC}	CC	T	Slow external crystal oscillator consumption	—	—	8	μ A
$T_{SXOSCSU}$	CC	T	Slow external crystal oscillator start-up time	—	—	2 ²	s

¹ $V_{DD} = 3.3 \text{ V} \pm 10\% / 5.0 \text{ V} \pm 10\%$, $T_A = -40$ to 125°C , unless otherwise specified. Values are specified for no neighbor GPIO pin activity. If oscillator is enabled (OSC32K_XTAL and OSC32K_EXTAL pins), neighboring pins should not toggle.

² Start-up time has been measured with EPSON TOYOCOM MC306 crystal. Variation may be seen with other crystal.

3.23 FMPLL electrical characteristics

The device provides a frequency-modulated phase-locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.

Table 42. Fast internal RC oscillator (16 MHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions ¹		Value			Unit
						Min	Typ	Max	
I _{FIRCSTOP}	CC	T	Fast internal RC oscillator high frequency and system clock current in stop mode	T _A = 25 °C	sysclk = off	—	500	—	μA
					sysclk = 2 MHz	—	600	—	
					sysclk = 4 MHz	—	700	—	
					sysclk = 8 MHz	—	900	—	
					sysclk = 16 MHz	—	1250	—	
t _{FIRCSU}	CC	C	Fast internal RC oscillator start-up time	V _{DD} = 5.0 V ± 10%		—	1.1	2.0	μs
Δ _{FIRCPRE}	CC	T	Fast internal RC oscillator precision after software trimming of f _{FIRC}	T _A = 25 °C		–1	—	+1	%
Δ _{FIRCTRM}	CC	T	Fast internal RC oscillator trimming step	T _A = 25 °C		—	1.6		%
Δ _{FIRCVAR}	CC	P	Fast internal RC oscillator variation in overtemperature and supply with respect to f _{FIRC} at T _A = 25 °C in high-frequency configuration	—		–5	—	+5	%

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

² This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

3.25 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a 128 kHz slow internal RC oscillator. This can be used as the reference clock for the RTC module.

Table 43. Slow internal RC oscillator (128 kHz) electrical characteristics

Symbol	C	Parameter	Conditions ¹	Value			Unit
				Min	Typ	Max	
f _{SIRC}	CC	P	T _A = 25 °C, trimmed	—	128	—	kHz
	SR		—	100	—	150	
I _{SIRC} ²	CC	C	Slow internal RC oscillator low frequency current T _A = 25 °C, trimmed	—	—	5	μA
t _{SIRCSU}	CC	P	Slow internal RC oscillator start-up time T _A = 25 °C, V _{DD} = 5.0 V ± 10%	—	8	12	μs
Δ _{SIRCPRE}	CC	C	Slow internal RC oscillator precision after software trimming of f _{SIRC} T _A = 25 °C	–2	—	+2	%
Δ _{SIRCTRM}	CC	C	Slow internal RC oscillator trimming step	—	2.7	—	
Δ _{SIRCVAR}	CC	C	Slow internal RC oscillator variation in temperature and supply with respect to f _{SIRC} at T _A = 55 °C in high frequency configuration	–10	—	+10	%

3.26 ADC electrical characteristics

3.26.1 Introduction

The device provides a 10-bit Successive Approximation Register (SAR) analog-to-digital converter.

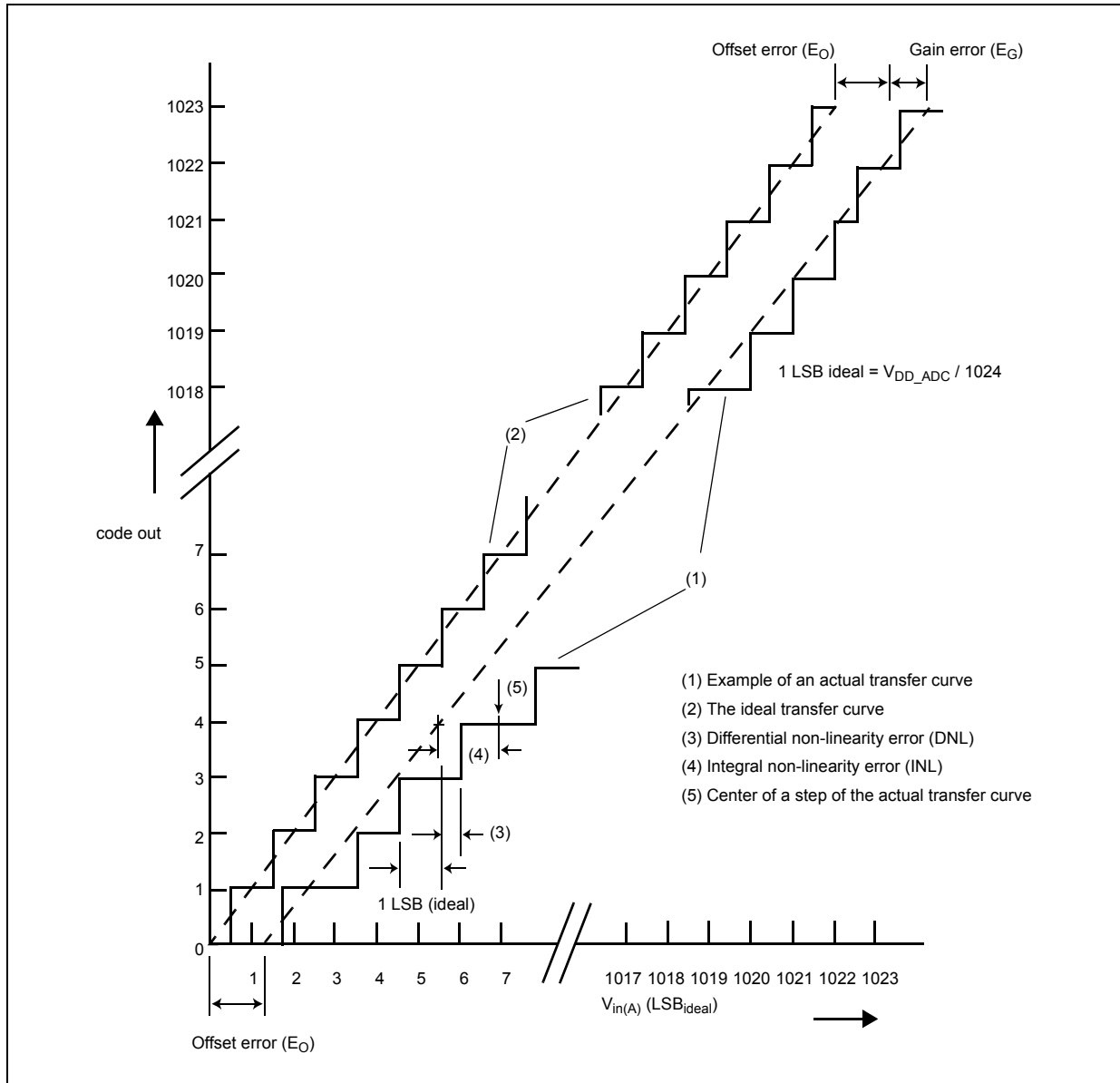


Figure 19. ADC characteristic and error definitions

3.26.2 Input impedance and ADC accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as

Package pinouts and signal descriptions

possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: being C_S and C_{P2} substantially two switched capacitances, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with $C_S + C_{P2}$ equal to 3 pF, a resistance of 330 kΩ is obtained ($R_{EQ} = 1 / (f_c \times (C_S + C_{P2}))$), where f_c represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on $C_S + C_{P2}$) and the sum of $R_S + R_F$, the external circuit must be designed to respect the [Equation 4](#):

Eqn. 4

$$V_A \cdot \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} \text{ LSB}$$

[Equation 4](#) generates a constraint for external network design, in particular on a resistive path.

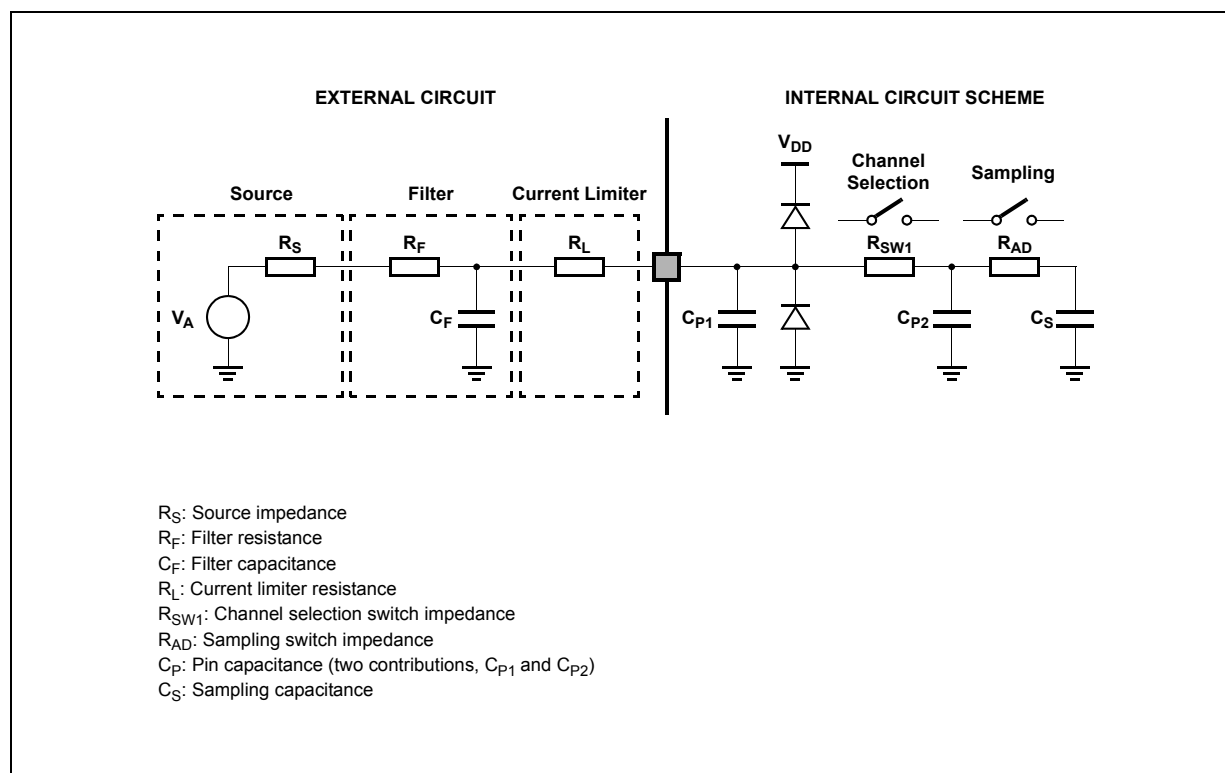


Figure 20. Input equivalent circuit (precise channels)

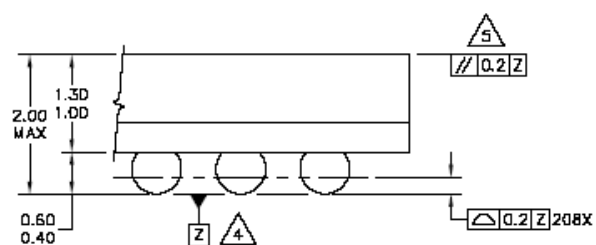
3.26.3 ADC electrical characteristics

Table 44. ADC input leakage current

Symbol	C	Parameter	Conditions	Value			Unit
				Min	Typ	Max	
I _{LKG}	CC	D	Input leakage current T _A = -40 °C No current injection on adjacent pin	—	1	70	nA
				—	1	70	
				—	3	100	
				—	8	200	
				—	45	400	
				—	45	400	

Table 45. ADC conversion characteristics

Symbol		C	Parameter	Conditions ¹	Value			Unit
					Min	Typ	Max	
V _{SS_ADC}	SR	—	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V _{SS}) ²	—	−0.1	—	0.1	V
V _{DD_ADC}	SR	—	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V _{SS})	—	V _{DD} −0.1	—	V _{DD} +0.1	V
V _{AINx}	SR	—	Analog input voltage ³	—	V _{SS_ADC} −0.1	—	V _{DD_ADC} +0.1	V
f _{ADC}	SR	—	ADC analog frequency	—	6	—	32 + 4%	MHz
Δ _{ADC_SYS}	SR	—	ADC digital clock duty cycle (ipg_clk)	ADCLKSEL = 1 ⁴	45	—	55	%
I _{ADCPWD}	SR	—	ADC0 consumption in power down mode	—	—	—	50	μA
I _{ADCRUN}	SR	—	ADC0 consumption in running mode	—	—	—	4	mA
t _{ADC_PU}	SR	—	ADC power up delay	—	—	—	1.5	μs
t _s	CC	T	Sampling time ⁵	f _{ADC} = 32 MHz, INPSAMP = 17	0.5	—		μs
				f _{ADC} = 6 MHz, INPSAMP = 255	—	—	42	
t _c	CC	P	Conversion time ⁶	f _{ADC} = 32 MHz, INPCMP = 2	0.625	—		μs
C _S	CC	D	ADC input sampling capacitance	—	—	—	3	pF
C _{P1}	CC	D	ADC input pin capacitance 1	—	—	—	3	pF
C _{P2}	CC	D	ADC input pin capacitance 2	—	—	—	1	pF



DETAIL K
(ROTATED 90° CLOCKWISE)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. PACKAGE CODE SUMMARY:
MAP BGA: 5253
MAP BGA PGE DIE: 5371

FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1-MM PITCH	DOCUMENT NO: 98ARS238B2W	REV: E
	CASE NUMBER: 1159A-01	28 MAR 2007
	STANDARD: JEDEC MO-151 AAF-1	

Figure 44. 208 MAPBGA package mechanical drawing (2 of 2)

Table 50. Revision history (continued)

Revision	Date	Description of Changes
2 (cont.)	06-Mar-2009	Updated Table 16, Table 17, Table 18, Table 19 and Table 20 Added Section 3.15.4, Output pin transition times Updated Table 23 Updated Figure 8 Updated Table 25 Section 3.17.1, Voltage regulator electrical characteristics: Amended description of LV_PLL Figure 10: Exchanged position of symbols C_{DEC1} and C_{DEC2} Updated Table 26 Added Figure 13 Updated Table 27 and Table 28 Updated Section 3.19, Flash memory electrical characteristics Added Section 3.20, Electromagnetic compatibility (EMC) characteristics Updated Section 3.21, Fast external crystal oscillator (4 to 16 MHz) electrical characteristics Updated Section 3.22, Slow external crystal oscillator (32 kHz) electrical characteristics Updated Table 41, Table 42 and Table 43 Added Section 3.27, On-chip peripherals Added Table 44 Updated Table 45 Updated Table 47 Added Section Appendix A, Abbreviations

Table 50. Revision history (continued)

Revision	Date	Description of Changes
6	15-Mar-2010	In the "Introduction" section, relocated a note. In the "MPC5604B/C device comparison" table, added footnote regarding SCI and CAN. In the "Absolute maximum ratings" table, removed the min value of V_{IN} relative to V_{DD}. In the "Recommended operating conditions (3.3 V)" table: • T_A C-Grade Part, T_J C-Grade Part, T_A V-Grade Part, T_J V-Grade Part, T_A M-Grade Part, T_J M-Grade Part: added new rows. • T_{VDD}: made single row. In the "LQFP thermal characteristics" table, added more rows. Removed "208 MAPBGA thermal characteristics" table. In the "I/O consumption" table: • Removed I_{DYNSEG} row. • Added "I/O weight" table. In the "Voltage regulator electrical characteristics" table: • Updated the values. • Removed $I_{VREGREF}$ and $I_{VREDLVD12}$. • Added a note about I_{DD_BC}. In the "Low voltage monitor electrical characteristics" table: • Updated V_{PORH} values. • Updated $V_{LVDLVCORL}$ value. Entirely updated the "Low voltage power domain electrical characteristics" table. In the "Program and erase specifications" table, inserted T_{eslat} row. Entirely updated the "Flash power supply DC electrical characteristics" table. Entirely updated the "Start-up time/Switch-off time" table. In the "Crystal oscillator and resonator connection scheme" figure, relocated a note. In the "Slow external crystal oscillator (32 kHz) electrical characteristics" table: • Removed g_{mSXOSC} row. • Inserted values of $I_{SXOSCBIAS}$. Entirely updated the "Fast internal RC oscillator (16 MHz) electrical characteristics" table. In the "ADC conversion characteristics" table: updated the description of the conditions of t_{ADC_PU} and t_{ADC_S}. Entirely updated the "DSPI characteristics" table. In the "Orderable part number summary" table, modified some orderable part number. Updated the "Commercial product code structure" figure. Removed the note about the condition from "Flash read access timing" table Removed the notes that assert the values need to be confirmed before validation Exchanged the order of "LQFP 100-pin configuration" and "LQFP 144-pin configuration" Exchanged the order of "LQFP 100-pin package mechanical drawing" and "LQFP 144-pin package mechanical drawing"