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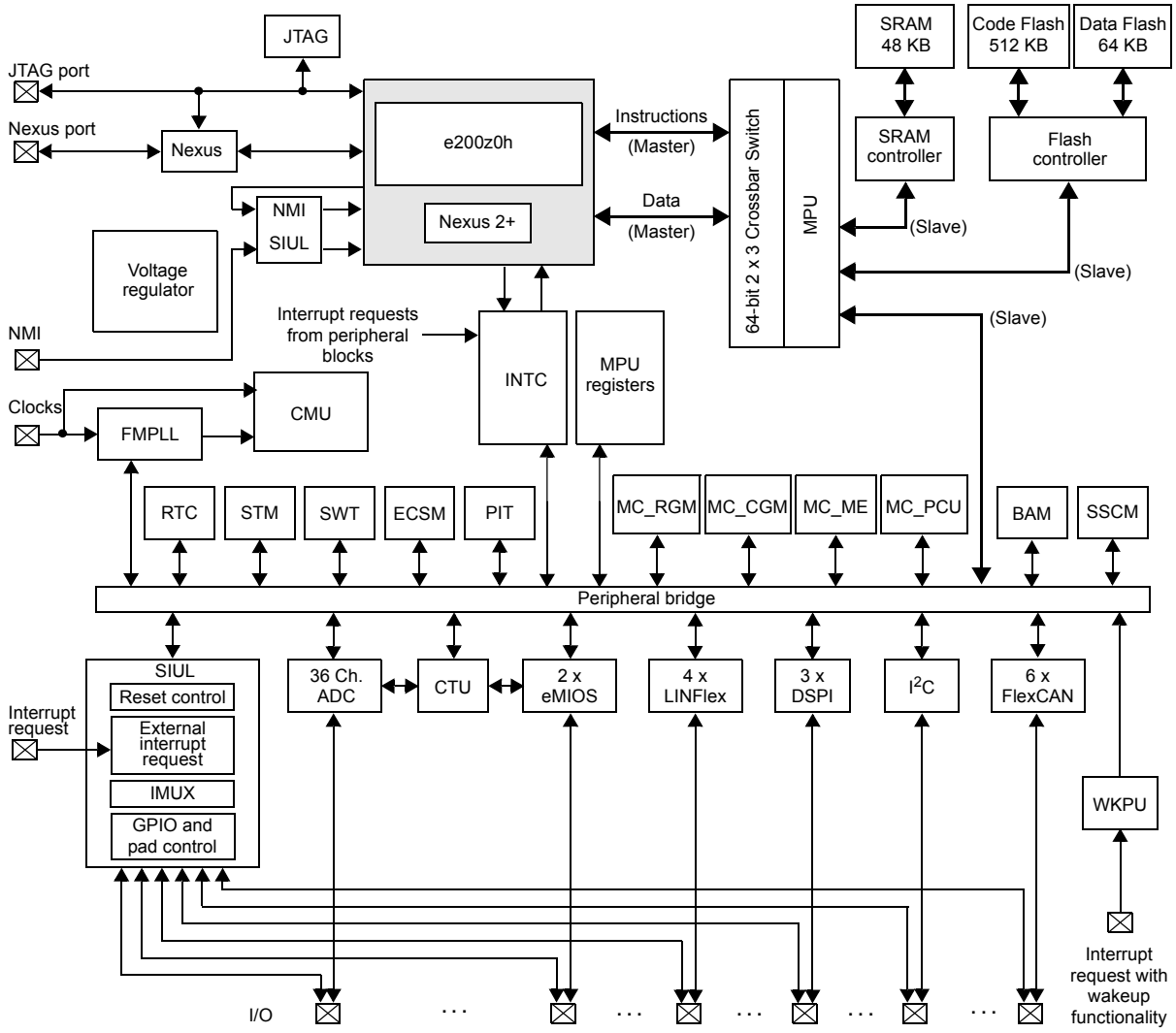
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	123
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 36x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5604bavlq6

1 Feature set dependent on selected peripheral multiplexing—table shows example implementation
2 Based on 125 °C ambient operating temperature
3 See the eMIOS section of the device reference manual for information on the channel configuration and functions.
4 IC – Input Capture; OC – Output Compare; PWM – Pulse Width Modulation; MC – Modulus counter
5 SCI0, SCI1 and SCI2 are available. SCI3 is not available.
6 CAN0, CAN1 are available. CAN2, CAN3, CAN4 and CAN5 are not available.
7 CAN0, CAN1 and CAN2 are available. CAN3, CAN4 and CAN5 are not available.
8 I/O count based on multiplexing with peripherals
9 208 MAPBGA available only as development package for Nexus2+

2 Block diagram

Figure 1 shows a top-level block diagram of the MPC5604B/C device series.



Legend:

ADC	Analog-to-Digital Converter
BAM	Boot Assist Module
FlexCAN	Controller Area Network
CMU	Clock Monitor Unit
CTU	Cross Triggering Unit
DSPI	Deserial Serial Peripheral Interface
eMIOS	Enhanced Modular Input Output System
FMPLL	Frequency-Modulated Phase-Locked Loop
I^2C	Inter-integrated Circuit Bus
IMUX	Internal Multiplexer
INTC	Interrupt Controller
JTAG	JTAG controller
LINFlex	Serial Communication Interface (LIN support)
ECSM	Error Correction Status Module
MC_CGM	Clock Generation Module
MC_ME	Mode Entry Module
MC_PCU	Power Control Unit
MC_RGM	Reset Generation Module
MPU	Memory Protection Unit
Nexus	Nexus Development Interface (NDI) Level
NMI	Non-Maskable Interrupt
PIT	Periodic Interrupt Timer
RTC	Real-Time Clock
SIUL	System Integration Unit Lite
SRAM	Static Random-Access Memory
SSCM	System Status Configuration Module
STM	System Timer Module
SWT	Software Watchdog Timer
WKPU	Wakeup Unit

Figure 1. MPC5604B/C block diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	PC[8]	PC[13]	NC	NC	PH[8]	PH[4]	PC[5]	PC[0]	NC	NC	PC[2]	NC	PE[15]	NC	NC	NC	A
B	PC[9]	PB[2]	NC	PC[12]	PE[6]	PH[5]	PC[4]	PH[9]	PH[10]	NC	PC[3]	PG[11]	PG[15]	PG[14]	PA[11]	PA[10]	B
C	PC[14]	VDD_HV	PB[3]	PE[7]	PH[7]	PE[5]	PE[3]	VSS_LV	PC[1]	NC	PA[5]	NC	PE[14]	PE[12]	PA[9]	PA[8]	C
D	NC	NC	PC[15]	NC	PH[6]	PE[4]	PE[2]	VDD_LV	VDD_HV	NC	PA[6]	NC	PG[10]	PF[14]	PE[13]	PA[7]	D
E	PG[4]	PG[5]	PG[3]	PG[2]									PG[1]	PG[0]	PF[15]	VDD_HV	E
F	PE[0]	PA[2]	PA[1]	PE[1]									PH[0]	PH[1]	PH[3]	PH[2]	F
G	PE[9]	PE[8]	PE[10]	PA[0]			VSS_HV	VSS_HV	VSS_HV	VSS_HV			VDD_HV	NC	NC	MSEO	G
H	VSS_HV	PE[11]	VDD_HV	NC			VSS_HV	VSS_HV	VSS_HV	VSS_HV			MDO3	MDO2	MDO0	MDO1	H
J	RESET	VSS_LV	NC	NC			VSS_HV	VSS_HV	VSS_HV	VSS_HV			NC	NC	NC	NC	J
K	EVTI	NC	VDD_BV	VDD_LV			VSS_HV	VSS_HV	VSS_HV	VSS_HV			NC	PG[12]	PA[3]	PG[13]	K
L	PG[9]	PG[8]	NC	EVTO									PB[15]	PD[15]	PD[14]	PB[14]	L
M	PG[7]	PG[6]	PC[10]	PC[11]									PB[13]	PD[13]	PD[12]	PB[12]	M
N	PB[1]	PF[9]	PB[0]	NC	NC	PA[4]	VSS_LV	EXTAL	VDD_HV	PF[0]	PF[4]	NC	PB[11]	PD[10]	PD[9]	PD[11]	N
P	PF[8]	NC	PC[7]	NC	NC	PA[14]	VDD_LV	XTAL	PB[10]	PF[1]	PF[5]	PD[0]	PD[3]	VDD_HV_ADC	PB[6]	PB[7]	P
R	PF[12]	PC[6]	PF[10]	PF[11]	VDD_HV	PA[15]	PA[13]	NC	OSC32K_XTAL	PF[3]	PF[7]	PD[2]	PD[4]	PD[7]	VSS_HV_ADC	PB[5]	R
T	NC	NC	NC	MCKO	NC	PF[13]	PA[12]	NC	OSC32K_EXTAL	PF[2]	PF[6]	PD[1]	PD[5]	PD[6]	PD[8]	PB[4]	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Note: 208 MAPBGA available only as development package for Nexus 2+.

NC = Not connected

Figure 6. 208 MAPBGA configuration

3.2 Pad configuration during reset phases

All pads have a fixed configuration under reset.

During the power-up phase, all pads are forced to tristate.

After power-up phase, all pads are forced to tristate with the following exceptions:

- PA[9] (FAB) is pull-down. Without external strong pull-up the device starts fetching from flash.
- PA[8] (ABS[0]) is pull-up.
- RESET pad is driven low. This is pull-up only after PHASE2 reset completion.
- JTAG pads (TCK, TMS and TDI) are pull-up whilst TDO remains tristate.
- Precise ADC pads (PB[7:4] and PD[11:0]) are left tristate (no output buffer available).
- Main oscillator pads (EXTAL, XTAL) are tristate.
- Nexus output pads (MDO[*n*], MCKO, EVTO, MSEO) are forced to output.

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 —	GPIO[2] E0UC[2] — — WKPU[3][4]	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	3	3	5	9	F2
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 —	GPIO[3] E0UC[3] — — EIRQ[0]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	43	39	68	90	K15
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 —	GPIO[4] E0UC[4] — — WKPU[9][4]	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	20	20	29	43	N6
PA[5]	PCR[5]	AF0 AF1 AF2 AF3	GPIO[5] E0UC[5] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	51	51	79	118	C11
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 —	GPIO[6] E0UC[6] — — EIRQ[1]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	52	52	80	119	D11
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 —	GPIO[7] E0UC[7] LIN3TX — EIRQ[2]	SIUL eMIOS_0 LINFlex_3 — SIUL	I/O I/O O — I	S	Tristate	44	44	71	104	D16
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — N/A[6] —	GPIO[8] E0UC[8] — — EIRQ[3] ABS[0] LIN3RX	SIUL eMIOS_0 — — SIUL BAM LINFlex_3	I/O I/O — — I I I	S	Input, weak pull-up	45	45	72	105	C16
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 N/A[6]	GPIO[9] E0UC[9] — — FAB	SIUL eMIOS_0 — — BAM	I/O I/O — — I	S	Pull-down	46	46	73	106	C15

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — —	GPIO[26] — — — ANS[2] WKPU[8][4]	SIUL — — — ADC WKPU	I/O — — — I I	J	Tristate	31	31	40	54	P9
PB[11][8]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ANS[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — I/O I	J	Tristate	38	36	59	81	N13
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ANX[0]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	39	—	61	83	M16
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ANX[1]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	40	—	63	85	M13
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ANX[2]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	41	37	65	87	L16
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ANX[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	42	38	67	89	L13
PC[0][9]	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M	Input, weak pull-up	59	59	87	126	A8
PC[1][9]	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO[10] —	SIUL — JTAGC —	I/O — O —	M	Tristate	54	54	82	121	C9

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PF[2]	PCR[82]	AF0 AF1 AF2 AF3 —	GPIO[82] E0UC[12] CS0_2 — ANS[10]	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O I/O — I	J	Tristate	—	—	—	57	T10
PF[3]	PCR[83]	AF0 AF1 AF2 AF3 —	GPIO[83] E0UC[13] CS1_2 — ANS[11]	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O O — I	J	Tristate	—	—	—	58	R10
PF[4]	PCR[84]	AF0 AF1 AF2 AF3 —	GPIO[84] E0UC[14] CS2_2 — ANS[12]	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O O — I	J	Tristate	—	—	—	59	N11
PF[5]	PCR[85]	AF0 AF1 AF2 AF3 —	GPIO[85] E0UC[22] CS3_2 — ANS[13]	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O O — I	J	Tristate	—	—	—	60	P11
PF[6]	PCR[86]	AF0 AF1 AF2 AF3 —	GPIO[86] E0UC[23] — — ANS[14]	SIUL eMIOS_0 — — ADC	I/O I/O — — I	J	Tristate	—	—	—	61	T11
PF[7]	PCR[87]	AF0 AF1 AF2 AF3 —	GPIO[87] — — — ANS[15]	SIUL — — — ADC	I/O — — — I	J	Tristate	—	—	—	62	R11
PF[8]	PCR[88]	AF0 AF1 AF2 AF3	GPIO[88] CAN3TX[14] CS4_0 CAN2TX[15]	SIUL FlexCAN_3 DSPI_0 FlexCAN_2	I/O O O O	M	Tristate	—	—	—	34	P1
PF[9]	PCR[89]	AF0 AF1 AF2 AF3 — —	GPIO[89] — CS5_0 — CAN2RX[15] CAN3RX[14]	SIUL — DSPI_0 — FlexCAN_2 FlexCAN_3	I/O — O — I I	S	Tristate	—	—	—	33	N2

[1] Default manufacturing value is ‘1’. Value can be programmed by customer in Shadow Flash.

3.11.2 NVUSRO[OSCILLATOR_MARGIN] field description

The fast external crystal oscillator consumption is dependent on the OSCILLATOR_MARGIN bit value. Table 10 shows how NVUSRO[OSCILLATOR_MARGIN] controls the device configuration.

Table 10. OSCILLATOR_MARGIN field description

Value[1]	Description
0	Low consumption configuration (4 MHz/8 MHz)
1	High margin configuration (4 MHz/16 MHz)

[1] Default manufacturing value is ‘1’. Value can be programmed by customer in Shadow Flash.

3.11.3 NVUSRO[WATCHDOG_EN] field description

The watchdog enable/disable configuration after reset is dependent on the WATCHDOG_EN bit value. Table 11 shows how NVUSRO[WATCHDOG_EN] controls the device configuration.

Table 11. WATCHDOG_EN field description

Value[1]	Description
0	Disable after reset
1	Enable after reset

[1] Default manufacturing value is ‘1’. Value can be programmed by customer in Shadow Flash.

3.14 Thermal characteristics

3.14.1 Package thermal characteristics

Table 15. LQFP thermal characteristics[1]

Symbol		C	Parameter	Conditions[2]	Pin count	Value	Unit
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection[3]	Single-layer board - 1s	64	60	°C/W
					100	64	
					144	64	
				Four-layer board - 2s2p	64	42	
					100	51	
					144	49	
$R_{\theta JB}$	CC	D	Thermal resistance, junction-to-board[4]	Single-layer board - 1s	64	24	°C/W
					100	36	
					144	37	
				Four-layer board - 2s2p	64	24	
					100	34	
					144	35	
$R_{\theta JC}$	CC	D	Thermal resistance, junction-to-case[5]	Single-layer board - 1s	64	11	°C/W
					100	22	
					144	22	
				Four-layer board - 2s2p	64	11	
					100	22	
					144	22	
Ψ_{JB}	CC	D	Junction-to-board thermal characterization parameter, natural convection	Single-layer board - 1s	64	TBD	°C/W
					100	33	
					144	34	
				Four-layer board - 2s2p	64	TBD	
					100	34	
					144	35	
Ψ_{JC}	CC	D	Junction-to-case thermal characterization parameter, natural convection	Single-layer board - 1s	64	TBD	°C/W
					100	9	
					144	10	
				Four-layer board - 2s2p	64	TBD	
					100	9	
					144	10	

[1] Thermal characteristics are based on simulation.

Table 24. I/O weight[1] (continued)

Supply segment			Pad	144/100 LQFP				64 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
144 LQFP	100 LQFP	64 LQFP[2]		SRC[3] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
2	2	2	PB[9]	1%	—	1%	—	1%	—	1%	—
			PB[8]	1%	—	1%	—	1%	—	1%	—
			PB[10]	6%	—	7%	—	6%	—	7%	—
	—	—	PF[0]	6%	—	7%	—	—	—	—	—
	—	—	PF[1]	7%	—	8%	—	—	—	—	—
	—	—	PF[2]	7%	—	8%	—	—	—	—	—
	—	—	PF[3]	7%	—	9%	—	—	—	—	—
	—	—	PF[4]	8%	—	9%	—	—	—	—	—
	—	—	PF[5]	8%	—	10%	—	—	—	—	—
	—	—	PF[6]	8%	—	10%	—	—	—	—	—
	—	—	PF[7]	9%	—	10%	—	—	—	—	—
	2	—	PD[0]	1%	—	1%	—	—	—	—	—
		—	PD[1]	1%	—	1%	—	—	—	—	—
		—	PD[2]	1%	—	1%	—	—	—	—	—
		—	PD[3]	1%	—	1%	—	—	—	—	—
		—	PD[4]	1%	—	1%	—	—	—	—	—
		—	PD[5]	1%	—	1%	—	—	—	—	—
		—	PD[6]	1%	—	1%	—	—	—	—	—
		—	PD[7]	1%	—	1%	—	—	—	—	—
		—	PD[8]	1%	—	1%	—	—	—	—	—
		2	PB[4]	1%	—	1%	—	1%	—	1%	—
			PB[5]	1%	—	1%	—	1%	—	2%	—
			PB[6]	1%	—	1%	—	1%	—	2%	—
			PB[7]	1%	—	1%	—	1%	—	2%	—
		—	PD[9]	1%	—	1%	—	—	—	—	—
		—	PD[10]	1%	—	1%	—	—	—	—	—
		—	PD[11]	1%	—	1%	—	—	—	—	—
		2	PB[11]	11%	—	13%	—	17%	—	21%	—
		—	PD[12]	11%	—	13%	—	—	—	—	—
		2	PB[12]	11%	—	13%	—	18%	—	21%	—
		—	PD[13]	10%	—	12%	—	—	—	—	—

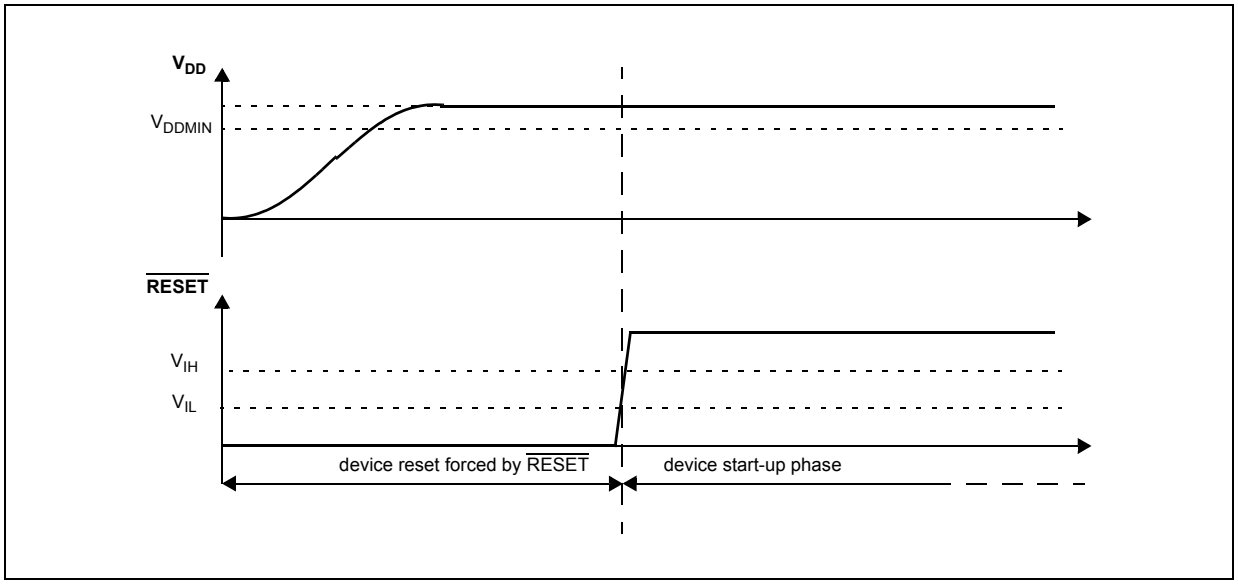


Figure 8. Start-up reset requirements

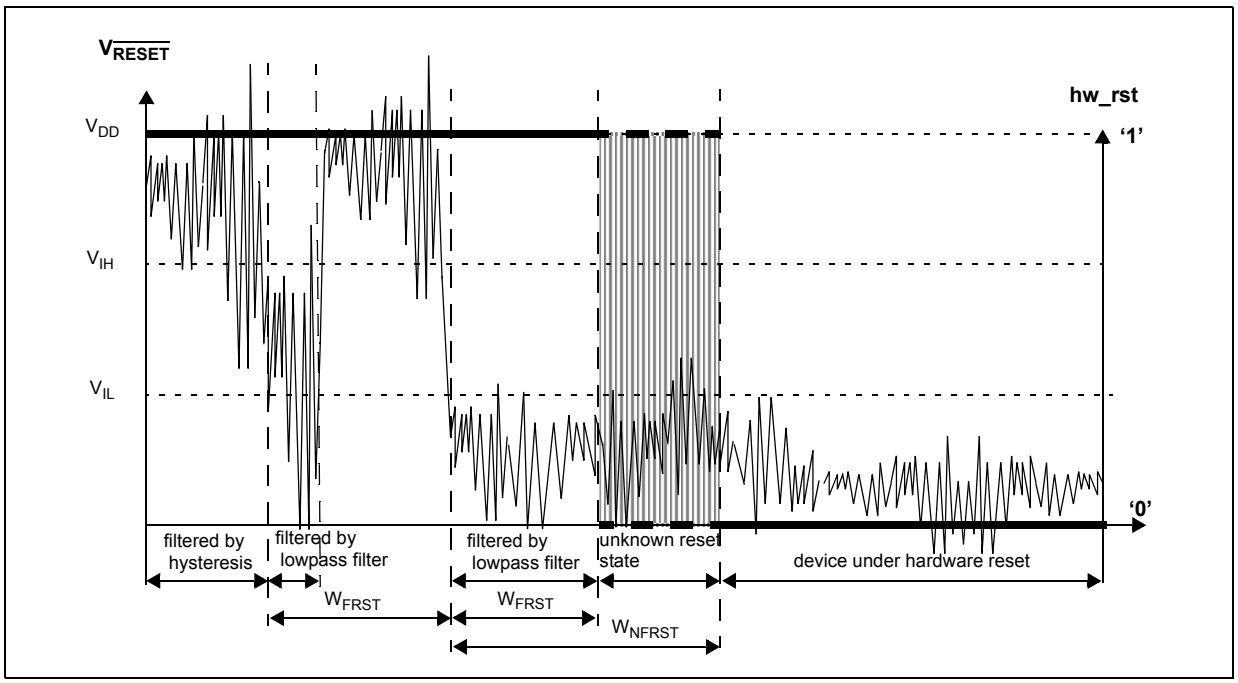


Figure 9. Noise filtering on reset signal

Table 25. Reset electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input High Level CMOS (Schmitt Trigger)	—	$0.65V_{DD}$	—	$V_{DD}+0.4$	V

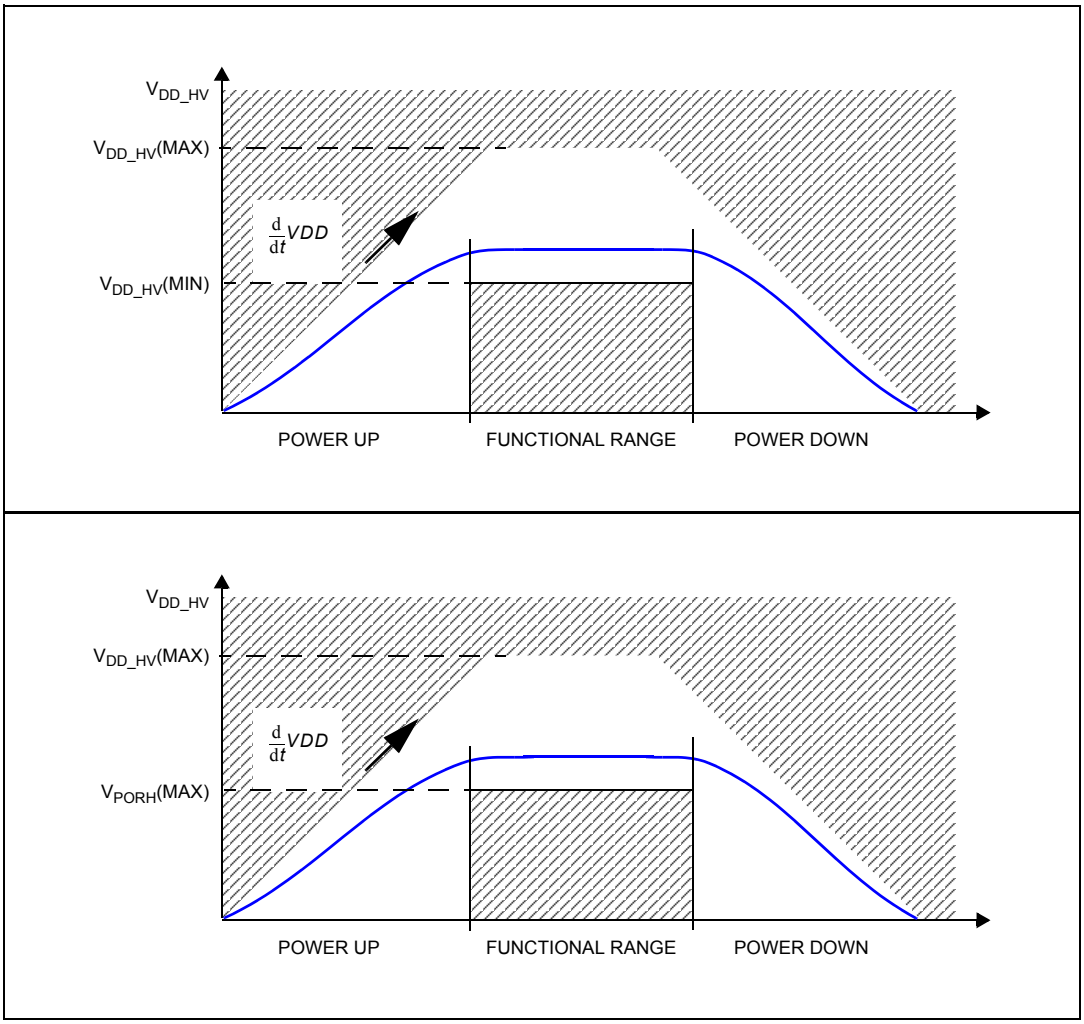


Figure 11. V_{DD_HV} and V_{DD_BV} maximum slope

When STANDBY mode is used, further constraints are applied to the both V_{DD_HV} and V_{DD_BV} in order to guarantee correct regulator function during STANDBY exit. This is described on Figure 12.

STANDBY regulator constraints should normally be guaranteed by implementing equivalent of CSTDBY capacitance on application board (capacitance and ESR typical values), but would actually depend on exact characteristics of application external regulator.

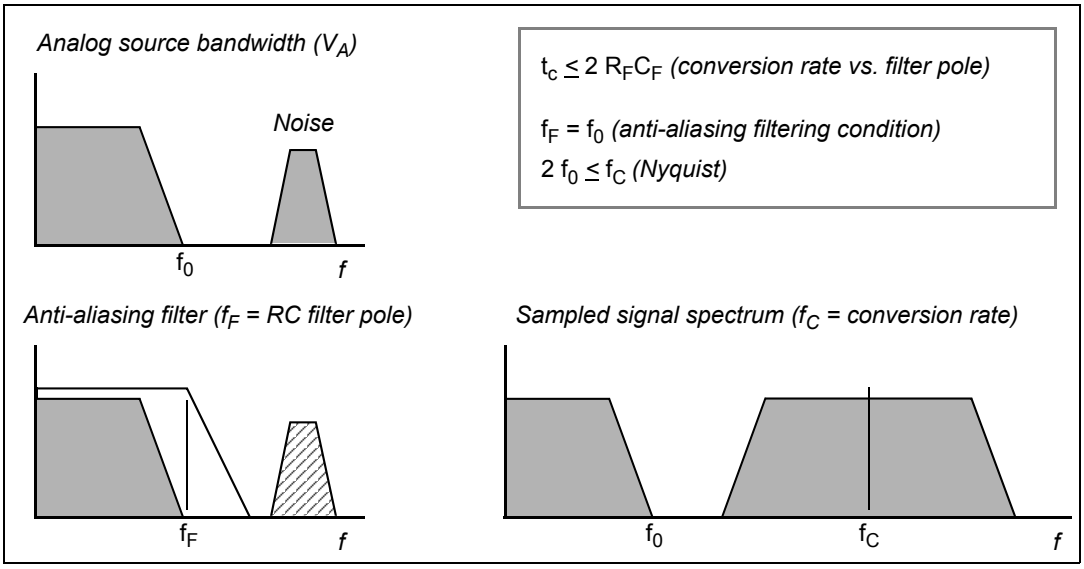


Figure 23. Spectral representation of input signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (t_c). Again the conversion period t_c is longer than the sampling time t_s, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter $R_F C_F$ is definitively much higher than the sampling time t_s, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive Equation 11 between the ideal and real sampled voltage on C_S:

Eqn. 11

$$\frac{V_{A2}}{V_A} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Eqn. 12

$$C_F > 2048 \bullet C_S$$

3.26.3 ADC electrical characteristics

Table 44. ADC input leakage current

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
I_{LKG}	CC	D	Input leakage current	T_A = –40 °C	No current injection on adjacent pin	—	1	70	nA
		D		T_A = 25 °C		—	1	70	
		D		T_A = 85 °C		—	3	100	
		D		T_A = 105 °C		—	8	200	
		P		T_A = 125 °C		—	45	400	

Table 45. ADC conversion characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SS_ADC}	SR	—	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS})[2]	—	–0.1	—	0.1	V
V_{DD_ADC}	SR	—	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	V_{DD}–0.1	—	V_{DD}+0.1	V
V_{AINx}	SR	—	Analog input voltage[3]	—	V_{SS_ADC}–0.1	—	V_{DD_ADC}+0.1	V
f_{ADC}	SR	—	ADC analog frequency	—	6	—	32 + 4%	MHz
Δ_{ADC_SYS}	SR	—	ADC digital clock duty cycle (ipg_clk)	ADCLKSEL = 1[4]	45	—	55	%
I_{ADCPWD}	SR	—	ADC0 consumption in power down mode	—	—	—	50	µA
I_{ADCRUN}	SR	—	ADC0 consumption in running mode	—	—	—	4	mA
t_{ADC_PU}	SR	—	ADC power up delay	—	—	—	1.5	µs
t_s	CC	T	Sampling time[5]	f_{ADC} = 32 MHz, INPSAMP = 17	0.5	—		µs
				f_{ADC} = 6 MHz, INPSAMP = 255	—	—	42	
t_c	CC	P	Conversion time[6]	f_{ADC} = 32 MHz, INPCMP = 2	0.625	—		µs
C_S	CC	D	ADC input sampling capacitance	—	—	—	3	pF
C_{P1}	CC	D	ADC input pin capacitance 1	—	—	—	3	pF
C_{P2}	CC	D	ADC input pin capacitance 2	—	—	—	1	pF

3.27 On-chip peripherals

3.27.1 Current consumption

Table 46. On-chip peripherals current consumption[1]

Symbol		C	Parameter	Conditions		Typical value[2]	Unit
$I_{DD\_BV(CAN)}$	CC	T	CAN (FlexCAN) supply current on VDD_BV	Bitrate: 500 Kbyte/s	Total (static + dynamic) consumption: • FlexCAN in loop-back mode • XTAL @ 8 MHz used as CAN engine clock source • Message sending period is 580 µs	8 * f_{periph} + 85	µA
				Bitrate: 125 Kbyte/s		8 * f_{periph} + 27	
$I_{DD\_BV(eMIOS)}$	CC	T	eMIOS supply current on VDD_BV	Static consumption: • eMIOS channel OFF • Global prescaler enabled		29 * f_{periph}	µA
				Dynamic consumption: • It does not change varying the frequency (0.003 mA)		3	
$I_{DD\_BV(SCI)}$	CC	T	SCI (LINFlex) supply current on VDD_BV	Total (static + dynamic) consumption: • LIN mode • Baudrate: 20 Kbyte/s		5 * f_{periph} + 31	µA
$I_{DD\_BV(SPI)}$	CC	T	SPI (DSPI) supply current on VDD_BV	Ballast static consumption (only clocked)		1	µA
				Ballast dynamic consumption (continuous communication): • Baudrate: 2 Mbit/s • Transmission every 8 µs • Frame: 16 bits		16 * f_{periph}	
$I_{DD\_BV(ADC)}$	CC	T	ADC supply current on VDD_BV	V_{DD} = 5.5 V	Ballast static consumption (no conversion)	41 * f_{periph}	µA
					Ballast dynamic consumption (continuous conversion)[3]	5 * f_{periph}	
$I_{DD\_HV\_ADC(ADC)}$	CC	T	ADC supply current on VDD_HV_ADC	V_{DD} = 5.5 V	Analog static consumption (no conversion)	2 * f_{periph}	µA
					Analog dynamic consumption (continuous conversion)	75 * f_{periph} + 32	
$I_{DD\_HV(FLASH)}$	CC	T	Code Flash + Data Flash supply current on VDD_HV	V_{DD} = 5.5 V	—	8.21	mA
$I_{DD\_HV(PLL)}$	CC	T	PLL supply current on VDD_HV	V_{DD} = 5.5 V	—	30 * f_{periph}	µA

1 Operating conditions: T_A = 25 °C, f_{periph} = 8 MHz to 64 MHz

2 f_{periph} is an absolute value.

3.27.2 DSPI characteristics

Table 47. DSPI characteristics[1]

No.	Symbol		C	Parameter		DSPI0/DSPI1			DSPI2			Unit
						Min	Typ	Max	Min	Typ	Max	
1	t_{SCK}	SR	D	SCK cycle time	Master mode (MTFE = 0)	125	—	—	333	—	—	ns
			D		Slave mode (MTFE = 0)	125	—	—	333	—	—	
			D		Master mode (MTFE = 1)	83	—	—	125	—	—	
			D		Slave mode (MTFE = 1)	83	—	—	125	—	—	
—	f_{DSPI}	SR	D	DSPI digital controller frequency		—	—	f_{CPU}	—	—	f_{CPU}	MHz
—	Δt_{CSC}	CC	D	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1→0	Master mode	—	—	130[2]	—	—	15[3]	ns
—	Δt_{ASC}	CC	D	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1→1	Master mode	—	—	130[3]	—	—	130[3]	ns
2	t_{CSCext}[4]	SR	D	CS to SCK delay	Slave mode	32	—	—	32	—	—	ns
3	t_{ASCext}[5]	SR	D	After SCK delay	Slave mode	$1/f_{DSPI} + 5$	—	—	$1/f_{DSPI} + 5$	—	—	ns
4	t_{SDC}	CC	D	SCK duty cycle	Master mode	—	$t_{SCK}/2$	—	—	$t_{SCK}/2$	—	ns
		SR	D		Slave mode	$t_{SCK}/2$	—	—	$t_{SCK}/2$	—	—	
5	t_A	SR	D	Slave access time	Slave mode	—	—	$1/f_{DSPI} + 70$	—	—	$1/f_{DSPI} + 130$	ns
6	t_{DI}	SR	D	Slave SOUT disable time	Slave mode	7	—	—	7	—	—	ns
7	t_{PCSC}	SR	D	PCSx to $\overline{PCSS}$ time		0	—	—	0	—	—	ns
8	t_{PASC}	SR	D	$\overline{PCSS}$ to PCSx time		0	—	—	0	—	—	ns
9	t_{SUI}	SR	D	Data setup time for inputs	Master mode	43	—	—	145	—	—	ns
					Slave mode	5	—	—	5	—	—	

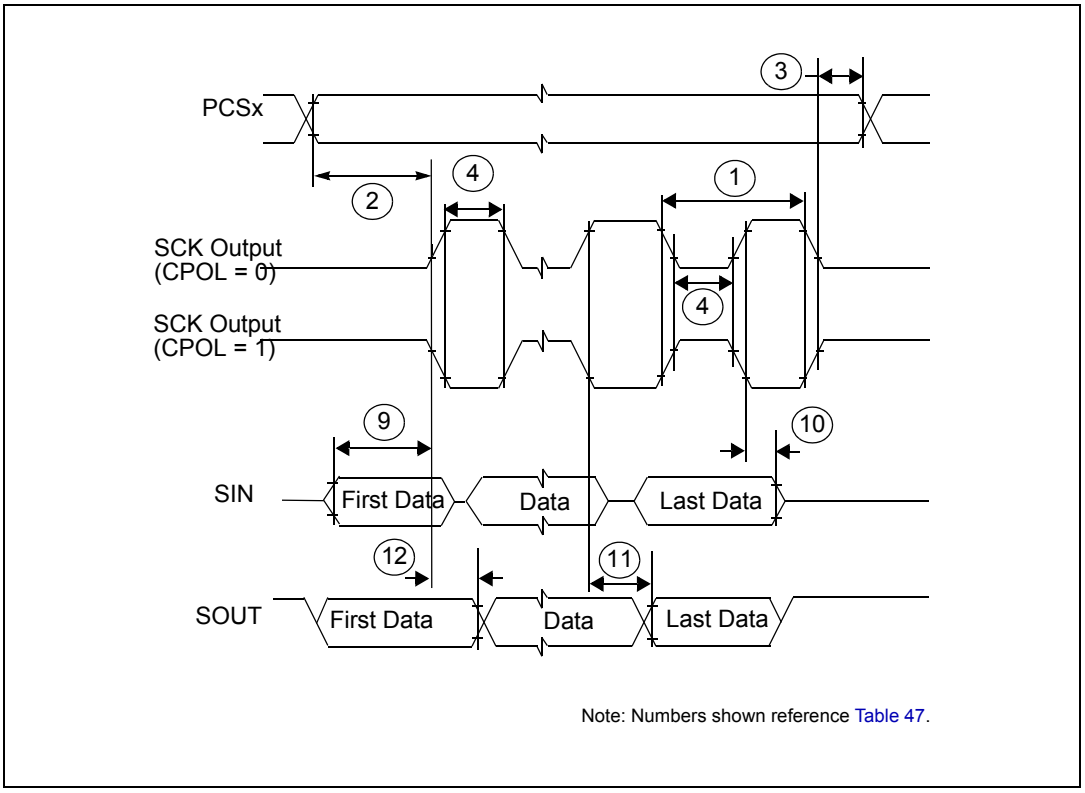


Figure 28. DSPI modified transfer format timing – master, CPHA = 0

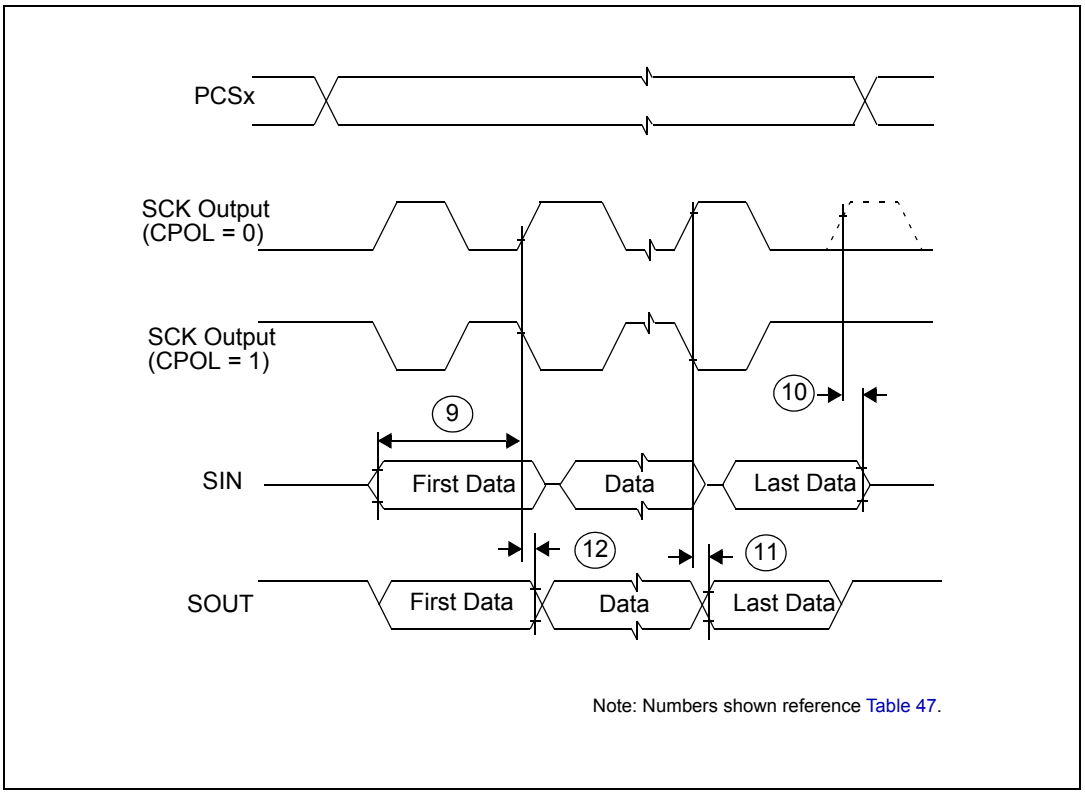


Figure 29. DSPI modified transfer format timing – master, CPHA = 1

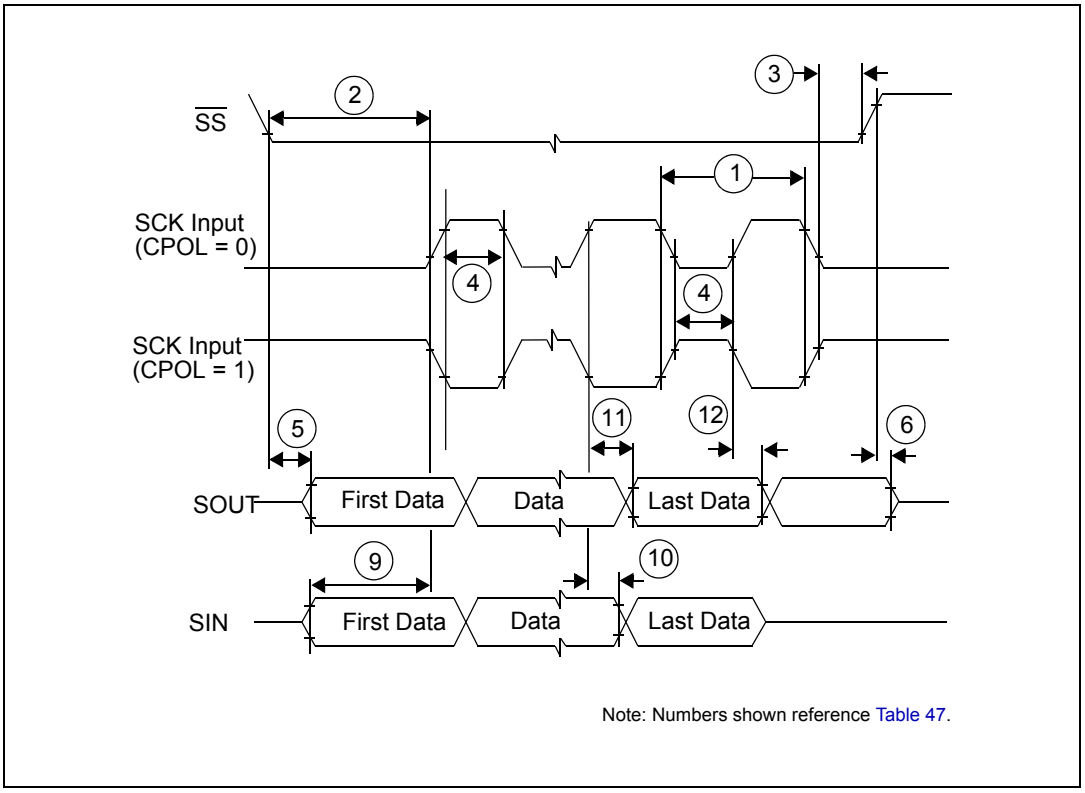


Figure 30. DSPI modified transfer format timing – slave, CPHA = 0

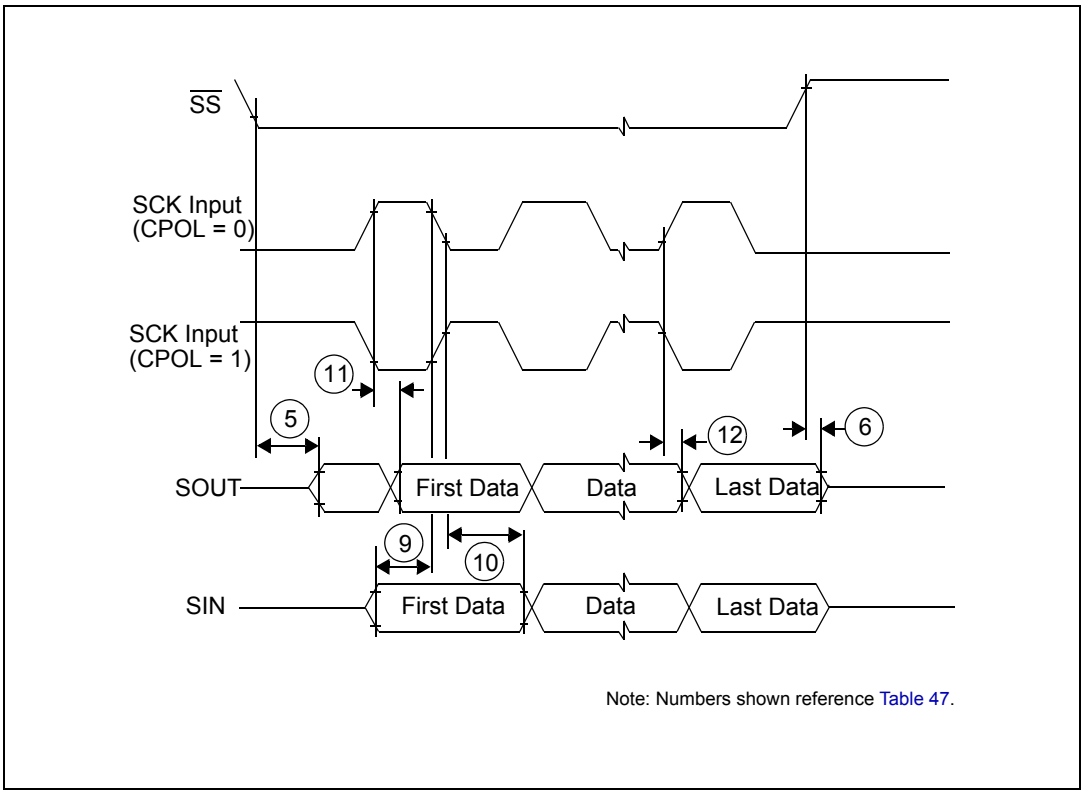


Figure 31. DSPI modified transfer format timing – slave, CPHA = 1

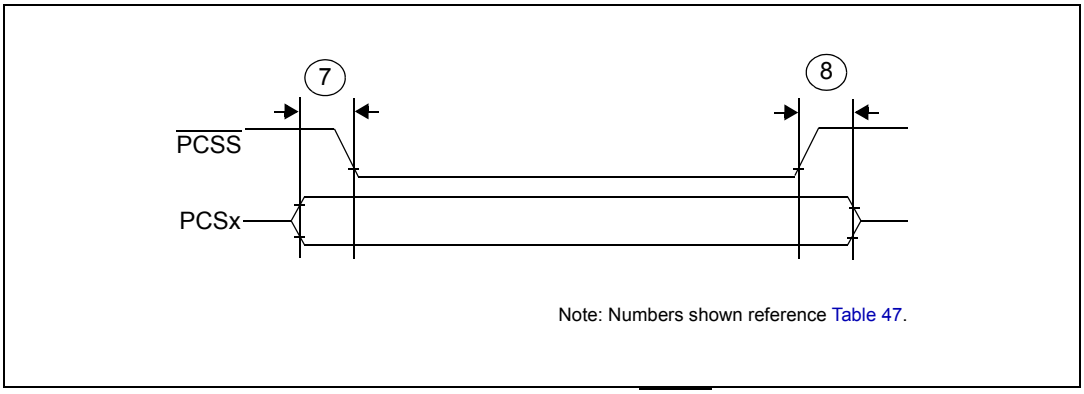


Figure 32. DSPI PCS strobe (PCSS) timing

3.27.3 Nexus characteristics

Table 48. Nexus characteristics

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{TCYC}	CC	D	TCK cycle time	64	—	—	ns
2	t_{MCYC}	CC	D	MCKO cycle time	32	—	—	ns
3	t_{MDOV}	CC	D	MCKO low to MDO data valid	—	—	8	ns
4	t_{MSEOV}	CC	D	MCKO low to MSEO_b data valid	—	—	8	ns
5	t_{EVTOV}	CC	D	MCKO low to EVTO data valid	—	—	8	ns
10	t_{NTDIS}	CC	D	TDI data setup time	15	—	—	ns
	t_{NTMSS}	CC	D	TMS data setup time	15	—	—	ns
11	t_{NTDIH}	CC	D	TDI data hold time	5	—	—	ns
	t_{NTMSH}	CC	D	TMS data hold time	5	—	—	ns
12	t_{TDOV}	CC	D	TCK low to TDO data valid	35	—	—	ns
13	t_{TDOI}	CC	D	TCK low to TDO data invalid	6	—	—	ns

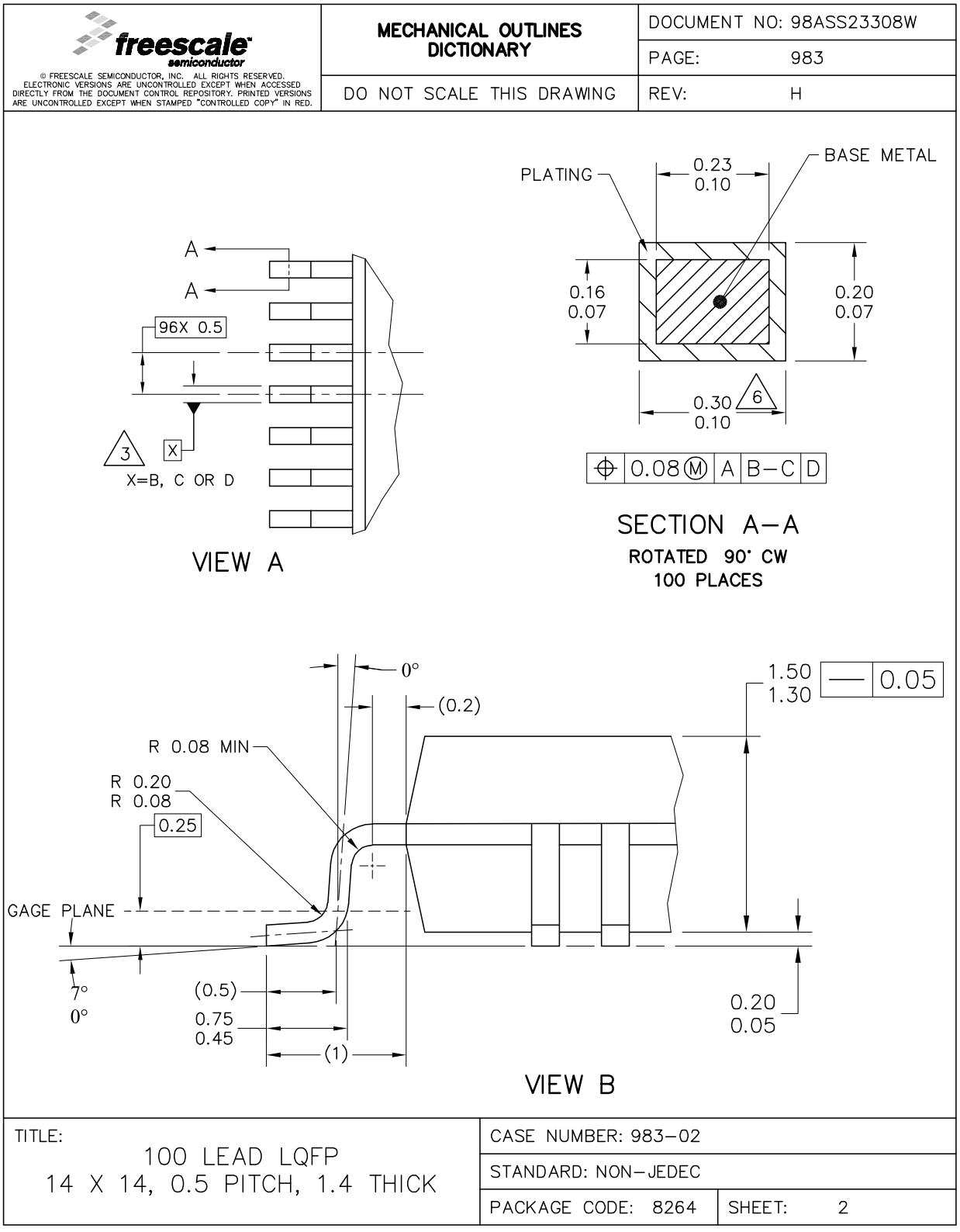


Figure 39. 100 LQFP package mechanical drawing (2 of 3)

4.1.3 144 LQFP

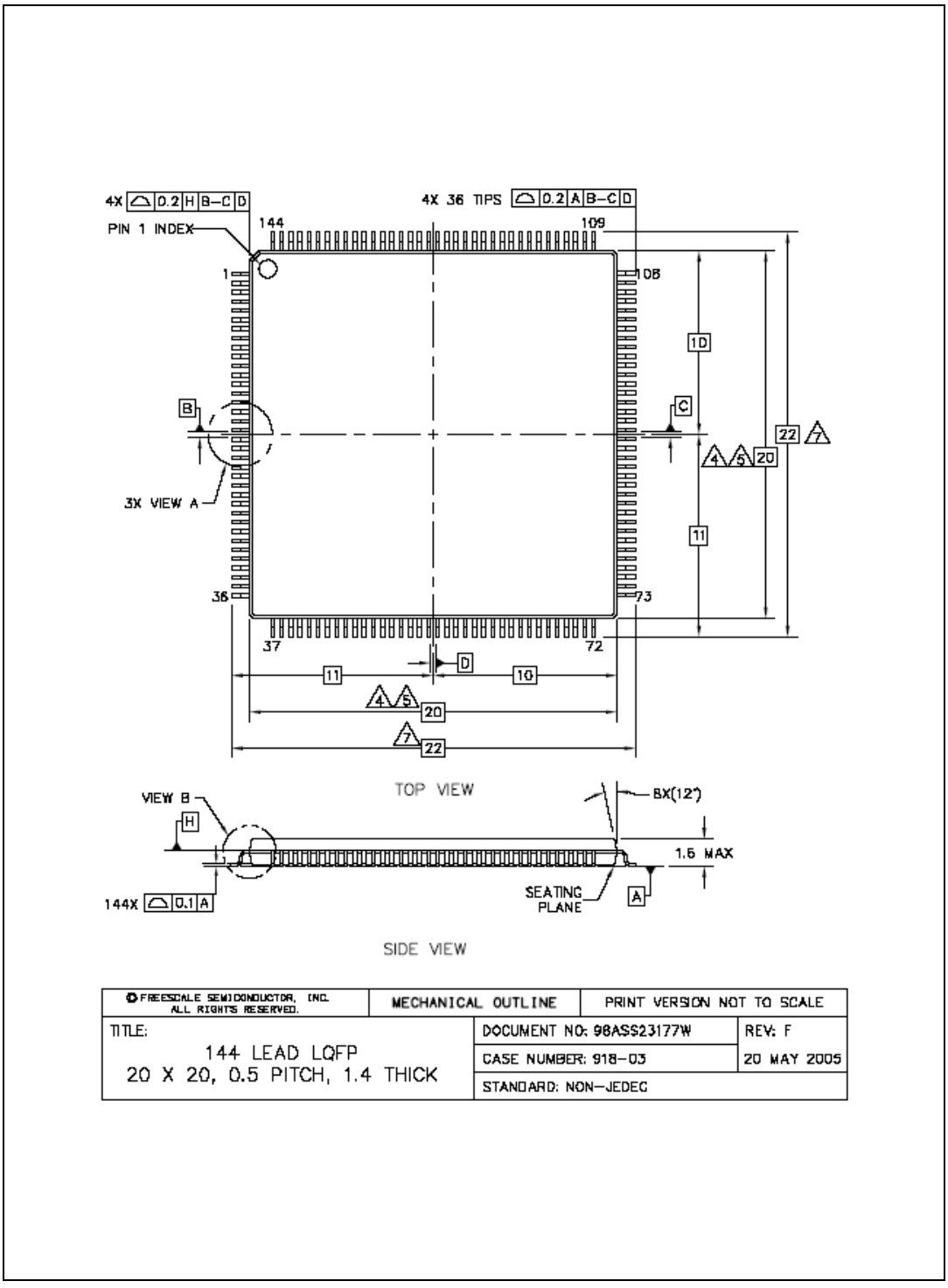


Figure 41. 144 LQFP package mechanical drawing (1 of 2)