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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I ² C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	123
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 36x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5604bav1q6r

- ⁶ CAN0, CAN1 are available. CAN2, CAN3, CAN4 and CAN5 are not available.
- ⁷ CAN0, CAN1 and CAN2 are available. CAN3, CAN4 and CAN5 are not available.
- ⁸ I/O count based on multiplexing with peripherals
- ⁹ All LQFP64 information is indicative and must be confirmed during silicon validation.
- ¹⁰ LBGA208 available only as development package for Nexus2+

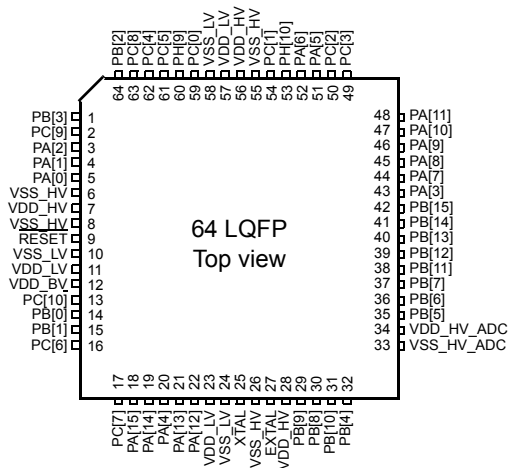


Figure 2. MPC560xB LQFP 64-pin configuration

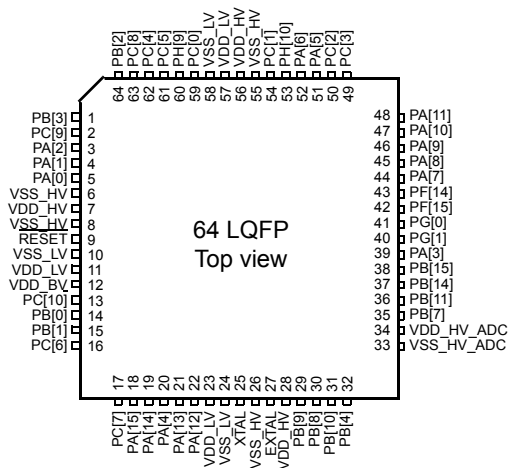


Figure 3. MPC560xC LQFP 64-pin configuration

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA ³
PE[1]	PCR[65]	AF0 AF1 AF2 AF3	GPIO[65] E0UC[17] CAN5TX ¹¹ —	SIUL eMIOS_0 FlexCAN_5 —	I/O I/O O —	M	Tristate	—	—	8	12	F4
PE[2]	PCR[66]	AF0 AF1 AF2 AF3 —	GPIO[66] E0UC[18] — — SIN_1	SIUL eMIOS_0 — — DSPI_1	I/O I/O — — I	M	Tristate	—	—	89	128	D7
PE[3]	PCR[67]	AF0 AF1 AF2 AF3	GPIO[67] E0UC[19] SOUT_1 —	SIUL eMIOS_0 DSPI_1 —	I/O I/O O —	M	Tristate	—	—	90	129	C7
PE[4]	PCR[68]	AF0 AF1 AF2 AF3 —	GPIO[68] E0UC[20] SCK_1 — EIRQ[9]	SIUL eMIOS_0 DSPI_1 — SIUL	I/O I/O I/O — I	M	Tristate	—	—	93	132	D6
PE[5]	PCR[69]	AF0 AF1 AF2 AF3	GPIO[69] E0UC[21] CS0_1 MA[2]	SIUL eMIOS_0 DSPI_1 ADC	I/O I/O I/O O	M	Tristate	—	—	94	133	C6
PE[6]	PCR[70]	AF0 AF1 AF2 AF3	GPIO[70] E0UC[22] CS3_0 MA[1]	SIUL eMIOS_0 DSPI_0 ADC	I/O I/O O O	M	Tristate	—	—	95	139	B5
PE[7]	PCR[71]	AF0 AF1 AF2 AF3	GPIO[71] E0UC[23] CS2_0 MA[0]	SIUL eMIOS_0 DSPI_0 ADC	I/O I/O O O	M	Tristate	—	—	96	140	C4
PE[8]	PCR[72]	AF0 AF1 AF2 AF3	GPIO[72] CAN2TX ¹² E0UC[22] CAN3TX ¹¹	SIUL FlexCAN_2 eMIOS_0 FlexCAN_3	I/O O I/O O	M	Tristate	—	—	9	13	G2
PE[9]	PCR[73]	AF0 AF1 AF2 AF3 — — —	GPIO[73] — E0UC[23] — WKPU[7] ⁴ CAN2RX ¹² CAN3RX ¹¹	SIUL — eMIOS_0 — WKPU FlexCAN_2 FlexCAN_3	I/O — I/O — I I I	S	Tristate	—	—	10	14	G1

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA ³
PF[2]	PCR[82]	AF0 AF1 AF2 AF3 —	GPIO[82] E0UC[12] CS0_2 — ANS[10]	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O I/O — I	J	Tristate	—	—	—	57	T10
PF[3]	PCR[83]	AF0 AF1 AF2 AF3 —	GPIO[83] E0UC[13] CS1_2 — ANS[11]	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O O — I	J	Tristate	—	—	—	58	R10
PF[4]	PCR[84]	AF0 AF1 AF2 AF3 —	GPIO[84] E0UC[14] CS2_2 — ANS[12]	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O O — I	J	Tristate	—	—	—	59	N11
PF[5]	PCR[85]	AF0 AF1 AF2 AF3 —	GPIO[85] E0UC[22] CS3_2 — ANS[13]	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O O — I	J	Tristate	—	—	—	60	P11
PF[6]	PCR[86]	AF0 AF1 AF2 AF3 —	GPIO[86] E0UC[23] — — ANS[14]	SIUL eMIOS_0 — — ADC	I/O I/O — — I	J	Tristate	—	—	—	61	T11
PF[7]	PCR[87]	AF0 AF1 AF2 AF3 —	GPIO[87] — — — ANS[15]	SIUL — — — ADC	I/O — — — I	J	Tristate	—	—	—	62	R11
PF[8]	PCR[88]	AF0 AF1 AF2 AF3	GPIO[88] CAN3TX ¹⁴ CS4_0 CAN2TX ¹⁵	SIUL FlexCAN_3 DSPI_0 FlexCAN_2	I/O O O O	M	Tristate	—	—	—	34	P1
PF[9]	PCR[89]	AF0 AF1 AF2 AF3 — —	GPIO[89] — CS5_0 — CAN2RX ¹⁵ CAN3RX ¹⁴	SIUL — DSPI_0 — FlexCAN_2 FlexCAN_3	I/O — O — I I	S	Tristate	—	—	—	33	N2

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA ³
PG[11]	PCR[107]	AF0 AF1 AF2 AF3	GPIO[107] E0UC[25] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	—	—	115	B12
PG[12]	PCR[108]	AF0 AF1 AF2 AF3	GPIO[108] E0UC[26] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	—	—	92	K14
PG[13]	PCR[109]	AF0 AF1 AF2 AF3	GPIO[109] E0UC[27] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	—	—	91	K16
PG[14]	PCR[110]	AF0 AF1 AF2 AF3	GPIO[110] E1UC[0] — —	SIUL eMIOS_1 — —	I/O I/O — —	S	Tristate	—	—	—	110	B14
PG[15]	PCR[111]	AF0 AF1 AF2 AF3	GPIO[111] E1UC[1] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	—	—	111	B13
PH[0]	PCR[112]	AF0 AF1 AF2 AF3 —	GPIO[112] E1UC[2] — — SIN1	SIUL eMIOS_1 — — DSPI_1	I/O I/O — — I	M	Tristate	—	—	—	93	F13
PH[1]	PCR[113]	AF0 AF1 AF2 AF3	GPIO[113] E1UC[3] SOUT1 —	SIUL eMIOS_1 DSPI_1 —	I/O I/O O —	M	Tristate	—	—	—	94	F14
PH[2]	PCR[114]	AF0 AF1 AF2 AF3	GPIO[114] E1UC[4] SCK_1 —	SIUL eMIOS_1 DSPI_1 —	I/O I/O I/O —	M	Tristate	—	—	—	95	F16
PH[3]	PCR[115]	AF0 AF1 AF2 AF3	GPIO[115] E1UC[5] CS0_1 —	SIUL eMIOS_1 DSPI_1 —	I/O I/O I/O —	M	Tristate	—	—	—	96	F15

- ⁷ Value of PCR.IBE bit must be 0
- ⁸ Be aware that this pad is used on the MPC5607B 100-pin and 144-pin to provide VDD_HV_ADC and VSS_HV_ADC1. Therefore, you should be careful in ensuring compatibility between MPC5604B/C and MPC5607B.
- ⁹ Out of reset all the functional pins except PC[0:1] and PH[9:10] are available to the user as GPIO. PC[0:1] are available as JTAG pins (TDI and TDO respectively). PH[9:10] are available as JTAG pins (TCK and TMS respectively). If the user configures these JTAG pins in GPIO mode the device is no longer compliant with IEEE 1149.1-2001.
- ¹⁰ The TDO pad has been moved into the STANDBY domain in order to allow low-power debug handshaking in STANDBY mode. However, no pull-resistor is active on the TDO pad while in STANDBY mode. At this time the pad is configured as an input. When no debugger is connected the TDO pad is floating causing additional current consumption. To avoid the extra consumption TDO must be connected. An external pull-up resistor in the range of 47–100 k Ω should be added between the TDO pin and VDD_HV. Only in case the TDO pin is used as application pin and a pull-up cannot be used then a pull-down resistor with the same value should be used between TDO pin and GND instead.
- ¹¹ Available only on MPC560xC versions, MPC5603B 64 LQFP, MPC5604B 64 LQFP and MPC5604B 208 MAPBGA devices
- ¹² Not available on MPC5602B devices
- ¹³ Not available in 100 LQFP package
- ¹⁴ Available only on MPC5604B 208 MAPBGA devices
- ¹⁵ Not available on MPC5603B 144-pin devices

3.7 Nexus 2+ pins

In the 208 MAPBGA package, eight additional debug pins are available (see [Table 7](#)).

Table 7. Nexus 2+ pin descriptions

Debug pin	Function	I/O direction	Pad type	Function after reset	Pin number		
					100 LQFP	144 LQFP	208 MAP BGA ¹
MCKO	Message clock out	O	F	—	—	—	T4
MDO0	Message data out 0	O	M	—	—	—	H15
MDO1	Message data out 1	O	M	—	—	—	H16
MDO2	Message data out 2	O	M	—	—	—	H14
MDO3	Message data out 3	O	M	—	—	—	H13
EVTI	Event in	I	M	Pull-up	—	—	K1
EVTO	Event out	O	M	—	—	—	L4
MSEO	Message start/end out	O	M	—	—	—	G16

¹ 208 MAPBGA available only as development package for Nexus2+

3.8 Electrical characteristics

3.9 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

3.13 Recommended operating conditions

Table 13. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}^1	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	3.0	3.6	V
$V_{SS_LV}^2$	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	$V_{SS}-0.1$	$V_{SS}+0.1$	V
$V_{DD_BV}^3$	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	3.0	3.6	V
			Relative to V_{DD}	$V_{DD}-0.1$	$V_{DD}+0.1$	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS})	—	$V_{SS}-0.1$	$V_{SS}+0.1$	V
$V_{DD_ADC}^4$	SR	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	3.0 ⁵	3.6	V
			Relative to V_{DD}	$V_{DD}-0.1$	$V_{DD}+0.1$	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	$V_{SS}-0.1$	—	V
			Relative to V_{DD}	—	$V_{DD}+0.1$	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	-5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	-50	50	
TV_{DD}	SR	V_{DD} slope to ensure correct power up ⁶	—	—	0.25	V/ μ s
T_A C-Grade Part	SR	Ambient temperature under bias	$f_{CPU} \leq 64$ MHz	-40	85	°C
T_J C-Grade Part	SR	Junction temperature under bias		-40	110	
T_A V-Grade Part	SR	Ambient temperature under bias		-40	105	
T_J V-Grade Part	SR	Junction temperature under bias		-40	130	
T_A M-Grade Part	SR	Ambient temperature under bias		-40	125	
T_J M-Grade Part	SR	Junction temperature under bias		-40	150	

¹ 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair

² 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.

³ 400 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics).

⁴ 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.

⁵ Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below V_{LVDHVL} , device is reset.

⁶ Guaranteed by device validation

Table 14. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V _{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V _{DD} ¹	SR	Voltage on VDD_HV pins with respect to ground (V _{SS})	—	4.5	5.5	V
			Voltage drop ²	3.0	5.5	
V _{SS_LV} ³	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V _{SS})	—	V _{SS} –0.1	V _{SS} +0.1	V
V _{DD_BV} ⁴	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V _{SS})	—	4.5	5.5	V
			Voltage drop ²	3.0	5.5	
			Relative to V _{DD}	V _{DD} –0.1	V _{DD} +0.1	
V _{SS_ADC}	SR	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V _{SS})	—	V _{SS} –0.1	V _{SS} +0.1	V
V _{DD_ADC} ⁵	SR	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V _{SS})	—	4.5	5.5	V
			Voltage drop ²	3.0	5.5	
			Relative to V _{DD}	V _{DD} –0.1	V _{DD} +0.1	
V _{IN}	SR	Voltage on any GPIO pin with respect to ground (V _{SS})	—	V _{SS} –0.1	—	V
			Relative to V _{DD}	—	V _{DD} +0.1	
I _{INJPAD}	SR	Injected input current on any pin during overload condition	—	–5	5	mA
I _{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
TV _{DD}	SR	V _{DD} slope to ensure correct power up ⁶	—	—	0.25	V/μs
T _A C-Grade Part	SR	Ambient temperature under bias	f _{CPU} ≤ 64 MHz	–40	85	°C
T _J C-Grade Part	SR	Junction temperature under bias		–40	110	
T _A V-Grade Part	SR	Ambient temperature under bias		–40	105	
T _J V-Grade Part	SR	Junction temperature under bias		–40	130	
T _A M-Grade Part	SR	Ambient temperature under bias		–40	125	
T _J M-Grade Part	SR	Junction temperature under bias		–40	150	

¹ 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.

² Full device operation is guaranteed by design when the voltage drops below 4.5 V down to 3.0 V. However, certain analog electrical characteristics will not be guaranteed to stay within the stated limits.

³ 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.

⁴ 100 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics).

⁵ 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.

⁶ Guaranteed by device validation

NOTE

RAM data retention is guaranteed with V_{DD_LV} not below 1.08 V.

3.15.2 I/O input DC characteristics

Table 16 provides input DC electrical characteristics as described in Figure 7.

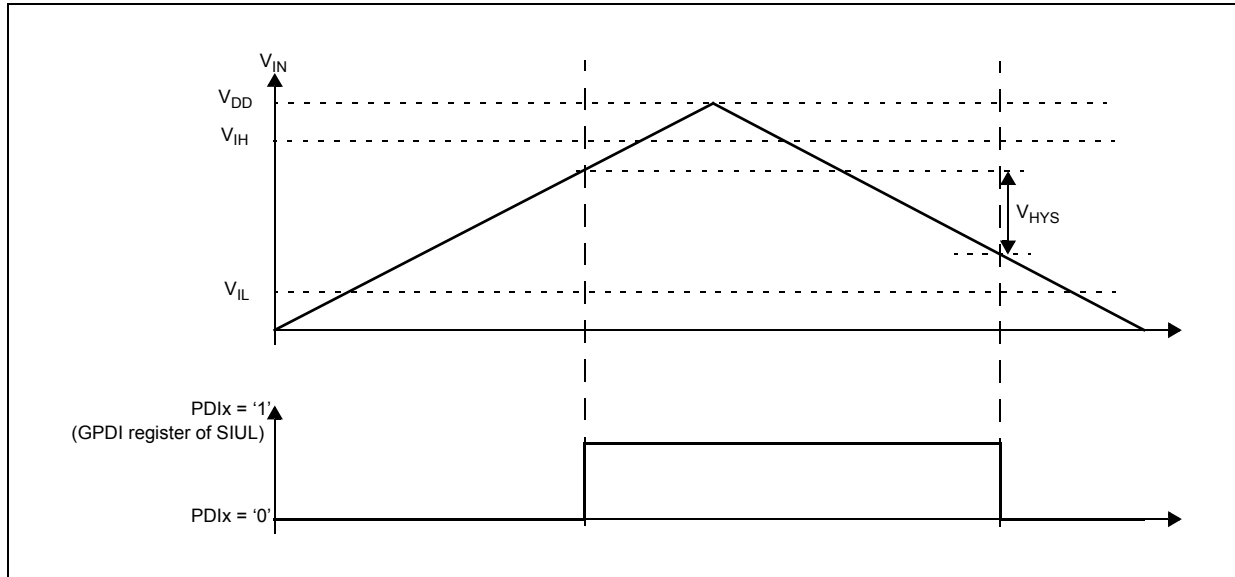


Figure 7. I/O input DC electrical characteristics definition

Table 16. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions ¹		Value			Unit
						Min	Typ	Max	
V _{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	—		0.65V _{DD}	—	V _{DD} +0.4	V
V _{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	—		−0.4	—	0.35V _{DD}	
V _{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—		0.1V _{DD}	—	—	
I _{LKG}	CC	D	Digital input leakage	No injection on adjacent pin	T _A = −40 °C	—	2	200	nA
		T _A = 25 °C			—	2	200		
		T _A = 85 °C			—	5	300		
		T _A = 105 °C			—	12	500		
		T _A = 125 °C			—	70	1000		
W _{FI} ²	SR	P	Wakeup input filtered pulse	—		—	—	40	ns
W _{NFI} ²	SR	P	Wakeup input not filtered pulse	—		1000	—	—	ns

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = −40 to 125 °C, unless otherwise specified

² In the range from 40 to 1000 ns, pulses can be filtered or not filtered, according to operating temperature and voltage.

Table 20. FAST configuration output buffer electrical characteristics (continued)

Symbol	C	Parameter	Conditions ¹	Value			Unit
				Min	Typ	Max	
V _{OL}	CC	P Output low level FAST configuration	Push Pull I _{OL} = 14mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	0.1V _{DD}	V
			I _{OL} = 7mA, V _{DD} = 5.0 V ± 10%, PAD3V5V = 1 ²	—	—	0.1V _{DD}	
			I _{OL} = 11mA, V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

² The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.15.4 Output pin transition times

Table 21. Output pin transition times

Symbol	C	Parameter	Conditions ¹	Value			Unit
				Min	Typ	Max	
t _{tr}	CC	D Output transition time output pin ² SLOW configuration	C _L = 25 pF V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
			C _L = 50 pF	—	—	100	
			C _L = 100 pF	—	—	125	
		D Output transition time output pin ² MEDIUM configuration	C _L = 25 pF V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
			C _L = 50 pF	—	—	100	
			C _L = 100 pF	—	—	125	
			C _L = 100 pF	—	—	125	
t _{tr}	CC	D Output transition time output pin ² MEDIUM configuration	C _L = 25 pF V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
			C _L = 50 pF	—	—	20	
			C _L = 100 pF	—	—	40	
		D Output transition time output pin ² FAST configuration	C _L = 25 pF V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
			C _L = 50 pF	—	—	25	
			C _L = 100 pF	—	—	40	
			C _L = 100 pF	—	—	40	
t _{tr}	CC	D Output transition time output pin ² FAST configuration	C _L = 25 pF V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	4	ns
			C _L = 50 pF	—	—	6	
			C _L = 100 pF	—	—	12	
		D Output transition time output pin ² FAST configuration	C _L = 25 pF V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	4	
			C _L = 50 pF	—	—	7	
			C _L = 100 pF	—	—	12	
			C _L = 100 pF	—	—	12	

¹ V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

Table 24. I/O weight¹ (continued)

Supply segment			Pad	144/100 LQFP				64 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
144 LQFP	100 LQFP	64 LQFP ²		SRC ³ = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
2	2	2	PB[9]	1%	—	1%	—	1%	—	1%	—
			PB[8]	1%	—	1%	—	1%	—	1%	—
			PB[10]	6%	—	7%	—	6%	—	7%	—
		—	PF[0]	6%	—	7%	—	—	—	—	—
		—	PF[1]	7%	—	8%	—	—	—	—	—
		—	PF[2]	7%	—	8%	—	—	—	—	—
		—	PF[3]	7%	—	9%	—	—	—	—	—
		—	PF[4]	8%	—	9%	—	—	—	—	—
		—	PF[5]	8%	—	10%	—	—	—	—	—
		—	PF[6]	8%	—	10%	—	—	—	—	—
		—	PF[7]	9%	—	10%	—	—	—	—	—
	2	—	PD[0]	1%	—	1%	—	—	—	—	—
		—	PD[1]	1%	—	1%	—	—	—	—	—
		—	PD[2]	1%	—	1%	—	—	—	—	—
		—	PD[3]	1%	—	1%	—	—	—	—	—
		—	PD[4]	1%	—	1%	—	—	—	—	—
		—	PD[5]	1%	—	1%	—	—	—	—	—
		—	PD[6]	1%	—	1%	—	—	—	—	—
		—	PD[7]	1%	—	1%	—	—	—	—	—
		—	PD[8]	1%	—	1%	—	—	—	—	—
		2	PB[4]	1%	—	1%	—	1%	—	1%	—
			PB[5]	1%	—	1%	—	1%	—	2%	—
			PB[6]	1%	—	1%	—	1%	—	2%	—
			PB[7]	1%	—	1%	—	1%	—	2%	—
		—	PD[9]	1%	—	1%	—	—	—	—	—
		—	PD[10]	1%	—	1%	—	—	—	—	—
		—	PD[11]	1%	—	1%	—	—	—	—	—
		2	PB[11]	11%	—	13%	—	17%	—	21%	—
		—	PD[12]	11%	—	13%	—	—	—	—	—
		2	PB[12]	11%	—	13%	—	18%	—	21%	—
		—	PD[13]	10%	—	12%	—	—	—	—	—

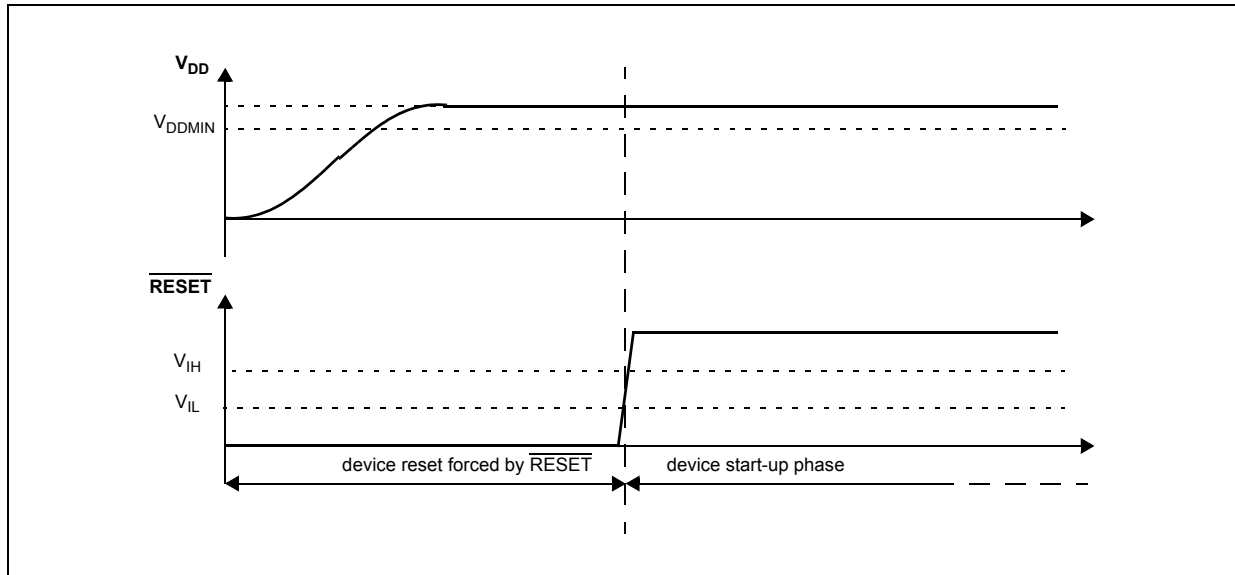


Figure 8. Start-up reset requirements

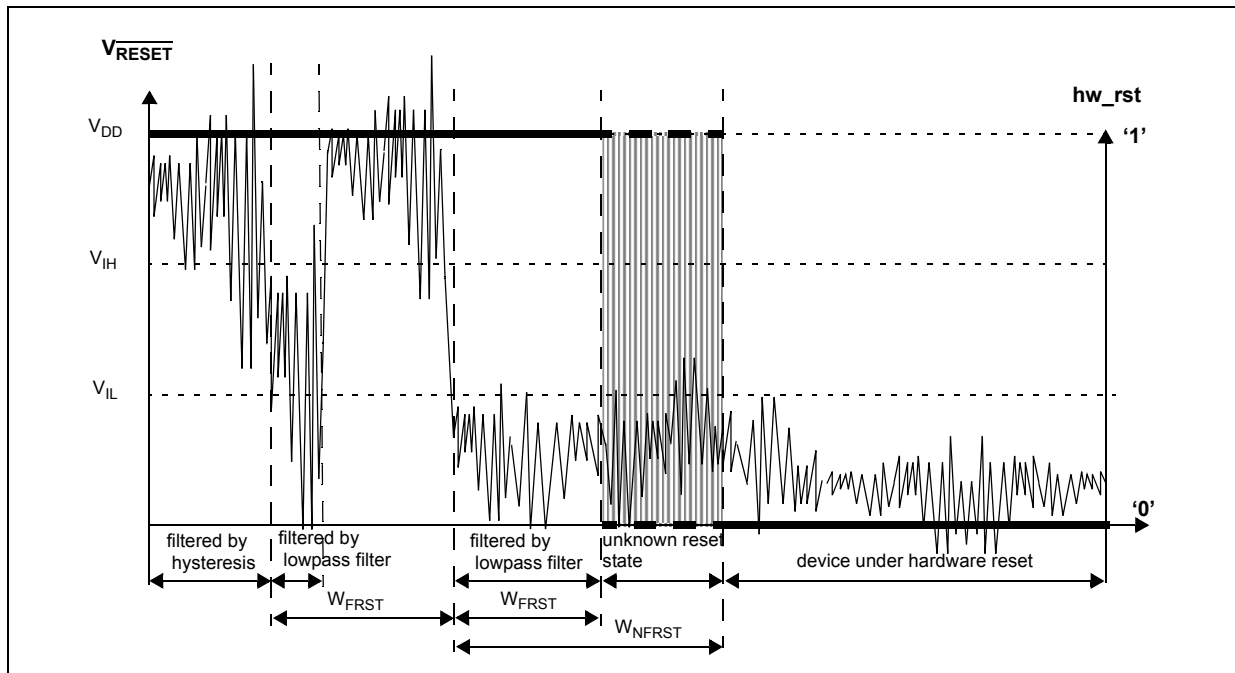


Figure 9. Noise filtering on reset signal

Table 25. Reset electrical characteristics

Symbol	C	Parameter	Conditions ¹	Value			Unit
				Min	Typ	Max	
V_{IH}	SR	P	Input High Level CMOS (Schmitt Trigger)	$0.65V_{DD}$	—	$V_{DD}+0.4$	V

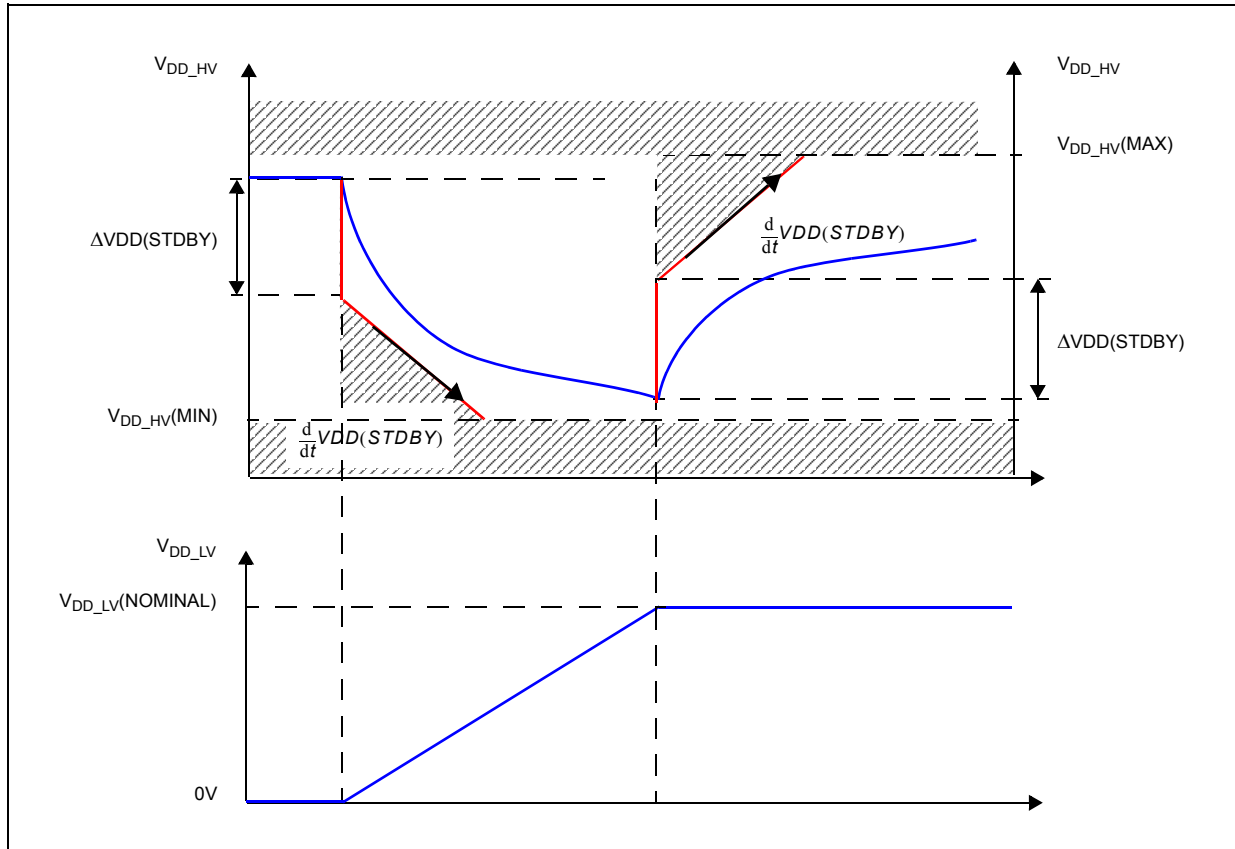
Figure 12. V_{DD_HV} and V_{DD_BV} supply constraints during STANDBY mode exit

Table 26. Voltage regulator electrical characteristics

Symbol	C	Parameter	Conditions ¹	Value			Unit
				Min	Typ	Max	
C_{REGn}	SR	Internal voltage regulator external capacitance	—	200	—	500	nF
R_{REG}	SR	Stability capacitor equivalent serial resistance	Range: 10 kHz to 20 MHz	—	—	0.2	Ω
C_{DEC1}	SR	Decoupling capacitance ² ballast	V_{DD_BV}/V_{SS_LV} pair: $V_{DD_BV} = 4.5\text{ V to }5.5\text{ V}$	100 ³	470 ⁴	—	nF
			V_{DD_BV}/V_{SS_LV} pair: $V_{DD_BV} = 3\text{ V to }3.6\text{ V}$	400		—	
C_{DEC2}	SR	Decoupling capacitance regulator supply	V_{DD}/V_{SS} pair	10	100	—	nF
$\left \frac{dV_{DD}}{dt} \right $	SR	Maximum slope on V_{DD}		—	—	250	mV/ μ s
$ \Delta V_{DD}(STDBY) $	SR	Maximum instant variation on V_{DD} during standby exit		—	—	30	mV

Example 1. No regulator (worst case)

The $|\Delta V_{DD}(STDBY)|$ parameter can be seen as the V_{DD} voltage drop through the ESR resistance of the regulator stability capacitor when the I_{DD_BV} current required to load V_{DD_LV} domain during the standby exit. It is thus possible to define the maximum equivalent resistance $ESR_{STDBY}(MAX)$ of the total capacitance on the V_{DD} supply:

$$ESR_{STDBY}(MAX) = |\Delta V_{DD}(STDBY)| / I_{DD_BV} = (30 \text{ mV}) / (300 \text{ mA}) = 0.1 \Omega^1$$

The $dV_{DD}(STDBY)/dt$ parameter can be seen as the V_{DD} voltage drop at the capacitance pin (excluding ESR drop) while providing the I_{DD_BV} supply required to load V_{DD_LV} domain during the standby exit. It is thus possible to define the minimum equivalent capacitance $C_{STDBY}(MIN)$ of the total capacitance on the V_{DD} supply:

$$C_{STDBY}(MIN) = I_{DD_BV} / dV_{DD}(STDBY)/dt = (300 \text{ mA}) / (15 \text{ mV}/\mu\text{s}) = 20 \mu\text{F}$$

This configuration is a worst case, with the assumption no regulator is available.

Example 2. Simplified regulator

The regulator should be able to provide significant amount of the current during the standby exit process. For example, in case of an ideal voltage regulator providing 200 mA current, it is possible to recalculate the equivalent $ESR_{STDBY}(MAX)$ and $C_{STDBY}(MIN)$ as follows:

$$ESR_{STDBY}(MAX) = |\Delta V_{DD}(STDBY)| / (I_{DD_BV} - 200 \text{ mA}) = (30 \text{ mV}) / (100 \text{ mA}) = 0.3 \Omega$$

$$C_{STDBY}(MIN) = (I_{DD_BV} - 200 \text{ mA}) / dV_{DD}(STDBY)/dt = (300 \text{ mA} - 200 \text{ mA}) / (15 \text{ mV}/\mu\text{s}) = 6.7 \mu\text{F}$$

In case optimization is required, $C_{STDBY}(MIN)$ and $ESR_{STDBY}(MAX)$ should be calculated based on the regulator characteristics as well as the board V_{DD} plane characteristics.

3.17.2 Low voltage detector electrical characteristics

The device implements a Power-on Reset (POR) module to ensure correct power-up initialization, as well as four low voltage detectors (LVDs) to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state (refer to RGM Destructive Event Status (RGM_DES) Register flag F_POR in device reference manual)
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD27 in device reference manual)
- LVDHV5 monitors V_{DD} when application uses device in the $5.0 \text{ V} \pm 10\%$ range (refer to RGM Functional Event Status (RGM_FES) Register flag F_LVD45 in device reference manual)
- LVDLVCOR monitors power domain No. 1 (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD12_PD1 in device reference manual)
- LVDLVBKP monitors power domain No. 0 (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD12_PD0 in device reference manual)

NOTE

When enabled, power domain No. 2 is monitored through LVDLVBKP.

1. Based on typical time for standby exit sequence of 20 μs , $ESR(MIN)$ can actually be considered at $\sim 50 \text{ kHz}$.

Table 30. Flash module life

Symbol	C	Parameter	Conditions	Value			Unit
				Min	Typ	Max	
P/E	CC	C	Number of program/erase cycles per block over the operating temperature range (T_J)	16 KB blocks	100,000	—	cycles
				32 KB blocks	10,000	100,000	
				128 KB blocks	1,000	100,000	
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature ¹	Blocks with 0–1,000 P/E cycles	20	—	years
				Blocks with 1,001–10,000 P/E cycles	10	—	
				Blocks with 10,001–100,000 P/E cycles	5	—	

¹ Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 31. Flash read access timing

Symbol	C	Parameter	Conditions ¹	Max	Unit
f_{READ}	CC	P	Maximum frequency for Flash reading	2 wait states	MHz
				1 wait state	
				0 wait states	

¹ $V_{DD} = 3.3 \text{ V} \pm 10\% / 5.0 \text{ V} \pm 10\%$, $T_A = -40$ to 125 °C, unless otherwise specified

3.19.2 Flash power supply DC characteristics

Table 32 shows the power supply DC characteristics on external supply.

Table 32. Flash memory power supply DC electrical characteristics

Symbol	C	Parameter	Conditions ¹	Value			Unit	
				Min	Typ	Max		
I _{FREAD} ²	CC	D	Sum of the current consumption on VDD_HV and VDD_BV on read access	Code flash memory module read f _{CPU} = 64 MHz ³	—	15	33	mA
			Data flash memory module read f _{CPU} = 64 MHz ³	—	15	33		
I _{FMOD} ²	CC	D	Sum of the current consumption on VDD_HV and VDD_BV on matrix modification (program/erase)	Program/Erase ongoing while reading code flash memory registers f _{CPU} = 64 MHz ³	—	15	33	mA
			Program/Erase ongoing while reading data flash memory registers f _{CPU} = 64 MHz ³	—	15	33		

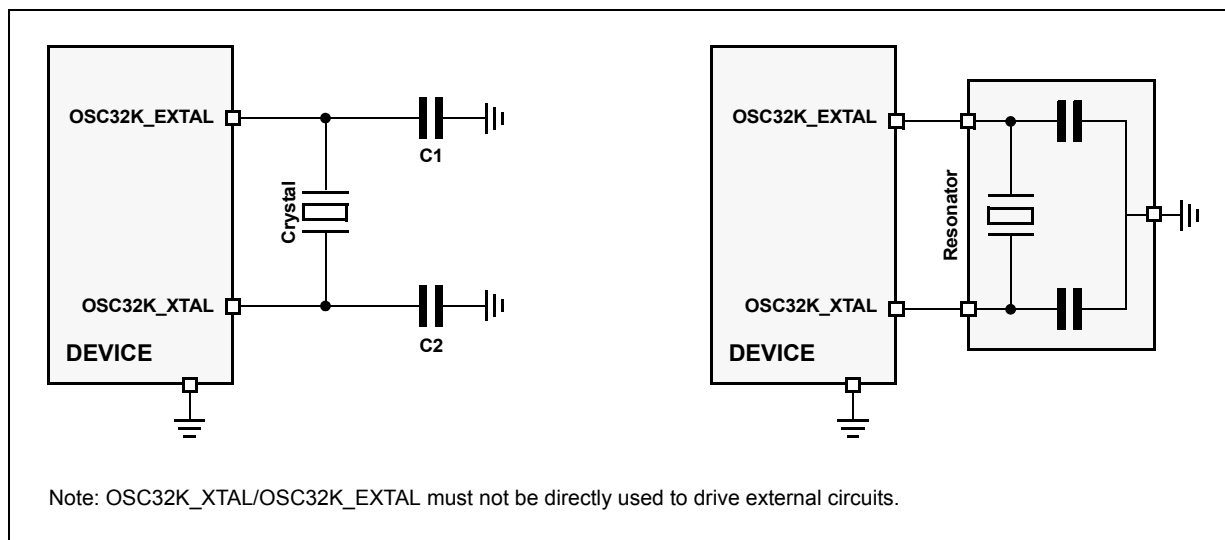


Figure 16. Crystal oscillator and resonator connection scheme

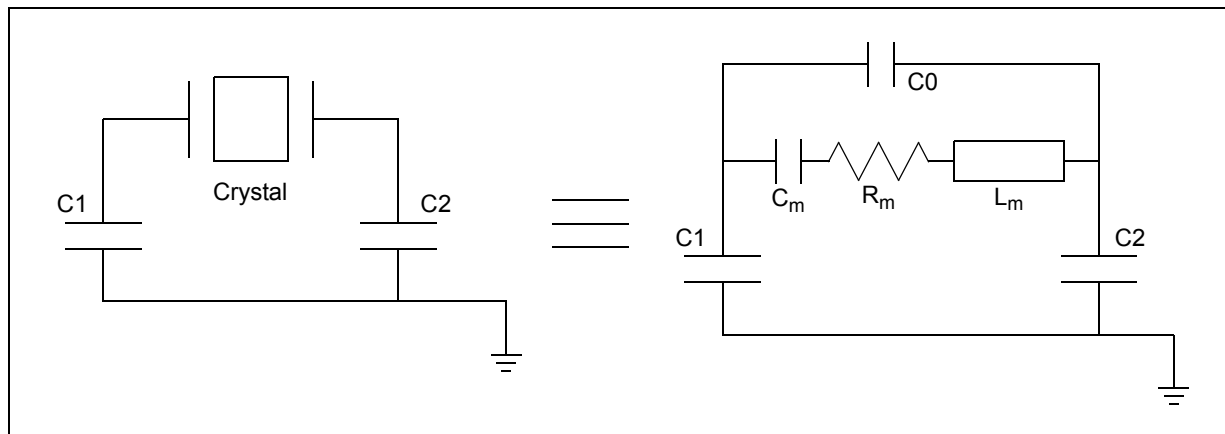


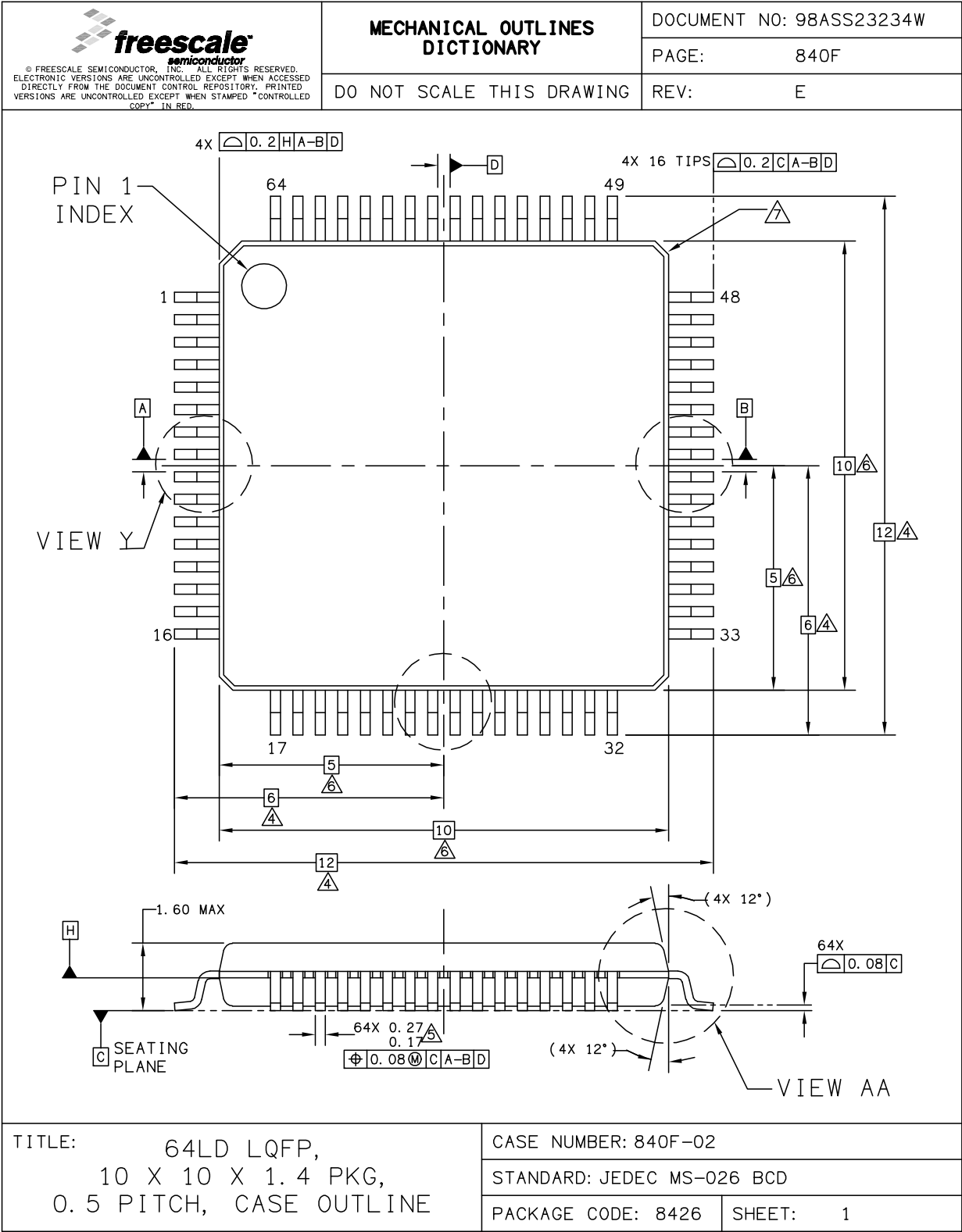
Figure 17. Equivalent circuit of a quartz crystal

Table 39. Crystal motional characteristics¹

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
L_m	Motional inductance	—	—	11.796	—	KH
C_m	Motional capacitance	—	—	2	—	fF
C1/C2	Load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground ²	—	18	—	28	pF
R_m ³	Motional resistance	AC coupled @ $C_0 = 2.85 \text{ pF}^4$	—	—	65	$k\Omega$
		AC coupled @ $C_0 = 4.9 \text{ pF}^4$	—	—	50	
		AC coupled @ $C_0 = 7.0 \text{ pF}^4$	—	—	35	
		AC coupled @ $C_0 = 9.0 \text{ pF}^4$	—	—	30	

¹ Crystal used: Epson Toyocom MC306

4.1.1 64 LQFP



4.1.4 208 MAPBGA

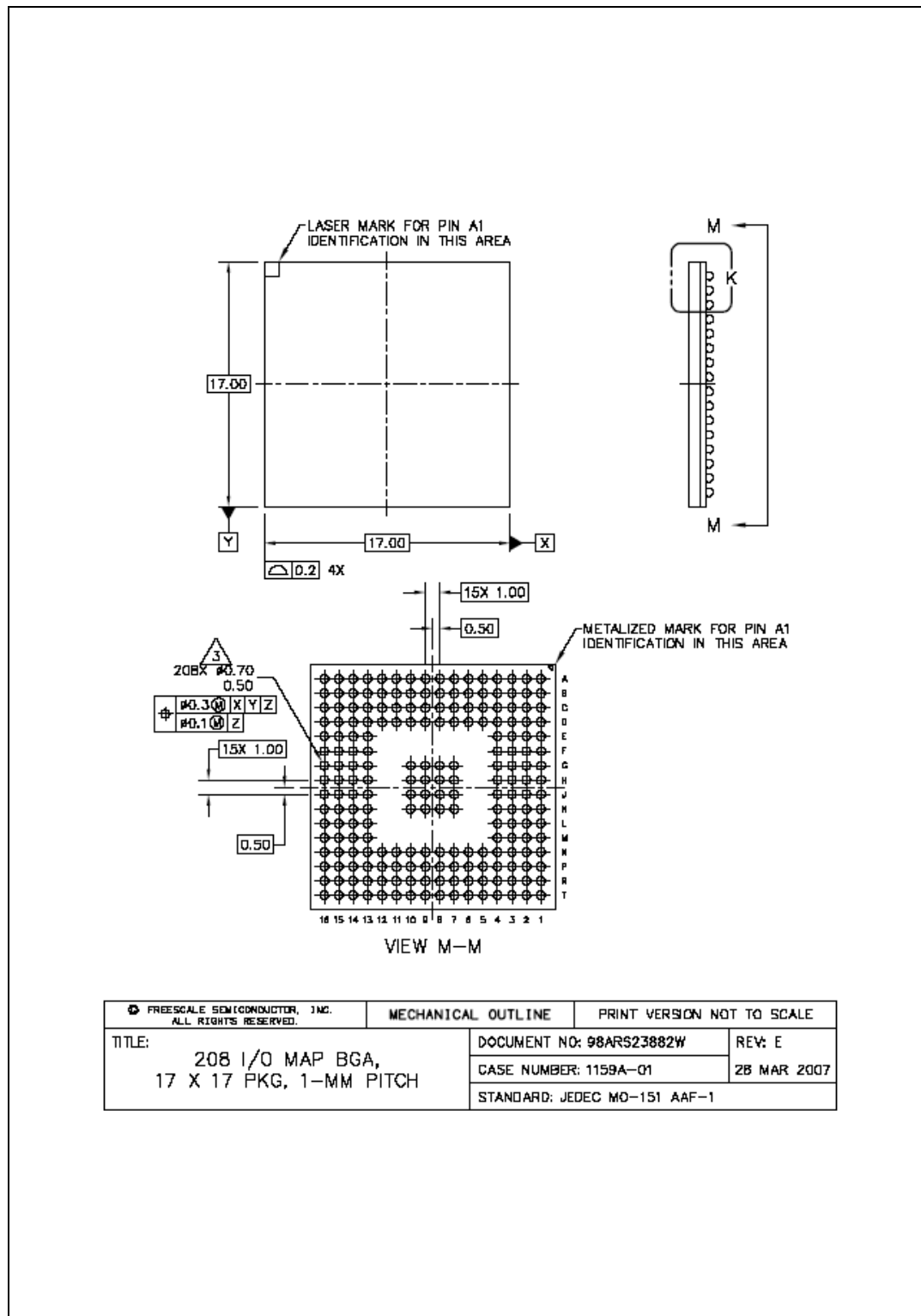
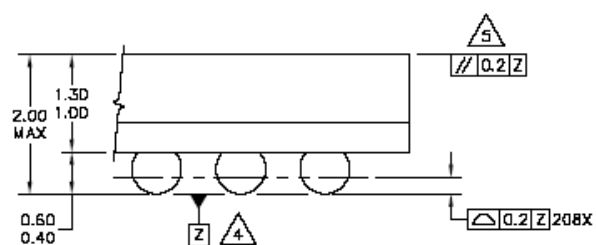


Figure 43. 208 MAPBGA package mechanical drawing (1 of 2)



DETAIL K
(ROTATED 90° CLOCKWISE)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. PACKAGE CODE SUMMARY:
MAP BGA: 5253
MAP BGA PGE DIE: 5371

 FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1-MM PITCH	DOCUMENT NO: 9BARS238B2W	REV: E
	CASE NUMBER: 1159A-01	28 MAR 2007
	STANDARD: JEDEC MO-151 AAF-1	

Figure 44. 208 MAPBGA package mechanical drawing (2 of 2)

Appendix A Abbreviations

Table A-1 lists abbreviations used but not defined elsewhere in this document.

Table A-1. Abbreviations

Abbreviation	Meaning
CMOS	Complementary metal–oxide–semiconductor
CPHA	Clock phase
CPOL	Clock polarity
CS	Peripheral chip select
EVTO	Event out
MCKO	Message clock out
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
SCK	Serial communications clock
SOUT	Serial data out
TBD	To be defined
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select