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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	45
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5604bk0mlh6r

[6] CAN0, CAN1 are available. CAN2, CAN3, CAN4 and CAN5 are not available.
[7] CAN0, CAN1 and CAN2 are available. CAN3, CAN4 and CAN5 are not available.
[8] I/O count based on multiplexing with peripherals
[9] All LQFP64information is indicative and must be confirmed during silicon validation.
[10] LBGA208 available only as development package for Nexus2+

3.3 Voltage supply pins

Voltage supply pins are used to provide power to the device. Three dedicated VDD_LV/VSS_LV supply pairs are used for 1.2 V regulator stabilization.

Table 4. Voltage supply pin descriptions

Port pin	Function	Pin number			
		64 LQFP[1]	100 LQFP	144 LQFP	208 MAPBGA[2]
VDD_HV	Digital supply voltage	7, 28, 56	15, 37, 70, 84	19, 51, 100, 123	C2, D9, E16, G13, H3, N9, R5
VSS_HV	Digital ground	6, 8, 26, 55	14, 16, 35, 69, 83	18, 20, 49, 99, 122	G7, G8, G9, G10, H1, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10
VDD_LV	1.2V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest V_{SS_LV} pin.[3]	11, 23, 57	19, 32, 85	23, 46, 124	D8, K4, P7
VSS_LV	1.2V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest V_{DD_LV} pin.[3]	10, 24, 58	18, 33, 86	22, 47, 125	C8, J2, N7
VDD_BV	Internal regulator supply voltage	12	20	24	K3
VSS_HV_ADC	Reference ground and analog ground for the ADC	33	51	73	R15
VDD_HV_ADC	Reference voltage and analog supply for the ADC	34	52	74	P14

1 Pin numbers apply to both the MPC560xB and MPC560xC packages.

2 208 MAPBGA available only as development package for Nexus2+

3 A decoupling capacitor must be placed between each of the three VDD_LV/VSS_LV supply pairs to ensure stable voltage (see the recommended operating conditions in the device datasheet for details).

3.4 Pad types

In the device the following types of pads are available for system pins and functional port pins:

S = Slow[1]

M = Medium[1 2]

F = Fast[1 2]

I = Input only with analog feature[1]

J = Input/Output ('S' pad) with analog feature

X = Oscillator

1. See the I/O pad electrical characteristics in the device datasheet for details.
2. All medium and fast pads are in slow configuration by default at reset and can be configured as fast or medium (see PCR.SRC in section Pad Configuration Registers (PCR0–PCR122) in the device reference manual).

[7] Value of PCR.IBE bit must be 0

[8] Be aware that this pad is used on the MPC5607B 100-pin and 144-pin to provide VDD_HV_ADC and VSS_HV_ADC1. Therefore, you should be careful in ensuring compatibility between MPC5604B/C and MPC5607B.

[9] Out of reset all the functional pins except PC[0:1] and PH[9:10] are available to the user as GPIO.
PC[0:1] are available as JTAG pins (TDI and TDO respectively).
PH[9:10] are available as JTAG pins (TCK and TMS respectively).
If the user configures these JTAG pins in GPIO mode the device is no longer compliant with IEEE 1149.1-2001.

[10] The TDO pad has been moved into the STANDBY domain in order to allow low-power debug handshaking in STANDBY mode. However, no pull-resistor is active on the TDO pad while in STANDBY mode. At this time the pad is configured as an input. When no debugger is connected the TDO pad is floating causing additional current consumption. To avoid the extra consumption TDO must be connected. An external pull-up resistor in the range of 47–100 kΩ should be added between the TDO pin and VDD_HV. Only in case the TDO pin is used as application pin and a pull-up cannot be used then a pull-down resistor with the same value should be used between TDO pin and GND instead.

[11] Available only on MPC560xC versions, MPC5603B 64 LQFP, MPC5604B 64 LQFP and MPC5604B 208 MAPBGA devices

[12] Not available on MPC5602B devices

[13] Not available in 100 LQFP package

[14] Available only on MPC5604B 208 MAPBGA devices

[15] Not available on MPC5603B 144-pin devices

3.7 Nexus 2+ pins

In the 208 MAPBGA package, eight additional debug pins are available (see Table 7).

Table 7. Nexus 2+ pin descriptions

Debug pin	Function	I/O direction	Pad type	Function after reset	Pin number		
					100 LQFP	144 LQFP	208 MAP BGA[1]
MCKO	Message clock out	O	F	—	—	—	T4
MDO0	Message data out 0	O	M	—	—	—	H15
MDO1	Message data out 1	O	M	—	—	—	H16
MDO2	Message data out 2	O	M	—	—	—	H14
MDO3	Message data out 3	O	M	—	—	—	H13
EVTI	Event in	I	M	Pull-up	—	—	K1
EVTO	Event out	O	M	—	—	—	L4
MSEO	Message start/end out	O	M	—	—	—	G16

[1] 208 MAPBGA available only as development package for Nexus2+

3.8 Electrical characteristics

3.9 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid applying any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol "CC" for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol "SR" for System Requirement is included in the Symbol column.

3.10 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in Table 8 are used and the parameters are tagged accordingly in the tables where appropriate.

Table 8. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled "C" in the parameter tables where appropriate.

3.11 NVUSRO register

Bit values in the Non-Volatile User Options (NVUSRO) Register control portions of the device configuration, namely electrical parameters such as high voltage supply and oscillator margin, as well as digital functionality (watchdog enable/disable after reset).

For a detailed description of the NVUSRO register, please refer to the device reference manual.

3.11.1 NVUSRO[PAD3V5V] field description

The DC electrical characteristics are dependent on the PAD3V5V bit value. Table 9 shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 9. PAD3V5V field description

Value[1]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

[1] Default manufacturing value is ‘1’. Value can be programmed by customer in Shadow Flash.

3.11.2 NVUSRO[OSCILLATOR_MARGIN] field description

The fast external crystal oscillator consumption is dependent on the OSCILLATOR_MARGIN bit value. Table 10 shows how NVUSRO[OSCILLATOR_MARGIN] controls the device configuration.

Table 10. OSCILLATOR_MARGIN field description

Value[1]	Description
0	Low consumption configuration (4 MHz/8 MHz)
1	High margin configuration (4 MHz/16 MHz)

[1] Default manufacturing value is ‘1’. Value can be programmed by customer in Shadow Flash.

3.11.3 NVUSRO[WATCHDOG_EN] field description

The watchdog enable/disable configuration after reset is dependent on the WATCHDOG_EN bit value. Table 11 shows how NVUSRO[WATCHDOG_EN] controls the device configuration.

Table 11. WATCHDOG_EN field description

Value[1]	Description
0	Disable after reset
1	Enable after reset

[1] Default manufacturing value is ‘1’. Value can be programmed by customer in Shadow Flash.

[2] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C

[3] Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

[4] Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

[5] Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

3.14.2 Power considerations

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using Equation 1:

$$T_J = T_A + (P_D \times R_{\theta JA}) \quad \textit{Eqn. 1}$$

Where:

T_A is the ambient temperature in °C.

$R_{\theta JA}$ is the package junction-to-ambient thermal resistance, in °C/W.

P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$).

P_{INT} is the product of I_{DD} and V_{DD}, expressed in watts. This is the chip internal power.

$P_{I/O}$ represents the power dissipation on input and output pins; user determined.

Most of the time for the applications, $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant, if the device is configured to continuously drive external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273\ °C) \quad \textit{Eqn. 2}$$

Therefore, solving equations 1 and 2:

$$K = P_D \times (T_A + 273\ °C) + R_{\theta JA} \times P_D^2 \quad \textit{Eqn. 3}$$

Where:

K is a constant for the particular part, which may be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations 1 and 2 iteratively for any value of T_A.

3.15 I/O pad electrical characteristics

3.15.1 I/O pad types

The device provides four main I/O pad types depending on the associated alternate functions:

- Slow pads—These pads are the most common pads, providing a good compromise between transition time and low electromagnetic emission.
- Medium pads—These pads provide transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
- Fast pads—These pads provide maximum speed. There are used for improved Nexus debugging capability.
- Input only pads—These pads are associated to ADC channels and the external 32 kHz crystal oscillator (SXOSC) providing low input leakage.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance.

3.15.2 I/O input DC characteristics

Table 16 provides input DC electrical characteristics as described in Figure 7.

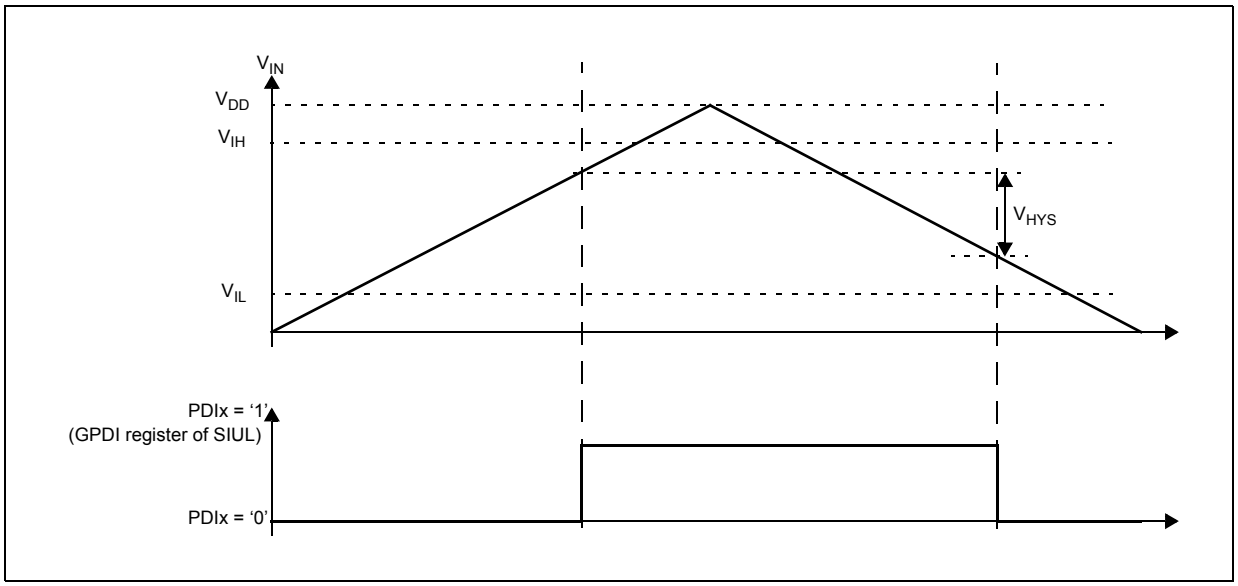

Figure 7. I/O input DC electrical characteristics definition

Table 16. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	—		$0.65V_{DD}$	—	$V_{DD}+0.4$	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	—		–0.4	—	$0.35V_{DD}$	
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—		$0.1V_{DD}$	—	—	
I_{LKG}	CC	D	Digital input leakage	No injection on adjacent pin	T_A = –40 °C	—	2	200	nA
		D			T_A = 25 °C	—	2	200	
		D			T_A = 85 °C	—	5	300	
		D			T_A = 105 °C	—	12	500	
		P			T_A = 125 °C	—	70	1000	
W_{FI}[2]	SR	P	Wakeup input filtered pulse	—		—	—	40	ns
W_{NFI}[2]	SR	P	Wakeup input not filtered pulse	—		1000	—	—	ns

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 In the range from 40 to 1000 ns, pulses can be filtered or not filtered, according to operating temperature and voltage.

[2] C_L includes device and package capacitances (C_{PKG} < 5 pF).

3.15.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in Table 22.

Table 22. I/O supply segment

Package	Supply segment					
	1	2	3	4	5	6
208 MAPBGA[1]	Equivalent to 144 LQFP segment pad distribution				MCKO	MDOn/MSEO
144 LQFP	pin20–pin49	pin51–pin99	pin100–pin122	pin 123–pin19	—	—
100 LQFP	pin16–pin35	pin37–pin69	pin70–pin83	pin 84–pin15	—	—
64 LQFP	pin8–pin26	pin28–pin55	pin56–pin7	—	—	—

[1] 208 MAPBGA available only as development package for Nexus2+

Table 23 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

Table 23. I/O consumption

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{SWTSLW}[2]	CC	D	Dynamic I/O current for SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16	
I_{SWTMED}[2]	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	29	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	17	
I_{SWTFST}[2]	CC	D	Dynamic I/O current for FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	110	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
I_{RMSSLW}	CC	D	Root mean square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.3	mA
				C_L = 25 pF, 4 MHz		—	—	3.2	
				C_L = 100 pF, 2 MHz		—	—	6.6	
				C_L = 25 pF, 2 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.6	
				C_L = 25 pF, 4 MHz		—	—	2.3	
				C_L = 100 pF, 2 MHz		—	—	4.7	

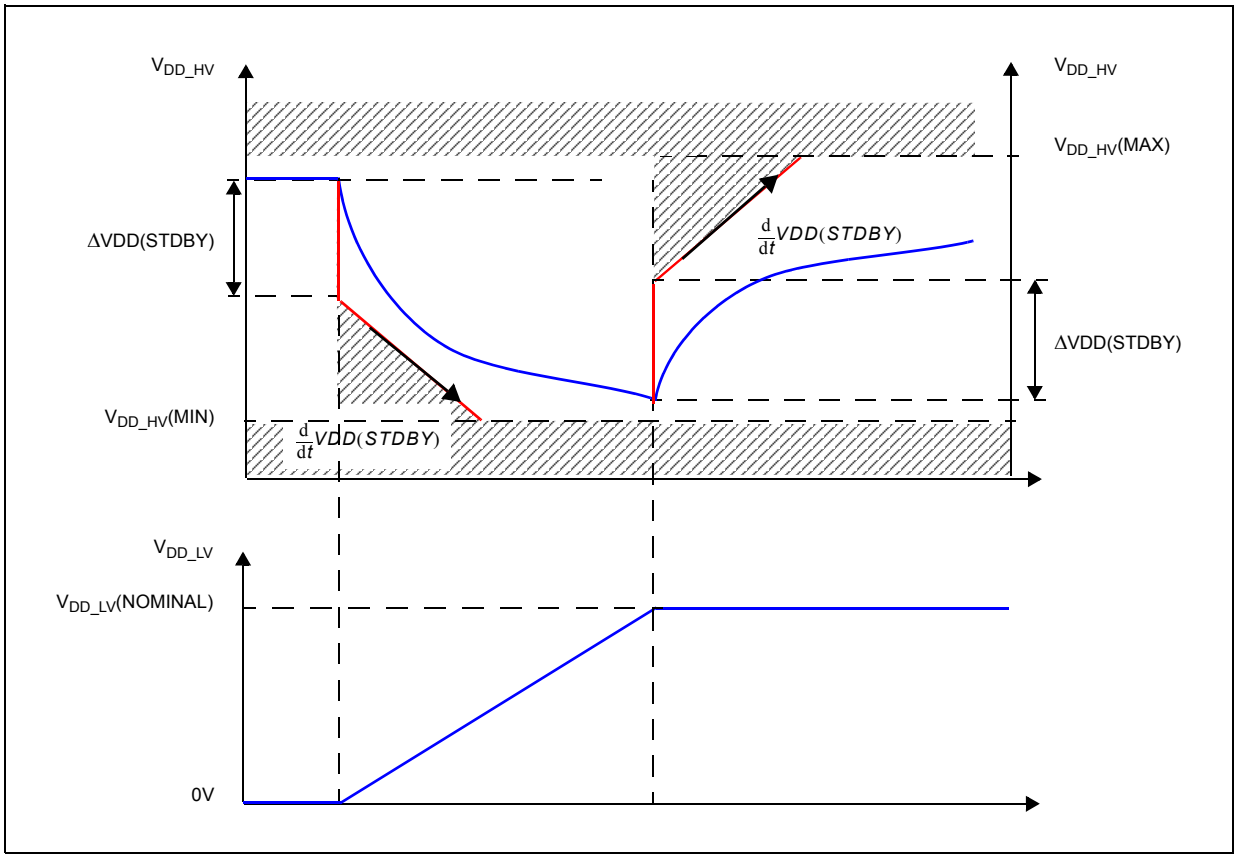

Figure 12. V_{DD_HV} and V_{DD_BV} supply constraints during STANDBY mode exit

Table 26. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
C_{REGn}	SR	—	Internal voltage regulator external capacitance	—	200	—	500	nF
R_{REG}	SR	—	Stability capacitor equivalent serial resistance	Range: 10 kHz to 20 MHz	—	—	0.2	Ω
C_{DEC1}	SR	—	Decoupling capacitance[2] ballast	V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 4.5 V to 5.5 V	100[3]	470[4]	—	nF
				V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 3 V to 3.6 V	400		—	
C_{DEC2}	SR	—	Decoupling capacitance regulator supply	V_{DD}/V_{SS} pair	10	100	—	nF
$\left\|\frac{d}{dt}VDD\right\|$	SR	—	Maximum slope on V_{DD}		—	—	250	mV/µs
$\|\Delta_{VDD(STDBY)}\|$	SR	—	Maximum instant variation on V_{DD} during standby exit		—	—	30	mV

Table 28. Power consumption on VDD_BV and VDD_HV

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{DDMAX}[2]	CC	D	RUN mode maximum average current	—		—	115	140[3]	mA
I_{DDRUN}[4]	CC	T	RUN mode typical average current[5]	f_{CPU} = 8 MHz		—	7	—	mA
		T		f_{CPU} = 16 MHz		—	18	—	
		T		f_{CPU} = 32 MHz		—	29	—	
		P		f_{CPU} = 48 MHz		—	40	100	
		P		f_{CPU} = 64 MHz		—	51	125	
I_{DDHALT}	CC	C	HALT mode current[6]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	8	15	mA
		P			T_A = 125 °C	—	14	25	
I_{DDSTOP}	CC	P	STOP mode current[7]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	180	700[8]	µA
		D			T_A = 55 °C	—	500	—	
		D			T_A = 85 °C	—	1	6[8]	mA
		D			T_A = 105 °C	—	2	9[8]	
		P			T_A = 125 °C	—	4.5	12[8]	
$I_{DDSTDBY2}$	CC	P	STANDBY2 mode current[9]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	30	100	µA
		D			T_A = 55 °C	—	75	—	
		D			T_A = 85 °C	—	180	700	
		D			T_A = 105 °C	—	315	1000	
		P			T_A = 125 °C	—	560	1700	
$I_{DDSTDBY1}$	CC	T	STANDBY1 mode current[10]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	20	60	µA
		D			T_A = 55 °C	—	45	—	
		D			T_A = 85 °C	—	100	350	
		D			T_A = 105 °C	—	165	500	
		D			T_A = 125 °C	—	280	900	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 I_{DDMAX} is drawn only from the V_{DD_BV} pin. Running consumption does not include I/Os toggling which is highly dependent on the application. The given value is thought to be a worst case value with all peripherals running, and code fetched from code flash while modify operation ongoing on data flash. Notice that this value can be significantly reduced by application: switch off not used peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.

3 Higher current may be sinked by device during power-up and standby exit. Please refer to in rush current on Table 26.

4 I_{DDRUN} is drawn only from the V_{DD_BV} pin. RUN current measured with typical application with accesses on both flash and RAM.

5 Only for the “P” classification: Data and Code Flash in Normal Power. Code fetched from RAM: Serial IPs CAN and LIN in loop back mode, DSPI as Master, PLL as system Clock (4 x Multiplier) peripherals on (eMIOS/CTU/ADC) and running at max frequency, periodic SW/WDG timer reset enabled.

6 Data Flash Power Down. Code Flash in Low Power. SIRC (128 kHz) and FIRC (16 MHz) on. 10 MHz XTAL clock. FlexCAN: instances: 0, 1, 2 ON (clocked but not reception or transmission), instances: 4, 5, 6 clock gated. LINFlex: instances: 0, 1, 2 ON (clocked but not reception or transmission), instance: 3 clock gated. eMIOS: instance: 0 ON (16 channels on PA[0]–PA[11] and PC[12]–PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication). RTC/API ON. PIT ON. STM ON. ADC ON but not conversion except 2 analog watchdog.

7 Only for the “P” classification: No clock, FIRC (16 MHz) off, SIRC (128 kHz) on, PLL off, HPvreg off, ULPVreg/LPVreg on. All possible peripherals off and clock gated. Flash in power down mode.

8 When going from RUN to STOP mode and the core consumption is > 6 mA, it is normal operation for the main regulator module to be kept on by the on-chip current monitoring circuit. This is most likely to occur with junction temperatures exceeding 125 °C and under these circumstances, it is possible for the current to initially exceed the maximum STOP specification by up to 2 mA. After entering stop, the application junction temperature will reduce to the ambient level and the main regulator will be automatically switched off when the load current is below 6 mA.

9 Only for the “P” classification: ULPreg on, HP/LPVreg off, 32 KB RAM on, device configured for minimum consumption, all possible modules switched off.

10 ULPreg on, HP/LPVreg off, 8 KB RAM on, device configured for minimum consumption, all possible modules switched off.

3.19 Flash memory electrical characteristics

3.19.1 Program/Erase characteristics

Table 29 shows the program and erase characteristics.

Table 29. Program and erase specifications

Symbol		C	Parameter	Value				Unit
				Min	Typ[1]	Initial max[2]	Max[3]	
$T_{dwprogram}$	CC	C	Double word (64 bits) program time[4]	—	22	50	500	µs
$T_{16Kpperase}$			16 KB block preprogram and erase time	—	300	500	5000	ms
$T_{32Kpperase}$			32 KB block preprogram and erase time	—	400	600	5000	ms
$T_{128Kpperase}$			128 KB block preprogram and erase time	—	800	1300	7500	ms
T_{esus}	CC	D	Erase suspend latency	—	—	30	30	µs

1 Typical program and erase times assume nominal supply values and operation at 25 °C.

2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3 The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

Table 35. ESD absolute maximum ratings[1] [2]

Symbol		C	Ratings	Conditions	Class	Max value	Unit
$V_{ESD(HBM)}$	CC	T	Electrostatic discharge voltage (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(MM)}$	CC	T	Electrostatic discharge voltage (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	
$V_{ESD(CDM)}$	CC	T	Electrostatic discharge voltage (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500	
						750 (corners)	

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3.20.3.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 36. Latch-up results

Symbol		C	Parameter	Conditions	Class
LU	CC	T	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

3.21 Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

The device provides an oscillator/resonator driver. Figure 14 describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

Table 37 provides the parameter description of 4 MHz to 16 MHz crystals used for the design simulations.

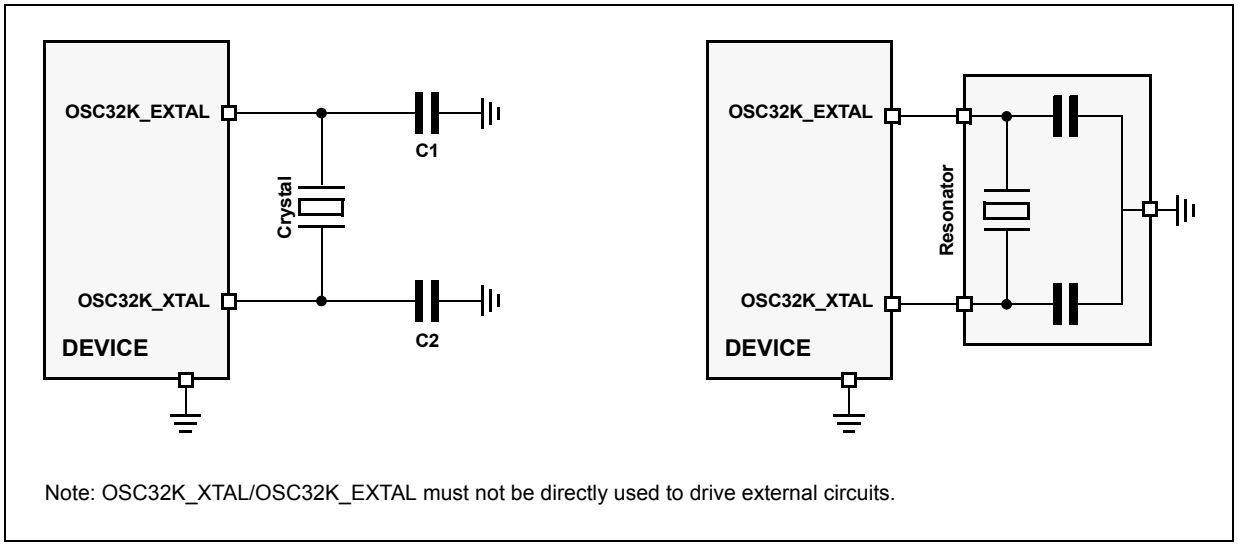

Figure 16. Crystal oscillator and resonator connection scheme

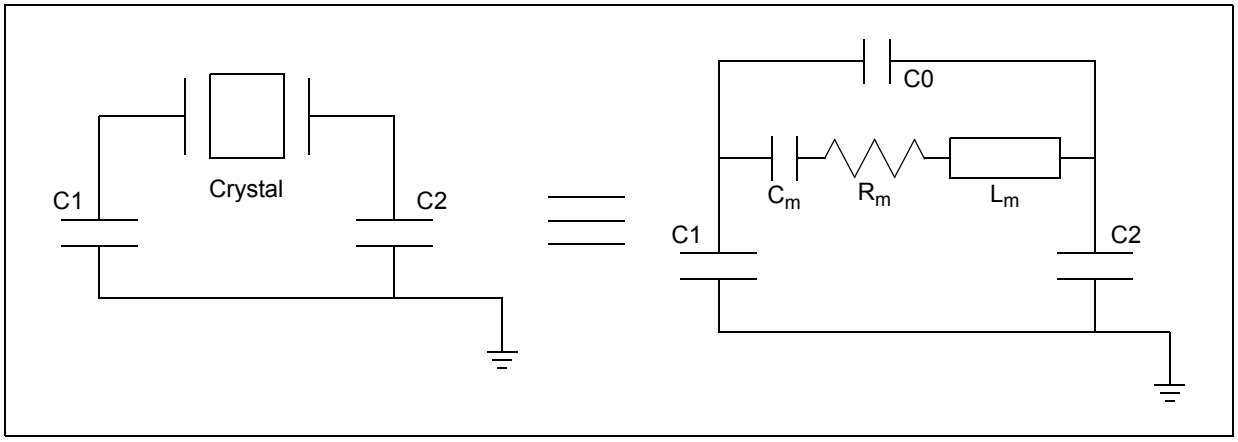

Figure 17. Equivalent circuit of a quartz crystal

Table 39. Crystal motional characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
L_m	Motional inductance	—	—	11.796	—	KH
C_m	Motional capacitance	—	—	2	—	fF
C1/C2	Load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground[2]	—	18	—	28	pF
R_m[3]	Motional resistance	AC coupled @ C0 = 2.85 pF[4]	—	—	65	kΩ
		AC coupled @ C0 = 4.9 pF[4]	—	—	50	
		AC coupled @ C0 = 7.0 pF[4]	—	—	35	
		AC coupled @ C0 = 9.0 pF[4]	—	—	30	

[1] Crystal used: Epson Toyocom MC306

Table 42. Fast internal RC oscillator (16 MHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
$I_{FIRCSTOP}$	CC	T	Fast internal RC oscillator high frequency and system clock current in stop mode	T_A = 25 °C	sysclk = off	—	500	—	µA
					sysclk = 2 MHz	—	600	—	
					sysclk = 4 MHz	—	700	—	
					sysclk = 8 MHz	—	900	—	
					sysclk = 16 MHz	—	1250	—	
t_{FIRCSU}	CC	C	Fast internal RC oscillator start-up time	V_{DD} = 5.0 V ± 10%		—	1.1	2.0	µs
$\Delta_{FIRCPRE}$	CC	T	Fast internal RC oscillator precision after software trimming of f_{FIRC}	T_A = 25 °C		–1	—	+1	%
$\Delta_{FIRCTRIM}$	CC	T	Fast internal RC oscillator trimming step	T_A = 25 °C		—	1.6		%
$\Delta_{FIRCVAR}$	CC	P	Fast internal RC oscillator variation in overtemperature and supply with respect to f_{FIRC} at T_A = 25 °C in high-frequency configuration	—		–5	—	+5	%

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

3.25 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a 128 kHz slow internal RC oscillator. This can be used as the reference clock for the RTC module.

Table 43. Slow internal RC oscillator (128 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{SIRC}	CC	P	Slow internal RC oscillator low frequency	T_A = 25 °C, trimmed	—	128	—	kHz
	SR	—		—	100	—	150	
I_{SIRC}[2],	CC	C	Slow internal RC oscillator low frequency current	T_A = 25 °C, trimmed	—	—	5	µA
t_{SIRCSU}	CC	P	Slow internal RC oscillator start-up time	T_A = 25 °C, V_{DD} = 5.0 V ± 10%	—	8	12	µs
$\Delta_{SIRCPRE}$	CC	C	Slow internal RC oscillator precision after software trimming of f_{SIRC}	T_A = 25 °C	–2	—	+2	%
$\Delta_{SIRCTRIM}$	CC	C	Slow internal RC oscillator trimming step	—	—	2.7	—	
$\Delta_{SIRCVAR}$	CC	C	Slow internal RC oscillator variation in temperature and supply with respect to f_{SIRC} at T_A = 55 °C in high frequency configuration	High frequency configuration	–10	—	+10	%

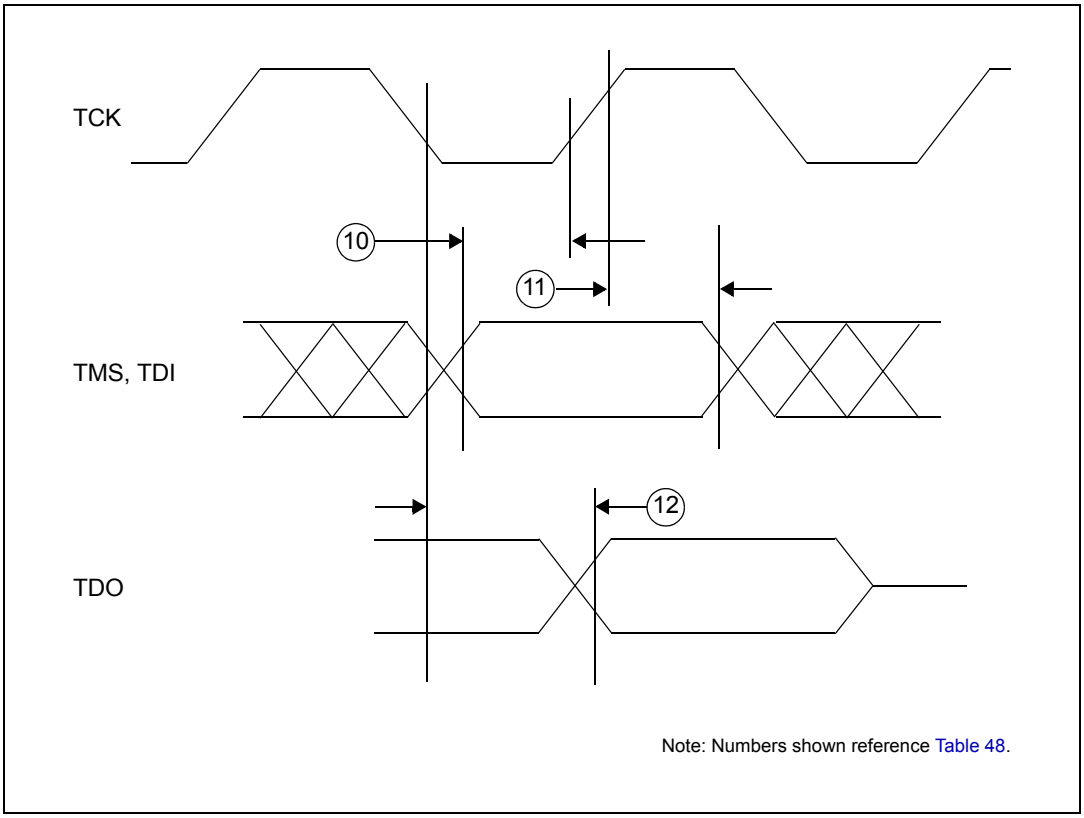

Figure 33. Nexus TDI, TMS, TDO timing

3.27.4 JTAG characteristics

Table 49. JTAG characteristics

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{JCYC}	CC	D	TCK cycle time	64	—	—	ns
2	t_{TDIS}	CC	D	TDI setup time	15	—	—	ns
3	t_{TDIH}	CC	D	TDI hold time	5	—	—	ns
4	t_{TMSS}	CC	D	TMS setup time	15	—	—	ns
5	t_{TMSH}	CC	D	TMS hold time	5	—	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO valid	—	—	33	ns
7	t_{TDOI}	CC	D	TCK low to TDO invalid	6	—	—	ns

4.1.2 100 LQFP

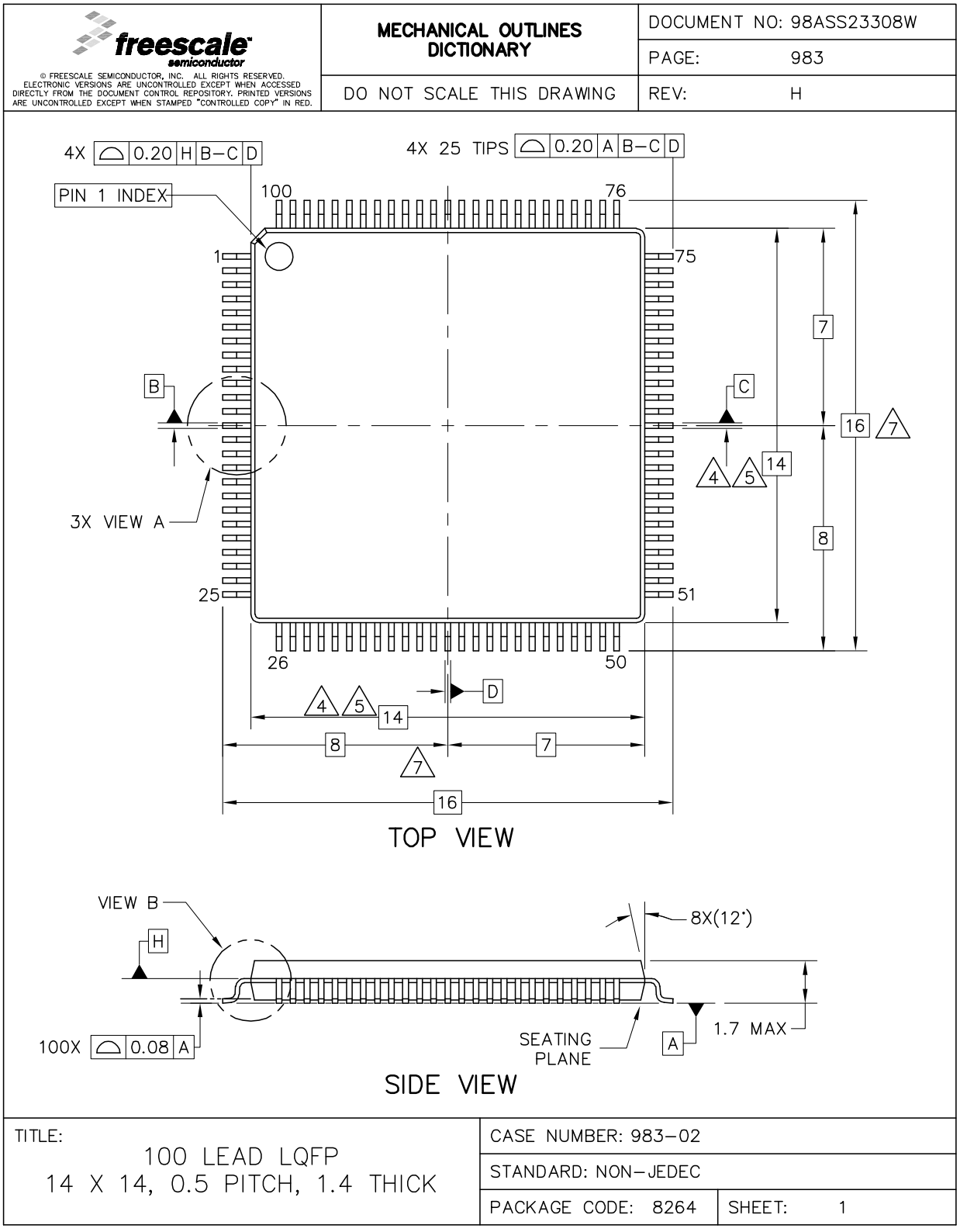

Figure 38. 100 LQFP package mechanical drawing (1 of 3)

4.1.3 144 LQFP

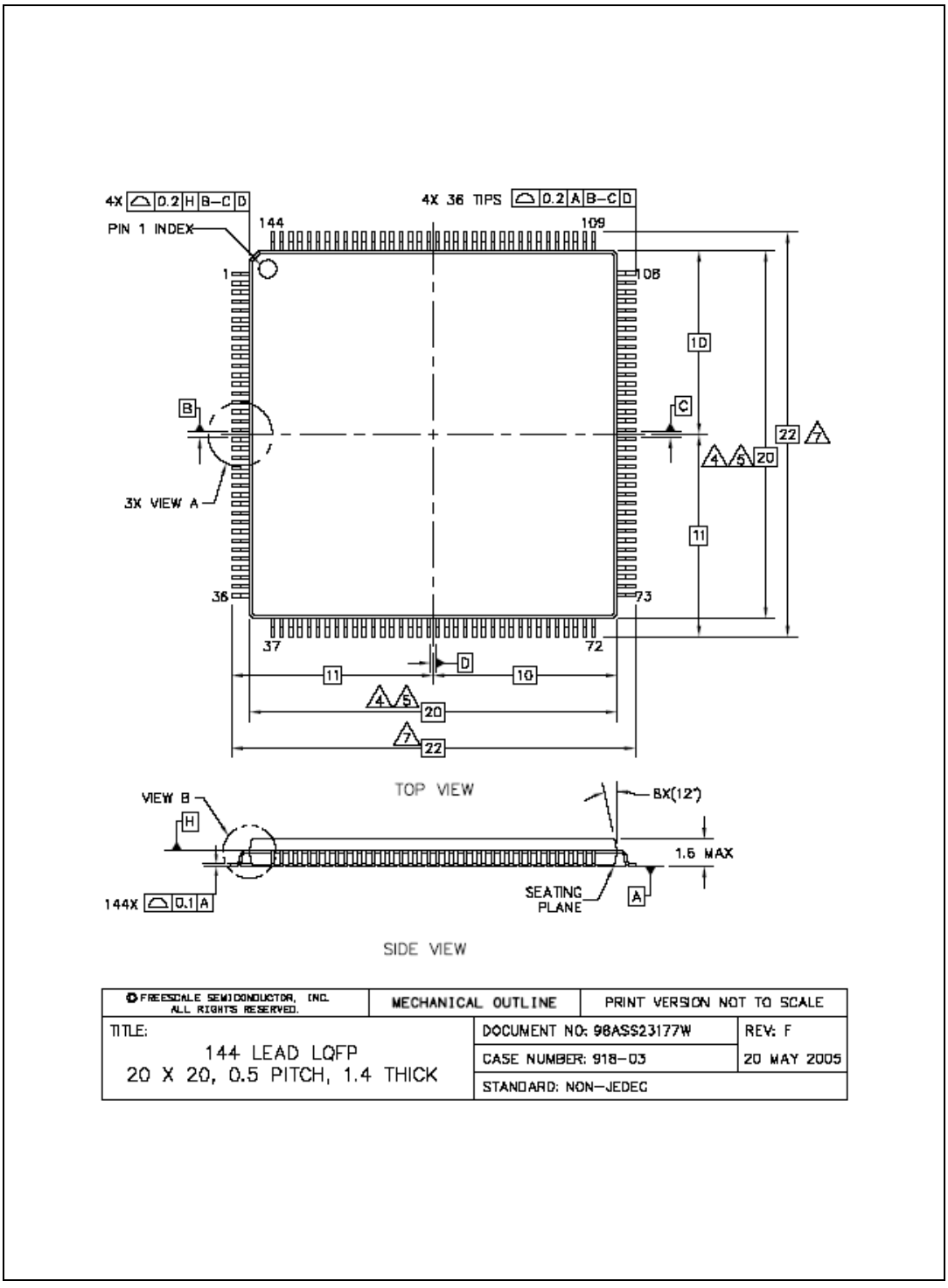

Figure 41. 144 LQFP package mechanical drawing (1 of 2)

Table 50. Revision history (continued)

Revision	Date	Description of Changes
4	06-Aug-2009	Updated Figure 6 Table 12 • V_{DD_ADC}: changed min value for “relative to V_{DD}” condition • V_{IN}: changed min value for “relative to V_{DD}” condition • I_{CORELV}: added new row Table 14 • $T_{A\ C\text{-}Grade\ Part}$, $T_{J\ C\text{-}Grade\ Part}$, $T_{A\ V\text{-}Grade\ Part}$, $T_{J\ V\text{-}Grade\ Part}$, $T_{A\ M\text{-}Grade\ Part}$, $T_{J\ M\text{-}Grade\ Part}$: added new rows • Changed capacitance value in footnote Table 21 • MEDIUM configuration: added condition for PAD3V5V = 0 Updated Figure 10 Table 26 • C_{DEC1}: changed min value • $I_{MREG:}$ changed max value • I_{DD_BV}: added max value footnote Table 27 • $V_{LVDHV3H}$: changed max value • $V_{LVDHV3L}$: added max value • $V_{LVDHV5H}$: changed max value • $V_{LVDHV5L}$: added max value Updated Table 28 Table 30 • Retention: deleted min value footnote for “Blocks with 100,000 P/E cycles“ Table 38 • I_{FXOSC}: added typ value Table 40 • V_{SXOSC}: changed typ value • $T_{SXOSCSU}$: added max value footnote Table 41 • Δt_{LTJIT}: added max value Updated Figure 38

Appendix A Abbreviations

Table A-1 lists abbreviations used but not defined elsewhere in this document.

Table A-1. Abbreviations

Abbreviation	Meaning
CMOS	Complementary metal–oxide–semiconductor
CPHA	Clock phase
CPOL	Clock polarity
CS	Peripheral chip select
EVTO	Event out
MCKO	Message clock out
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
SCK	Serial communications clock
SOUT	Serial data out
TBD	To be defined
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select

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