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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	123
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 36x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5604bk0mlq6

1 Feature set dependent on selected peripheral multiplexing—table shows example implementation
2 Based on 125 °C ambient operating temperature
3 See the eMIOS section of the device reference manual for information on the channel configuration and functions.
4 IC – Input Capture; OC – Output Compare; PWM – Pulse Width Modulation; MC – Modulus counter
5 SCI0, SCI1 and SCI2 are available. SCI3 is not available.
6 CAN0, CAN1 are available. CAN2, CAN3, CAN4 and CAN5 are not available.
7 CAN0, CAN1 and CAN2 are available. CAN3, CAN4 and CAN5 are not available.
8 I/O count based on multiplexing with peripherals
9 208 MAPBGA available only as development package for Nexus2+

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 —	GPIO[2] E0UC[2] — — WKPU[3][4]	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	3	3	5	9	F2
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 —	GPIO[3] E0UC[3] — — EIRQ[0]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	43	39	68	90	K15
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 —	GPIO[4] E0UC[4] — — WKPU[9][4]	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	20	20	29	43	N6
PA[5]	PCR[5]	AF0 AF1 AF2 AF3	GPIO[5] E0UC[5] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	51	51	79	118	C11
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 —	GPIO[6] E0UC[6] — — EIRQ[1]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	52	52	80	119	D11
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 —	GPIO[7] E0UC[7] LIN3TX — EIRQ[2]	SIUL eMIOS_0 LINFlex_3 — SIUL	I/O I/O O — I	S	Tristate	44	44	71	104	D16
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — N/A[6] —	GPIO[8] E0UC[8] — — EIRQ[3] ABS[0] LIN3RX	SIUL eMIOS_0 — — SIUL BAM LINFlex_3	I/O I/O — — I I I	S	Input, weak pull-up	45	45	72	105	C16
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 N/A[6]	GPIO[9] E0UC[9] — — FAB	SIUL eMIOS_0 — — BAM	I/O I/O — — I	S	Pull-down	46	46	73	106	C15

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PC[2]	PCR[34]	AF0 AF1 AF2 AF3 —	GPIO[34] SCK_1 CAN4TX[11] — EIRQ[5]	SIUL DSPI_1 FlexCAN_4 — SIUL	I/O I/O O — I	M	Tristate	50	50	78	117	A11
PC[3]	PCR[35]	AF0 AF1 AF2 AF3 — — —	GPIO[35] CS0_1 MA[0] — CAN1RX CAN4RX[11] EIRQ[6]	SIUL DSPI_1 ADC — FlexCAN_1 FlexCAN_4 SIUL	I/O I/O O — I I I	S	Tristate	49	49	77	116	B11
PC[4]	PCR[36]	AF0 AF1 AF2 AF3 — —	GPIO[36] — — — SIN_1 CAN3RX[11]	SIUL — — — DSPI_1 FlexCAN_3	I/O — — — I I	M	Tristate	62	62	92	131	B7
PC[5]	PCR[37]	AF0 AF1 AF2 AF3 —	GPIO[37] SOUT_1 CAN3TX[11] — EIRQ[7]	SIUL DSPI1 FlexCAN_3 — SIUL	I/O O O — I	M	Tristate	61	61	91	130	A7
PC[6]	PCR[38]	AF0 AF1 AF2 AF3	GPIO[38] LIN1TX — —	SIUL LINFlex_1 — —	I/O O — —	S	Tristate	16	16	25	36	R2
PC[7]	PCR[39]	AF0 AF1 AF2 AF3 — —	GPIO[39] — — — LIN1RX WKPU[12][4]	SIUL — — — LINFlex_1 WKPU	I/O — — — I I	S	Tristate	17	17	26	37	P3
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX — —	SIUL LINFlex_2 — —	I/O O — —	S	Tristate	63	63	99	143	A1

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PE[10]	PCR[74]	AF0 AF1 AF2 AF3 —	GPIO[74] LIN3TX CS3_1 — EIRQ[10]	SIUL LINFlex_3 DSPI_1 — SIUL	I/O O O — I	S	Tristate	—	—	11	15	G3
PE[11]	PCR[75]	AF0 AF1 AF2 AF3 — —	GPIO[75] — CS4_1 — LIN3RX WKPU[14][4]	SIUL — DSPI_1 — LINFlex_3 WKPU	I/O — O — I I	S	Tristate	—	—	13	17	H2
PE[12]	PCR[76]	AF0 AF1 AF2 AF3 — —	GPIO[76] — E1UC[19][13] — SIN_2 EIRQ[11]	SIUL — eMIOS_1 — DSPI_2 SIUL	I/O — I/O — I I	S	Tristate	—	—	76	109	C14
PE[13]	PCR[77]	AF0 AF1 AF2 AF3	GPIO[77] SOUT2 E1UC[20] —	SIUL DSPI_2 eMIOS_1 —	I/O O I/O —	S	Tristate	—	—	—	103	D15
PE[14]	PCR[78]	AF0 AF1 AF2 AF3 —	GPIO[78] SCK_2 E1UC[21] — EIRQ[12]	SIUL DSPI_2 eMIOS_1 — SIUL	I/O I/O I/O — I	S	Tristate	—	—	—	112	C13
PE[15]	PCR[79]	AF0 AF1 AF2 AF3	GPIO[79] CS0_2 E1UC[22] —	SIUL DSPI_2 eMIOS_1 —	I/O I/O I/O —	M	Tristate	—	—	—	113	A13
PF[0]	PCR[80]	AF0 AF1 AF2 AF3 —	GPIO[80] E0UC[10] CS3_1 — ANS[8]	SIUL eMIOS_0 DSPI_1 — ADC	I/O I/O O — I	J	Tristate	—	—	—	55	N10
PF[1]	PCR[81]	AF0 AF1 AF2 AF3 —	GPIO[81] E0UC[11] CS4_1 — ANS[9]	SIUL eMIOS_0 DSPI_1 — I	I/O I/O O — I	J	Tristate	—	—	—	56	P10

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PF[10]	PCR[90]	AF0 AF1 AF2 AF3	GPIO[90] — — —	SIUL — — —	I/O — — —	M	Tristate	—	—	—	38	R3
PF[11]	PCR[91]	AF0 AF1 AF2 AF3 —	GPIO[91] — — — WKPU[15][4]	SIUL — — — WKPU	I/O — — — I	S	Tristate	—	—	—	39	R4
PF[12]	PCR[92]	AF0 AF1 AF2 AF3	GPIO[92] E1UC[25] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	—	—	35	R1
PF[13]	PCR[93]	AF0 AF1 AF2 AF3 —	GPIO[93] E1UC[26] — — WKPU[16][4]	SIUL eMIOS_1 — — WKPU	I/O I/O — — I	S	Tristate	—	—	—	41	T6
PF[14]	PCR[94]	AF0 AF1 AF2 AF3	GPIO[94] CAN4TX[11] E1UC[27] CAN1TX	SIUL FlexCAN_4 eMIOS_1 FlexCAN_4	I/O O I/O O	M	Tristate	—	43	—	102	D14
PF[15]	PCR[95]	AF0 AF1 AF2 AF3 — — —	GPIO[95] — — — CAN1RX CAN4RX[11] EIRQ[13]	SIUL — — — FlexCAN_1 FlexCAN_4 SIUL	I/O — — — I I I	S	Tristate	—	42	—	101	E15
PG[0]	PCR[96]	AF0 AF1 AF2 AF3	GPIO[96] CAN5TX[11] E1UC[23] —	SIUL FlexCAN_5 eMIOS_1 —	I/O O I/O —	M	Tristate	—	41	—	98	E14
PG[1]	PCR[97]	AF0 AF1 AF2 AF3 — —	GPIO[97] — E1UC[24] — CAN5RX[11] EIRQ[14]	SIUL — eMIOS_1 — FlexCAN_5 SIUL	I/O — I/O — I I	S	Tristate	—	40	—	97	E13

[2] C_L includes device and package capacitances (C_{PKG} < 5 pF).

3.15.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in Table 22.

Table 22. I/O supply segment

Package	Supply segment					
	1	2	3	4	5	6
208 MAPBGA[1]	Equivalent to 144 LQFP segment pad distribution				MCKO	MDOn/MSEO
144 LQFP	pin20–pin49	pin51–pin99	pin100–pin122	pin 123–pin19	—	—
100 LQFP	pin16–pin35	pin37–pin69	pin70–pin83	pin 84–pin15	—	—
64 LQFP	pin8–pin26	pin28–pin55	pin56–pin7	—	—	—

[1] 208 MAPBGA available only as development package for Nexus2+

Table 23 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

Table 23. I/O consumption

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{SWTSLW}[2]	CC	D	Dynamic I/O current for SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16	
I_{SWTMED}[2]	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	29	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	17	
I_{SWTFST}[2]	CC	D	Dynamic I/O current for FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	110	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
I_{RMSSLW}	CC	D	Root mean square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.3	mA
				C_L = 25 pF, 4 MHz		—	—	3.2	
				C_L = 100 pF, 2 MHz		—	—	6.6	
				C_L = 25 pF, 2 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.6	
				C_L = 25 pF, 4 MHz		—	—	2.3	
				C_L = 100 pF, 2 MHz		—	—	4.7	

Table 23. I/O consumption (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{RMSMED}	CC	D	Root mean square I/O current for MEDIUM configuration	C_L = 25 pF, 13 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	mA
				C_L = 25 pF, 40 MHz		—	—	13.4	
				C_L = 100 pF, 13 MHz		—	—	18.3	
				C_L = 25 pF, 13 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	5	
				C_L = 25 pF, 40 MHz		—	—	8.5	
				C_L = 100 pF, 13 MHz		—	—	11	
I_{RMSFST}	CC	D	Root mean square I/O current for FAST configuration	C_L = 25 pF, 40 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	22	mA
				C_L = 25 pF, 64 MHz		—	—	33	
				C_L = 100 pF, 40 MHz		—	—	56	
				C_L = 25 pF, 40 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C_L = 25 pF, 64 MHz		—	—	20	
				C_L = 100 pF, 40 MHz		—	—	35	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to125 °C, unless otherwise specified

2 Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

Table 24 provides the weight of concurrent switching I/Os.

Due to the dynamic current limitations, the sum of the weight of concurrent switching I/Os on a single segment must not exceed 100% to ensure device functionality.

Table 24. I/O weight[1]

Supply segment			Pad	144/100 LQFP				64 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
144 LQFP	100 LQFP	64 LQFP[2]		SRC[3] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
4	4	3	PB[3]	10%	—	12%	—	10%	—	12%	—
			PC[9]	10%	—	12%	—	10%	—	12%	—
		—	PC[14]	9%	—	11%	—	—	—	—	—
		—	PC[15]	9%	13%	11%	12%	—	—	—	—
	—	—	PG[5]	9%	—	11%	—	—	—	—	—
	—	—	PG[4]	9%	12%	10%	11%	—	—	—	—
	—	—	PG[3]	9%	—	10%	—	—	—	—	—

Table 24. I/O weight[1] (continued)

Supply segment			Pad	144/100 LQFP				64 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
144 LQFP	100 LQFP	64 LQFP[2]		SRC[3] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
2	2	2	PB[9]	1%	—	1%	—	1%	—	1%	—
			PB[8]	1%	—	1%	—	1%	—	1%	—
			PB[10]	6%	—	7%	—	6%	—	7%	—
	—	—	PF[0]	6%	—	7%	—	—	—	—	—
	—	—	PF[1]	7%	—	8%	—	—	—	—	—
	—	—	PF[2]	7%	—	8%	—	—	—	—	—
	—	—	PF[3]	7%	—	9%	—	—	—	—	—
	—	—	PF[4]	8%	—	9%	—	—	—	—	—
	—	—	PF[5]	8%	—	10%	—	—	—	—	—
	—	—	PF[6]	8%	—	10%	—	—	—	—	—
	—	—	PF[7]	9%	—	10%	—	—	—	—	—
	2	—	PD[0]	1%	—	1%	—	—	—	—	—
		—	PD[1]	1%	—	1%	—	—	—	—	—
		—	PD[2]	1%	—	1%	—	—	—	—	—
		—	PD[3]	1%	—	1%	—	—	—	—	—
		—	PD[4]	1%	—	1%	—	—	—	—	—
		—	PD[5]	1%	—	1%	—	—	—	—	—
		—	PD[6]	1%	—	1%	—	—	—	—	—
		—	PD[7]	1%	—	1%	—	—	—	—	—
		—	PD[8]	1%	—	1%	—	—	—	—	—
		2	PB[4]	1%	—	1%	—	1%	—	1%	—
			PB[5]	1%	—	1%	—	1%	—	2%	—
			PB[6]	1%	—	1%	—	1%	—	2%	—
			PB[7]	1%	—	1%	—	1%	—	2%	—
		—	PD[9]	1%	—	1%	—	—	—	—	—
		—	PD[10]	1%	—	1%	—	—	—	—	—
		—	PD[11]	1%	—	1%	—	—	—	—	—
		2	PB[11]	11%	—	13%	—	17%	—	21%	—
		—	PD[12]	11%	—	13%	—	—	—	—	—
		2	PB[12]	11%	—	13%	—	18%	—	21%	—
		—	PD[13]	10%	—	12%	—	—	—	—	—

6 Data Flash Power Down. Code Flash in Low Power. SIRC (128 kHz) and FIRC (16 MHz) on. 10 MHz XTAL clock. FlexCAN: instances: 0, 1, 2 ON (clocked but not reception or transmission), instances: 4, 5, 6 clock gated. LINFlex: instances: 0, 1, 2 ON (clocked but not reception or transmission), instance: 3 clock gated. eMIOS: instance: 0 ON (16 channels on PA[0]–PA[11] and PC[12]–PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication). RTC/API ON. PIT ON. STM ON. ADC ON but not conversion except 2 analog watchdog.

7 Only for the “P” classification: No clock, FIRC (16 MHz) off, SIRC (128 kHz) on, PLL off, HPvreg off, ULPVreg/LPVreg on. All possible peripherals off and clock gated. Flash in power down mode.

8 When going from RUN to STOP mode and the core consumption is > 6 mA, it is normal operation for the main regulator module to be kept on by the on-chip current monitoring circuit. This is most likely to occur with junction temperatures exceeding 125 °C and under these circumstances, it is possible for the current to initially exceed the maximum STOP specification by up to 2 mA. After entering stop, the application junction temperature will reduce to the ambient level and the main regulator will be automatically switched off when the load current is below 6 mA.

9 Only for the “P” classification: ULPreg on, HP/LPVreg off, 32 KB RAM on, device configured for minimum consumption, all possible modules switched off.

10 ULPreg on, HP/LPVreg off, 8 KB RAM on, device configured for minimum consumption, all possible modules switched off.

3.19 Flash memory electrical characteristics

3.19.1 Program/Erase characteristics

Table 29 shows the program and erase characteristics.

Table 29. Program and erase specifications

Symbol		C	Parameter	Value				Unit
				Min	Typ[1]	Initial max[2]	Max[3]	
$T_{dwprogram}$	CC	C	Double word (64 bits) program time[4]	—	22	50	500	µs
$T_{16Kpperase}$			16 KB block preprogram and erase time	—	300	500	5000	ms
$T_{32Kpperase}$			32 KB block preprogram and erase time	—	400	600	5000	ms
$T_{128Kpperase}$			128 KB block preprogram and erase time	—	800	1300	7500	ms
T_{esus}	CC	D	Erase suspend latency	—	—	30	30	µs

1 Typical program and erase times assume nominal supply values and operation at 25 °C.

2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3 The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

Table 30. Flash module life

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
P/E	CC	C	Number of program/erase cycles per block over the operating temperature range (T_J)	16 KB blocks	100,000	—	—	cycles
				32 KB blocks	10,000	100,000	—	
				128 KB blocks	1,000	100,000	—	
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature[1]	Blocks with 0–1,000 P/E cycles	20	—	—	years
				Blocks with 1,001–10,000 P/E cycles	10	—	—	
				Blocks with 10,001–100,000 P/E cycles	5	—	—	

1 Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 31. Flash read access timing

Symbol		C	Parameter	Conditions[1]	Max	Unit
f_{READ}	CC	P	Maximum frequency for Flash reading	2 wait states	64	MHz
		C		1 wait state	40	
		C		0 wait states	20	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

3.19.2 Flash power supply DC characteristics

Table 32 shows the power supply DC characteristics on external supply.

Table 32. Flash memory power supply DC electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
I_{FREAD}[2]	CC	D	Sum of the current consumption on VDD_HV and VDD_BV on read access	Code flash memory module read f_{CPU} = 64 MHz[3]	—	15	33	mA
				Data flash memory module read f_{CPU} = 64 MHz[3]	—	15	33	
I_{FMOD}[2]	CC	D	Sum of the current consumption on VDD_HV and VDD_BV on matrix modification (program/erase)	Program/Erase ongoing while reading code flash memory registers f_{CPU} = 64 MHz[3]	—	15	33	mA
				Program/Erase ongoing while reading data flash memory registers f_{CPU} = 64 MHz[3]	—	15	33	

Table 32. Flash memory power supply DC electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
I_{FLPW}	CC	D	Sum of the current consumption on VDD_HV and VDD_BV	During code flash memory low-power mode	—	—	900	µA
				During data flash memory low-power mode	—	—	900	
I_{FPWD}	CC	D	Sum of the current consumption on VDD_HV and VDD_BV	During code flash memory power-down mode	—	—	150	µA
				During data flash memory power-down mode	—	—	150	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 This value is only relative to the actual duration of the read cycle

3 f_{CPU} 64 MHz can be achieved only at up to 105 °C

3.19.3 Start-up/Switch-off timings

Table 33. Start-up time/Switch-off time

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
$T_{FLARSTEXIT}$	CC	T	Delay for Flash module to exit reset mode	Code Flash	—	—	125	µs
		T		Data Flash	—	—	125	
$T_{FLALPEXIT}$	CC	T	Delay for Flash module to exit low-power mode	Code Flash	—	—	0.5	
		T		Data Flash	—	—	0.5	
$T_{FLAPDEXIT}$	CC	T	Delay for Flash module to exit power-down mode	Code Flash	—	—	30	
		T		Data Flash	—	—	30	
$T_{FLALPENTRY}$	CC	T	Delay for Flash module to enter low-power mode	Code Flash	—	—	0.5	
		T		Data Flash	—	—	0.5	
$T_{FLAPDENTRY}$	CC	T	Delay for Flash module to enter power-down mode	Code Flash	—	—	1.5	
		T		Data Flash	—	—	1.5	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

3.20 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

3.20.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Table 35. ESD absolute maximum ratings[1] [2]

Symbol		C	Ratings	Conditions	Class	Max value	Unit
$V_{ESD(HBM)}$	CC	T	Electrostatic discharge voltage (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(MM)}$	CC	T	Electrostatic discharge voltage (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	
$V_{ESD(CDM)}$	CC	T	Electrostatic discharge voltage (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500	
						750 (corners)	

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3.20.3.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 36. Latch-up results

Symbol		C	Parameter	Conditions	Class
LU	CC	T	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

3.21 Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

The device provides an oscillator/resonator driver. Figure 14 describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

Table 37 provides the parameter description of 4 MHz to 16 MHz crystals used for the design simulations.

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
[2] This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

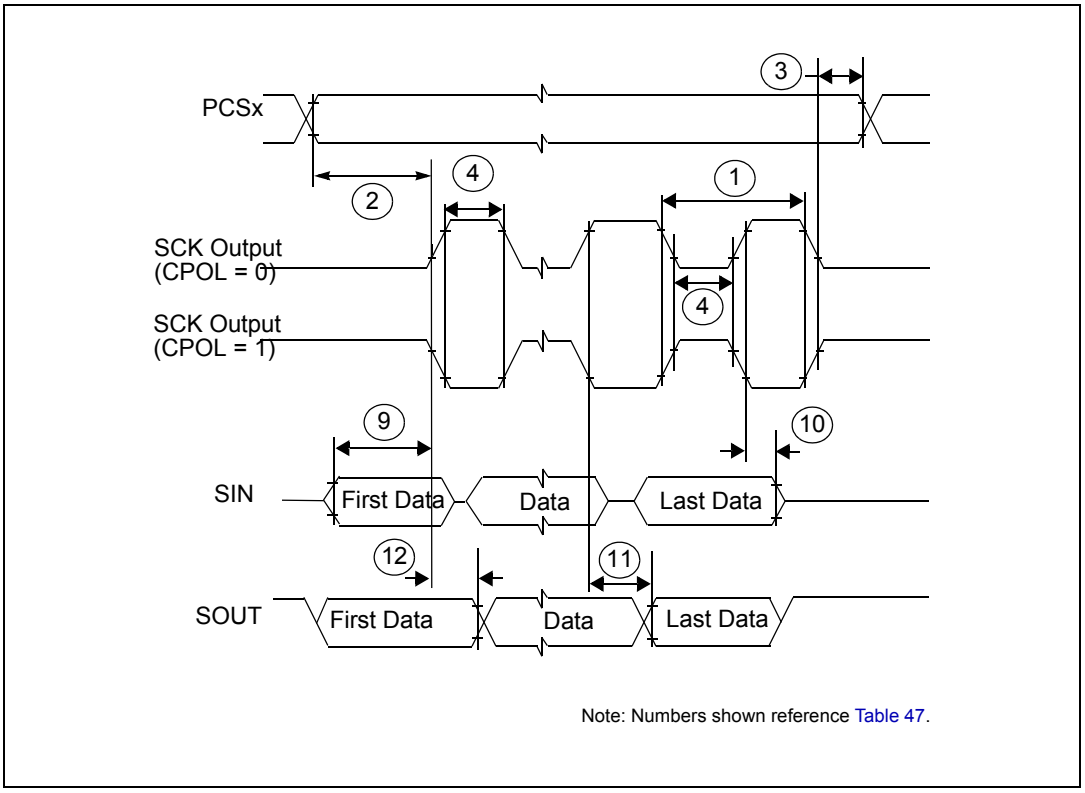

Figure 28. DSPI modified transfer format timing – master, CPHA = 0

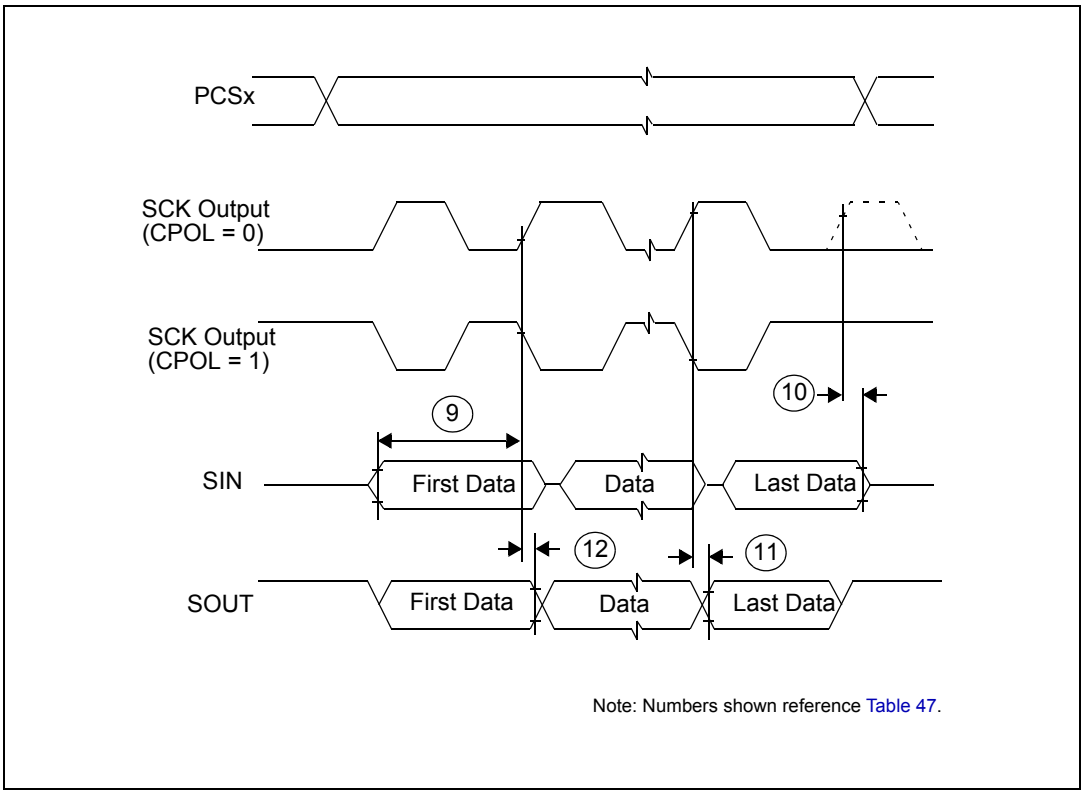

Figure 29. DSPI modified transfer format timing – master, CPHA = 1

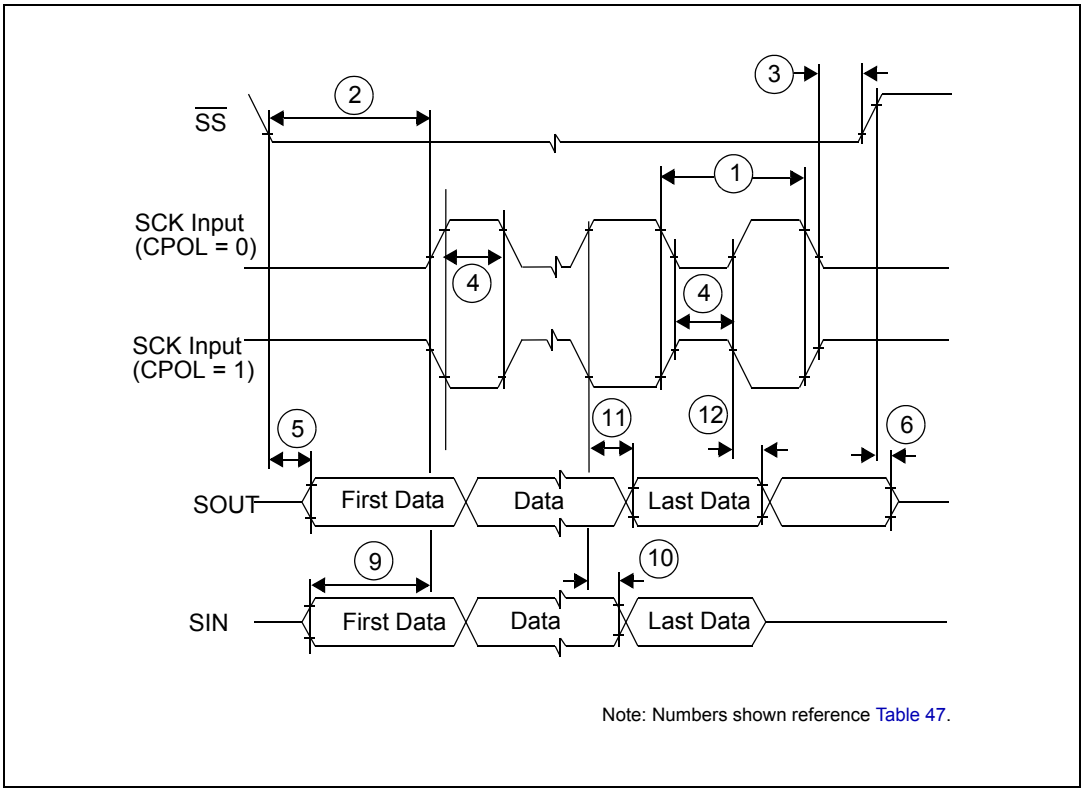

Figure 30. DSPI modified transfer format timing – slave, CPHA = 0

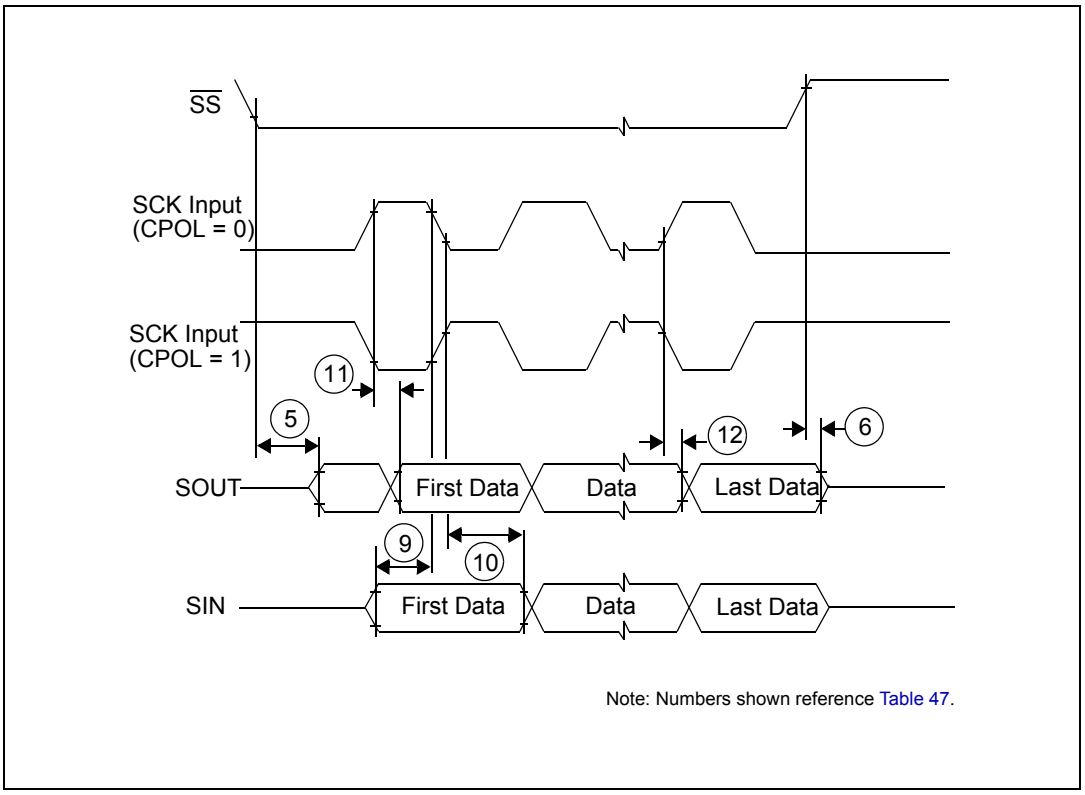

Figure 31. DSPI modified transfer format timing – slave, CPHA = 1

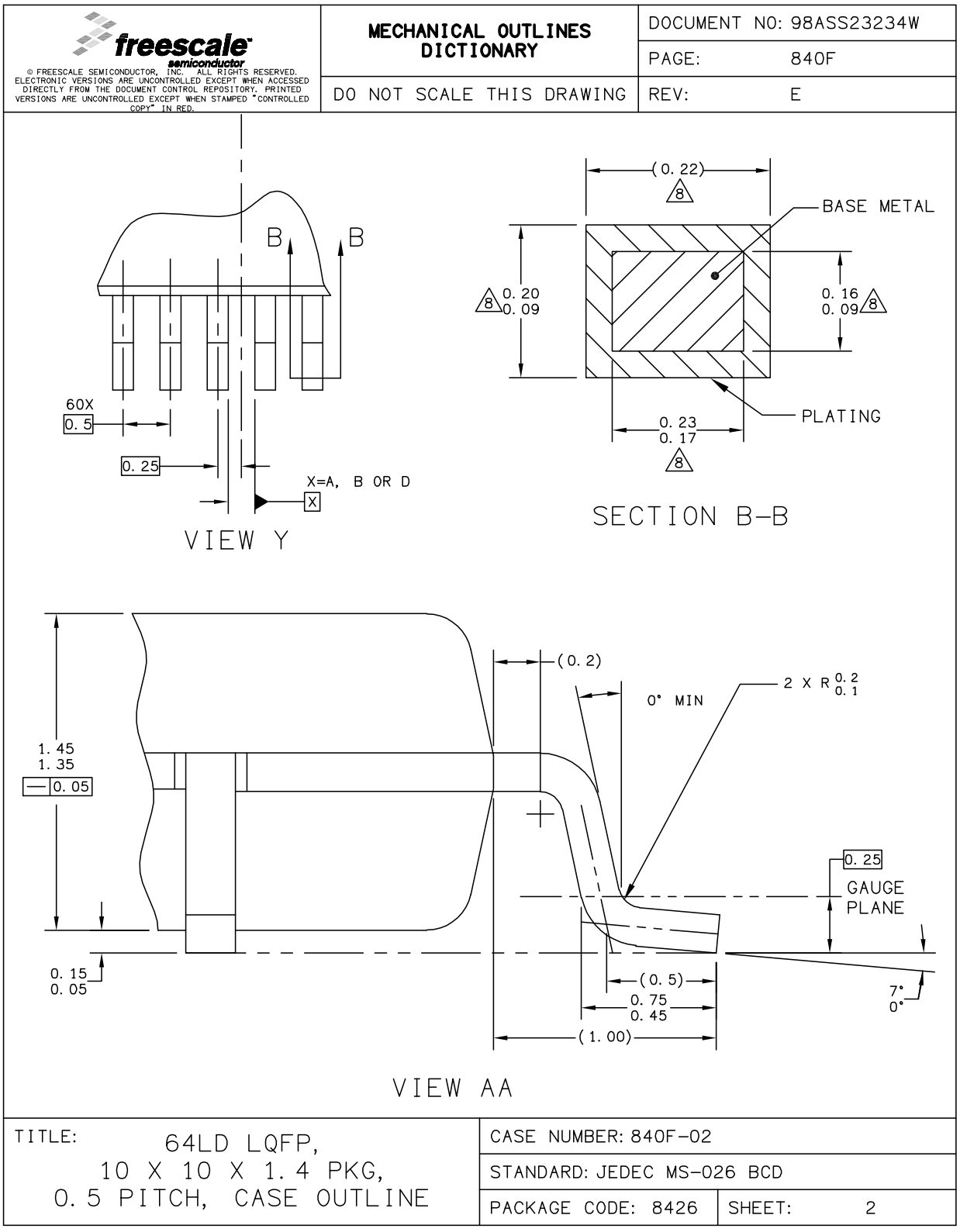

Figure 36. 64 LQFP package mechanical drawing (2 of 3)

4.1.4 208 MAPBGA

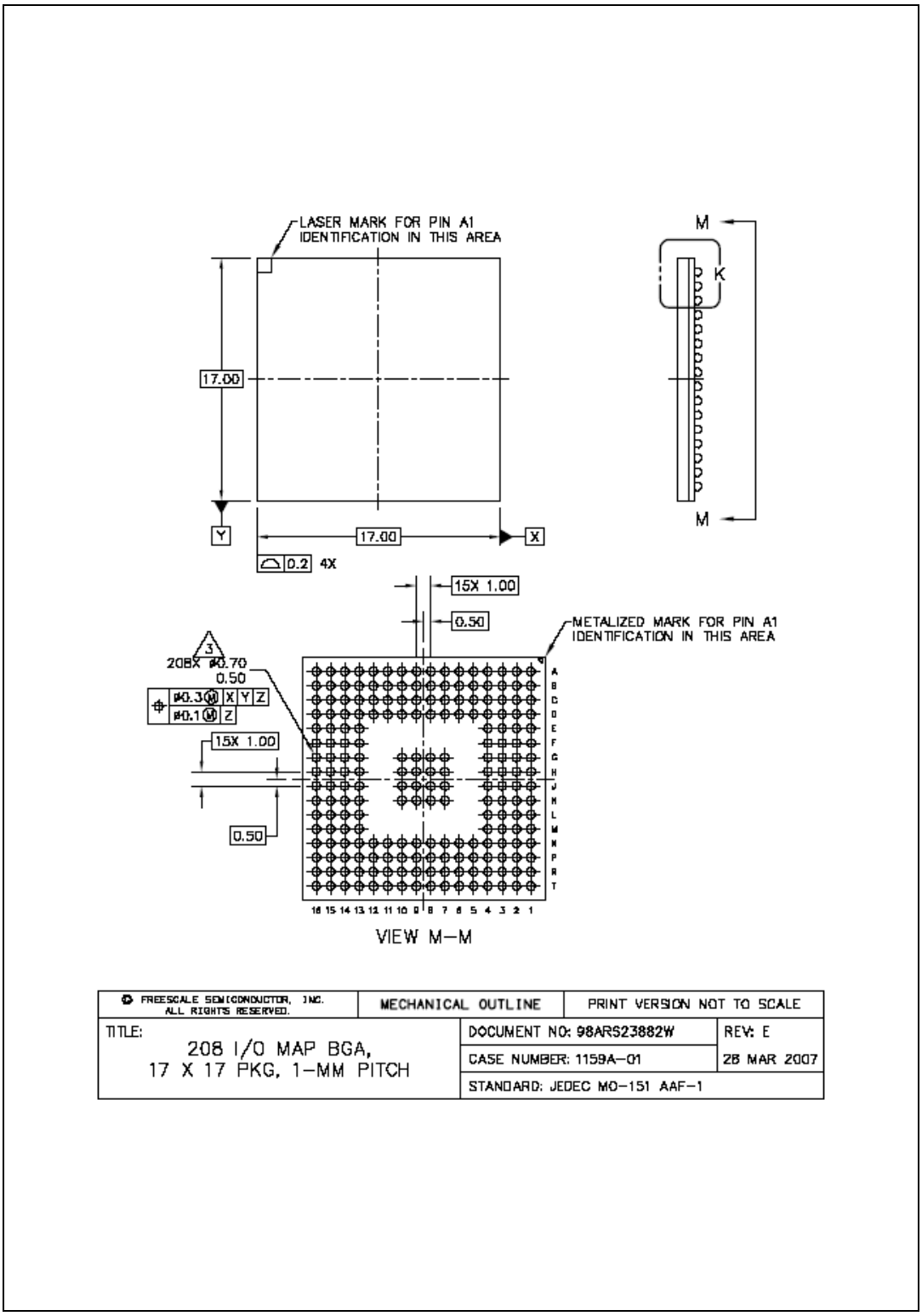

Figure 43. 208 MAPBGA package mechanical drawing (1 of 2)

Table 50. Revision history (continued)

Revision	Date	Description of Changes
2	06-Mar-2009	Made minor editing and formatting changes to improve readability Harmonized oscillator naming throughout document Features: —Replaced 32 KB with 48 KB as max SRAM size —Updated description of INTC —Changed max number of GPIO pins from 121 to 123 Updated Section 1.2, Description Updated Table 2 Added Section 2, Block diagram Section 3, Package pinouts and signal descriptions: Removed signal descriptions (these are found in the device reference manual) Updated Figure 5: —Replaced VPP with VSS_HV on pin 18 —Added MA[1] as AF3 for PC[10] (pin 28) —Added MA[0] as AF2 for PC[3] (pin 116) —Changed description for pin 120 to PH[10] / GPIO[122] / TMS —Changed description for pin 127 to PH[9] / GPIO[121] / TCK —Replaced NMI[0] with NMI on pin 11 Updated Figure 4: —Replaced VPP with VSS_HV on pin 14 —Added MA[1] as AF3 for PC[10] (pin 22) —Added MA[0] as AF2 for PC[3] (pin 77) —Changed description for pin 81 to PH[10] / GPIO[122] / TMS —Changed description for pin 88 to PH[9] / GPIO[121] / TCK —Removed E1UC[19] from pin 76 —Replaced [11] with WKUP[11] for PB[3] (pin 1) —Replaced NMI[0] with NMI on pin 7 Updated Figure 6: —Changed description for ball B8 from TCK to PH[9] —Changed description for ball B9 from TMS to PH[10] —Updated descriptions for balls R9 and T9 Added Section 3.10, Parameter classification and tagged parameters in tables where appropriate Added Section 3.11, NVUSRO register Updated Table 12 Section 3.13, Recommended operating conditions: Added note on RAM data retention to end of section Updated Table 13 and Table 14 Added Section 3.14.1, Package thermal characteristics Updated Section 3.14.2, Power considerations Updated Figure 7

Table 50. Revision history (continued)

Revision	Date	Description of Changes
9	16 June 2011	Formatting and minor editorial changes throughout Harmonized oscillator nomenclature Removed all instances of note “All 64 LQFP information is indicative and must be confirmed during silicon validation.” Device comparison table: changed temperature value in footnote 2 from 105 °C to 125 °C MPC560xB LQFP 64-pin configuration and MPC560xC LQFP 64-pin configuration: renamed pin 6 from VPP_TEST to VSS_HV Removed “Pin Muxing” section; added sections “Pad configuration during reset phases”, “Voltage supply pins”, “Pad types”, “System pins,” “Functional ports”, and “Nexus 2+ pins” Section “NVUSRO register”: edited content to separate configuration into electrical parameters and digital functionality; updated footnote describing default value of ‘1’ in field descriptions NVUSRO[PAD3V5V] and NVUSRO[OSCILLATOR_MARGIN] Added section “NVUSRO[WATCHDOG_EN] field description” Recommended operating conditions (3.3 V) and Recommended operating conditions (5.0 V): updated conditions for ambient and junction temperature characteristics I/O input DC electrical characteristics: updated I_{LKG} characteristics Section “I/O pad current specification”: removed content referencing the I_{DYNSEG} maximum value I/O consumption: replaced instances of “Root medium square” with “Root mean square” I/O weight: replaced instances of bit “SRE” with “SRC”; added pads PH[9] and PH[10]; added supply segments; removed weight values in 64-pin LQFP for pads that do not exist in that package Reset electrical characteristics: updated parameter classification for $\|I_{WPU}\|$ Updated Voltage regulator electrical characteristics Section “Low voltage detector electrical characteristics”: changed title (was “Voltage monitor electrical characteristics”); added event status flag names found in RGM chapter of device reference manual to POR module and LVD descriptions; replaced instances of “Low voltage monitor” with “Low voltage detector”; updated values for $V_{LVDLVBKPL}$ and $V_{LVDLVCORL}$; replaced “LVD_DIGBKP” with “LVDLVBKP” in note Updated section “Power consumption” Fast external crystal oscillator (4 to 16 MHz) electrical characteristics: updated parameter classification for $V_{FXOSCOP}$ Crystal oscillator and resonator connection scheme: added footnote about possibility of adding a series resistor Slow external crystal oscillator (32 kHz) electrical characteristics: updated footnote 1 FMPLL electrical characteristics: added short term jitter characteristics; inserted “—” in empty min value cell of t_{lock} row Section “Input impedance and ADC accuracy”: changed “V_A/V_{A2}” to “V_{A2}/V_A” in Equation 11 ADC input leakage current: updated I_{LKG} characteristics ADC conversion characteristics: updated symbols On-chip peripherals current consumption: changed “supply current on “$V_{DD\_HV\_ADC}$” to “supply current on” V_{DD_HV}” in $I_{DD\_HV(FLASH)}$ row; updated $I_{DD\_HV(PLL)}$ value—was 3 * f_{periph}, is 30 * f_{periph}; updated footnotes DSPI characteristics: added rows t_{PCSC} and t_{PASC} Added DSPI PCS strobe (PCSS) timing diagram

Appendix A Abbreviations

Table A-1 lists abbreviations used but not defined elsewhere in this document.

Table A-1. Abbreviations

Abbreviation	Meaning
CMOS	Complementary metal–oxide–semiconductor
CPHA	Clock phase
CPOL	Clock polarity
CS	Peripheral chip select
EVTO	Event out
MCKO	Message clock out
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
SCK	Serial communications clock
SOUT	Serial data out
TBD	To be defined
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select