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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	123
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 36x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5604bk0vlq6

1 Feature set dependent on selected peripheral multiplexing—table shows example implementation
2 Based on 125 °C ambient operating temperature
3 See the eMIOS section of the device reference manual for information on the channel configuration and functions.
4 IC – Input Capture; OC – Output Compare; PWM – Pulse Width Modulation; MC – Modulus counter
5 SCI0, SCI1 and SCI2 are available. SCI3 is not available.
6 CAN0, CAN1 are available. CAN2, CAN3, CAN4 and CAN5 are not available.
7 CAN0, CAN1 and CAN2 are available. CAN3, CAN4 and CAN5 are not available.
8 I/O count based on multiplexing with peripherals
9 208 MAPBGA available only as development package for Nexus2+

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PB[3]	PCR[19]	AF0 AF1 AF2 AF3 — —	GPIO[19] — SCL — WKPU[11][4] LIN0RX	SIUL — I2C_0 — WKPU LINFlex_0	I/O — I/O — I I	S	Tristate	1	1	1	1	C3
PB[4]	PCR[20]	AF0 AF1 AF2 AF3 —	GPIO[20] — — — GPI[0]	SIUL — — — ADC	I — — — I	I	Tristate	32	32	50	72	T16
PB[5]	PCR[21]	AF0 AF1 AF2 AF3 —	GPIO[21] — — — GPI[1]	SIUL — — — ADC	I — — — I	I	Tristate	35	—	53	75	R16
PB[6]	PCR[22]	AF0 AF1 AF2 AF3 —	GPIO[22] — — — GPI[2]	SIUL — — — ADC	I — — — I	I	Tristate	36	—	54	76	P15
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 —	GPIO[23] — — — GPI[3]	SIUL — — — ADC	I — — — I	I	Tristate	37	35	55	77	P16
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 — —	GPIO[24] — — — ANS[0] OSC32K_XTAL[7]	SIUL — — — ADC SXOSC	I — — — I I/O	I	Tristate	30	30	39	53	R9
PB[9]	PCR[25]	AF0 AF1 AF2 AF3 — —	GPIO[25] — — — ANS[1] OSC32K_EXTAL[7]	SIUL — — — ADC SXOSC	I — — — I I/O	I	Tristate	29	29	38	52	T9

[1] Default manufacturing value is ‘1’. Value can be programmed by customer in Shadow Flash.

3.11.2 NVUSRO[OSCILLATOR_MARGIN] field description

The fast external crystal oscillator consumption is dependent on the OSCILLATOR_MARGIN bit value. Table 10 shows how NVUSRO[OSCILLATOR_MARGIN] controls the device configuration.

Table 10. OSCILLATOR_MARGIN field description

Value[1]	Description
0	Low consumption configuration (4 MHz/8 MHz)
1	High margin configuration (4 MHz/16 MHz)

[1] Default manufacturing value is ‘1’. Value can be programmed by customer in Shadow Flash.

3.11.3 NVUSRO[WATCHDOG_EN] field description

The watchdog enable/disable configuration after reset is dependent on the WATCHDOG_EN bit value. Table 11 shows how NVUSRO[WATCHDOG_EN] controls the device configuration.

Table 11. WATCHDOG_EN field description

Value[1]	Description
0	Disable after reset
1	Enable after reset

[1] Default manufacturing value is ‘1’. Value can be programmed by customer in Shadow Flash.

3.14 Thermal characteristics

3.14.1 Package thermal characteristics

Table 15. LQFP thermal characteristics[1]

Symbol		C	Parameter	Conditions[2]	Pin count	Value	Unit
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection[3]	Single-layer board - 1s	64	60	°C/W
					100	64	
					144	64	
				Four-layer board - 2s2p	64	42	
					100	51	
					144	49	
$R_{\theta JB}$	CC	D	Thermal resistance, junction-to-board[4]	Single-layer board - 1s	64	24	°C/W
					100	36	
					144	37	
				Four-layer board - 2s2p	64	24	
					100	34	
					144	35	
$R_{\theta JC}$	CC	D	Thermal resistance, junction-to-case[5]	Single-layer board - 1s	64	11	°C/W
					100	22	
					144	22	
				Four-layer board - 2s2p	64	11	
					100	22	
					144	22	
Ψ_{JB}	CC	D	Junction-to-board thermal characterization parameter, natural convection	Single-layer board - 1s	64	TBD	°C/W
					100	33	
					144	34	
				Four-layer board - 2s2p	64	TBD	
					100	34	
					144	35	
Ψ_{JC}	CC	D	Junction-to-case thermal characterization parameter, natural convection	Single-layer board - 1s	64	TBD	°C/W
					100	9	
					144	10	
				Four-layer board - 2s2p	64	TBD	
					100	9	
					144	10	

[1] Thermal characteristics are based on simulation.

Table 20. FAST configuration output buffer electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OL}	CC	P	Output low level FAST configuration	Push Pull	I_{OL} = 14mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 7mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 11mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.15.4 Output pin transition times

Table 21. Output pin transition times

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin[2] SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
t_{tr}	CC	D	Output transition time output pin[2] MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	
t_{tr}	CC	D	Output transition time output pin[2] FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	4	ns
				C_L = 50 pF		—	—	6	
				C_L = 100 pF		—	—	12	
				C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	4	
				C_L = 50 pF		—	—	7	
				C_L = 100 pF		—	—	12	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

Table 24. I/O weight[1] (continued)

Supply segment			Pad	144/100 LQFP				64 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
144 LQFP	100 LQFP	64 LQFP[2]		SRC[3] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
2	2	2	PB[9]	1%	—	1%	—	1%	—	1%	—
			PB[8]	1%	—	1%	—	1%	—	1%	—
			PB[10]	6%	—	7%	—	6%	—	7%	—
	—	—	PF[0]	6%	—	7%	—	—	—	—	—
	—	—	PF[1]	7%	—	8%	—	—	—	—	—
	—	—	PF[2]	7%	—	8%	—	—	—	—	—
	—	—	PF[3]	7%	—	9%	—	—	—	—	—
	—	—	PF[4]	8%	—	9%	—	—	—	—	—
	—	—	PF[5]	8%	—	10%	—	—	—	—	—
	—	—	PF[6]	8%	—	10%	—	—	—	—	—
	—	—	PF[7]	9%	—	10%	—	—	—	—	—
	2	—	PD[0]	1%	—	1%	—	—	—	—	—
		—	PD[1]	1%	—	1%	—	—	—	—	—
		—	PD[2]	1%	—	1%	—	—	—	—	—
		—	PD[3]	1%	—	1%	—	—	—	—	—
		—	PD[4]	1%	—	1%	—	—	—	—	—
		—	PD[5]	1%	—	1%	—	—	—	—	—
		—	PD[6]	1%	—	1%	—	—	—	—	—
		—	PD[7]	1%	—	1%	—	—	—	—	—
		—	PD[8]	1%	—	1%	—	—	—	—	—
		2	PB[4]	1%	—	1%	—	1%	—	1%	—
			PB[5]	1%	—	1%	—	1%	—	2%	—
			PB[6]	1%	—	1%	—	1%	—	2%	—
			PB[7]	1%	—	1%	—	1%	—	2%	—
		—	PD[9]	1%	—	1%	—	—	—	—	—
		—	PD[10]	1%	—	1%	—	—	—	—	—
		—	PD[11]	1%	—	1%	—	—	—	—	—
		2	PB[11]	11%	—	13%	—	17%	—	21%	—
		—	PD[12]	11%	—	13%	—	—	—	—	—
		2	PB[12]	11%	—	13%	—	18%	—	21%	—
		—	PD[13]	10%	—	12%	—	—	—	—	—

Table 24. I/O weight[1] (continued)

Supply segment			Pad	144/100 LQFP				64 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
144 LQFP	100 LQFP	64 LQFP[2]		SRC[3] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
2	2	2	PB[13]	10%	—	12%	—	18%	—	21%	—
		—	PD[14]	10%	—	12%	—	—	—	—	—
		2	PB[14]	10%	—	12%	—	18%	—	21%	—
		—	PD[15]	10%	—	11%	—	—	—	—	—
		2	PB[15]	9%	—	11%	—	18%	—	21%	—
			PA[3]	9%	—	11%	—	18%	—	21%	—
	—	—	PG[13]	9%	13%	10%	11%	—	—	—	—
	—	—	PG[12]	9%	12%	10%	11%	—	—	—	—
	—	—	PH[0]	5%	8%	6%	7%	—	—	—	—
	—	—	PH[1]	5%	7%	6%	6%	—	—	—	—
	—	—	PH[2]	5%	6%	5%	6%	—	—	—	—
	—	—	PH[3]	4%	6%	5%	5%	—	—	—	—
	—	—	PG[1]	4%	—	4%	—	—	—	—	—
	—	—	PG[0]	3%	4%	4%	4%	—	—	—	—
3	—	—	PF[15]	3%	—	4%	—	—	—	—	—
	—	—	PF[14]	4%	5%	5%	5%	—	—	—	—
	—	—	PE[13]	4%	—	5%	—	—	—	—	—
	3	2	PA[7]	5%	—	6%	—	16%	—	19%	—
			PA[8]	5%	—	6%	—	16%	—	19%	—
			PA[9]	5%	—	6%	—	15%	—	18%	—
			PA[10]	6%	—	7%	—	15%	—	18%	—
			PA[11]	6%	—	8%	—	14%	—	17%	—
		—	PE[12]	7%	—	8%	—	—	—	—	—
	—	—	PG[14]	7%	—	8%	—	—	—	—	—
	—	—	PG[15]	7%	10%	8%	9%	—	—	—	—
	—	—	PE[14]	7%	—	8%	—	—	—	—	—
	—	—	PE[15]	7%	9%	8%	8%	—	—	—	—
	—	—	PG[10]	6%	—	8%	—	—	—	—	—
	—	—	PG[11]	6%	9%	7%	8%	—	—	—	—
	3	2	PC[3]	6%	—	7%	—	7%	—	9%	—
			PC[2]	6%	8%	7%	7%	6%	9%	8%	8%

- HV—High voltage external power supply for voltage regulator module. This must be provided externally through VDD_HV power pin.
- BV—High voltage external power supply for internal ballast module. This must be provided externally through VDD_BV power pin. Voltage values should be aligned with V_{DD}.
- LV—Low voltage internal power supply for core, FMPLL and flash digital logic. This is generated by the internal voltage regulator but provided outside to connect stability capacitor. It is further split into four main domains to ensure noise isolation between critical LV modules within the device:
  - LV_COR—Low voltage supply for the core. It is also used to provide supply for FMPLL through double bonding.
  - LV_CFLA—Low voltage supply for code flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
  - LV_DFLA—Low voltage supply for data flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
  - LV_PLL—Low voltage supply for FMPLL. It is shorted to LV_COR through double bonding.

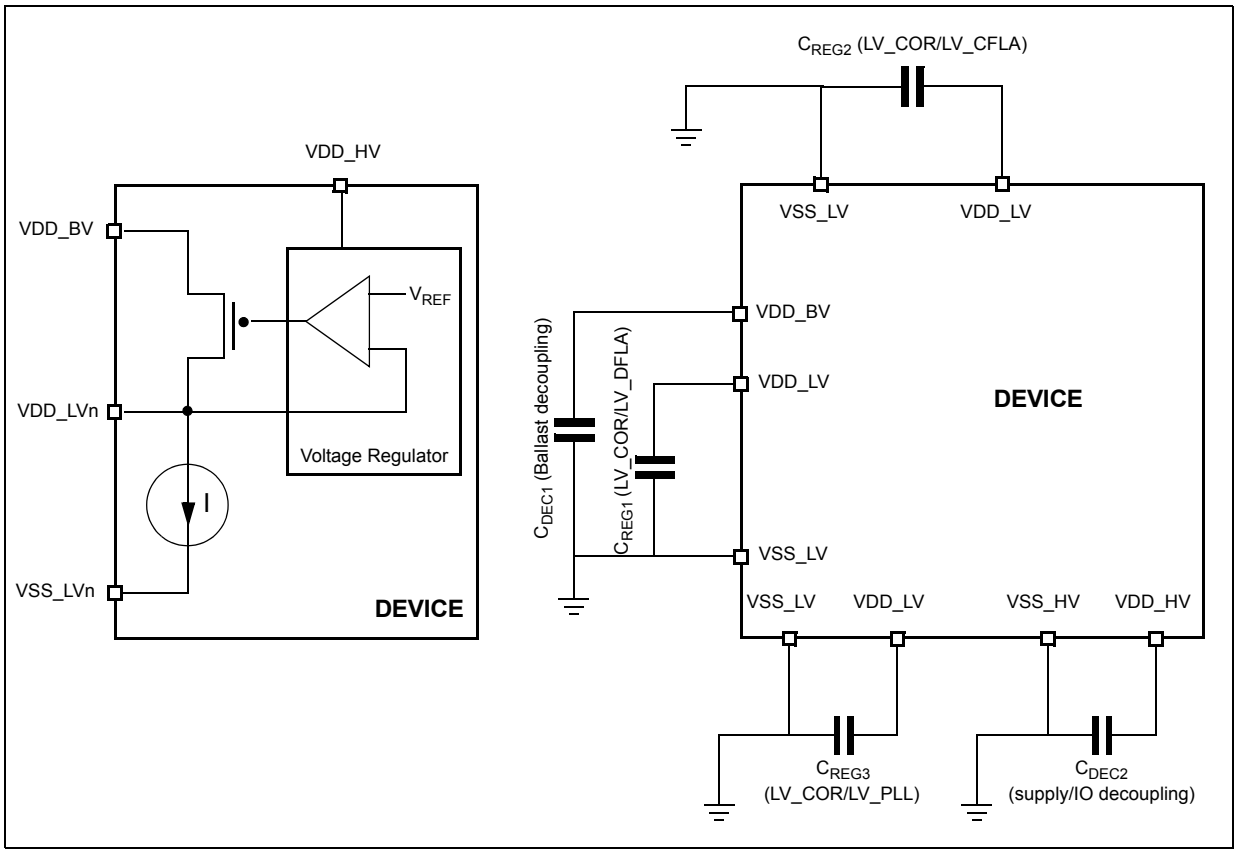

Figure 10. Voltage regulator capacitance connection

The internal voltage regulator requires external capacitance (C_{REGn}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 5 nH.

Each decoupling capacitor must be placed between each of the three V_{DD_LV}/V_{SS_LV} supply pairs to ensure stable voltage (see Section 3.13, Recommended operating conditions).

The internal voltage regulator requires a controlled slew rate of both V_{DD_HV} and V_{DD_BV} as described in Figure 11.

Table 26. Voltage regulator electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
$\left\|\frac{d}{dt}VDD(STDBY)\right\|$	SR	—	Maximum slope on V_{DD} during standby exit		—	—	15	mV/µs
V_{MREG}	CC	T	Main regulator output voltage	Before exiting from reset	—	1.32	—	V
		P		After trimming	1.16	1.28	—	
I_{MREG}	SR	—	Main regulator current provided to V_{DD_LV} domain	—	—	—	150	mA
$I_{MREGINT}$	CC	D	Main regulator module current consumption	I_{MREG} = 200 mA	—	—	2	mA
				I_{MREG} = 0 mA	—	—	1	
V_{LPREG}	CC	P	Low power regulator output voltage	After trimming	1.16	1.28	—	V
I_{LPREG}	SR	—	Low power regulator current provided to V_{DD_LV} domain	—	—	—	15	mA
$I_{LPREGINT}$	CC	D	Low power regulator module current consumption	I_{LPREG} = 15 mA; T_A = 55 °C	—	—	600	µA
		—		I_{LPREG} = 0 mA; T_A = 55 °C	—	5	—	
V_{ULPREG}	CC	P	Ultra low power regulator output voltage	After trimming	1.16	1.28	—	V
I_{ULPREG}	SR	—	Ultra low power regulator current provided to V_{DD_LV} domain	—	—	—	5	mA
$I_{ULPREGINT}$	CC	D	Ultra low power regulator module current consumption	I_{ULPREG} = 5 mA; T_A = 55 °C	—	—	100	µA
				I_{ULPREG} = 0 mA; T_A = 55 °C	—	2	—	
I_{DD_BV}	CC	D	In-rush average current on V_{DD_BV} during power-up[5]	—	—	—	300[6]	mA

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 This capacitance value is driven by the constraints of the external voltage regulator supplying the V_{DD_BV} voltage. A typical value is in the range of 470 nF.

3 This value is acceptable to guarantee operation from 4.5 V to 5.5 V

4 External regulator and capacitance circuitry must be capable of providing I_{DD_BV} while maintaining supply V_{DD_BV} in operating range.

5 In-rush average current is seen only for short time (maximum 20 µs) during power-up and on standby exit. It is dependant on the sum of the C_{REGn} capacitances.

6 The duration of the in-rush current depends on the capacitance placed on LV pins. BV decoupling capacitors must be sized accordingly. Refer to I_{MREG} value for minimum amount of current to be provided in cc.

The $|\Delta_{VDD(STDBY)}|$ and dVDD(STDBY)/dt system requirement can be used to define the component used for the V_{DD} supply generation. The following two examples describe how to calculate capacitance size:

6 Data Flash Power Down. Code Flash in Low Power. SIRC (128 kHz) and FIRC (16 MHz) on. 10 MHz XTAL clock. FlexCAN: instances: 0, 1, 2 ON (clocked but not reception or transmission), instances: 4, 5, 6 clock gated. LINFlex: instances: 0, 1, 2 ON (clocked but not reception or transmission), instance: 3 clock gated. eMIOS: instance: 0 ON (16 channels on PA[0]–PA[11] and PC[12]–PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication). RTC/API ON. PIT ON. STM ON. ADC ON but not conversion except 2 analog watchdog.

7 Only for the “P” classification: No clock, FIRC (16 MHz) off, SIRC (128 kHz) on, PLL off, HPvreg off, ULPVreg/LPVreg on. All possible peripherals off and clock gated. Flash in power down mode.

8 When going from RUN to STOP mode and the core consumption is > 6 mA, it is normal operation for the main regulator module to be kept on by the on-chip current monitoring circuit. This is most likely to occur with junction temperatures exceeding 125 °C and under these circumstances, it is possible for the current to initially exceed the maximum STOP specification by up to 2 mA. After entering stop, the application junction temperature will reduce to the ambient level and the main regulator will be automatically switched off when the load current is below 6 mA.

9 Only for the “P” classification: ULPreg on, HP/LPVreg off, 32 KB RAM on, device configured for minimum consumption, all possible modules switched off.

10 ULPreg on, HP/LPVreg off, 8 KB RAM on, device configured for minimum consumption, all possible modules switched off.

3.19 Flash memory electrical characteristics

3.19.1 Program/Erase characteristics

Table 29 shows the program and erase characteristics.

Table 29. Program and erase specifications

Symbol		C	Parameter	Value				Unit
				Min	Typ[1]	Initial max[2]	Max[3]	
$T_{dwprogram}$	CC	C	Double word (64 bits) program time[4]	—	22	50	500	µs
$T_{16Kpperase}$			16 KB block preprogram and erase time	—	300	500	5000	ms
$T_{32Kpperase}$			32 KB block preprogram and erase time	—	400	600	5000	ms
$T_{128Kpperase}$			128 KB block preprogram and erase time	—	800	1300	7500	ms
T_{esus}	CC	D	Erase suspend latency	—	—	30	30	µs

1 Typical program and erase times assume nominal supply values and operation at 25 °C.

2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3 The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

Table 30. Flash module life

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
P/E	CC	C	Number of program/erase cycles per block over the operating temperature range (T_J)	16 KB blocks	100,000	—	—	cycles
				32 KB blocks	10,000	100,000	—	
				128 KB blocks	1,000	100,000	—	
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature[1]	Blocks with 0–1,000 P/E cycles	20	—	—	years
				Blocks with 1,001–10,000 P/E cycles	10	—	—	
				Blocks with 10,001–100,000 P/E cycles	5	—	—	

1 Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 31. Flash read access timing

Symbol		C	Parameter	Conditions[1]	Max	Unit
f_{READ}	CC	P	Maximum frequency for Flash reading	2 wait states	64	MHz
		C		1 wait state	40	
		C		0 wait states	20	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

3.19.2 Flash power supply DC characteristics

Table 32 shows the power supply DC characteristics on external supply.

Table 32. Flash memory power supply DC electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
I_{FREAD}[2]	CC	D	Sum of the current consumption on VDD_HV and VDD_BV on read access	Code flash memory module read f_{CPU} = 64 MHz[3]	—	15	33	mA
				Data flash memory module read f_{CPU} = 64 MHz[3]	—	15	33	
I_{FMOD}[2]	CC	D	Sum of the current consumption on VDD_HV and VDD_BV on matrix modification (program/erase)	Program/Erase ongoing while reading code flash memory registers f_{CPU} = 64 MHz[3]	—	15	33	mA
				Program/Erase ongoing while reading data flash memory registers f_{CPU} = 64 MHz[3]	—	15	33	

Table 35. ESD absolute maximum ratings[1] [2]

Symbol		C	Ratings	Conditions	Class	Max value	Unit
$V_{ESD(HBM)}$	CC	T	Electrostatic discharge voltage (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(MM)}$	CC	T	Electrostatic discharge voltage (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	
$V_{ESD(CDM)}$	CC	T	Electrostatic discharge voltage (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500	
						750 (corners)	

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3.20.3.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 36. Latch-up results

Symbol		C	Parameter	Conditions	Class
LU	CC	T	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

3.21 Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

The device provides an oscillator/resonator driver. Figure 14 describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

Table 37 provides the parameter description of 4 MHz to 16 MHz crystals used for the design simulations.

2 This is the recommended range of load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground. It includes all the parasitics due to board traces, crystal and package.

3 Maximum ESR (R_m) of the crystal is 50 kΩ

4 C0 includes a parasitic capacitance of 2.0 pF between OSC32K_XTAL and OSC32K_EXTAL pins

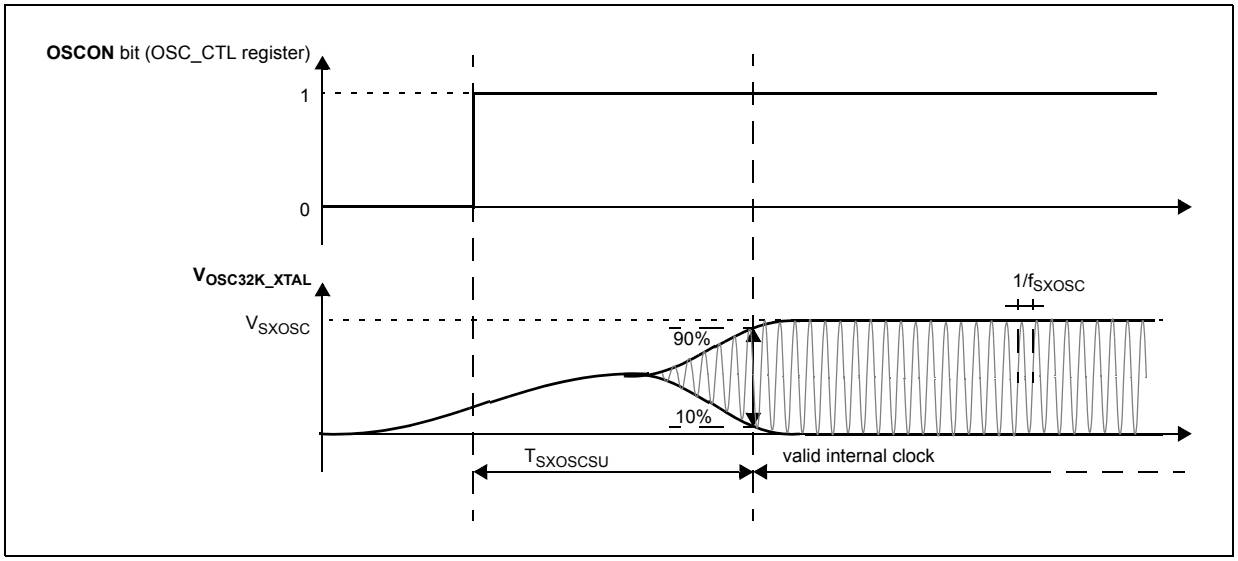

Figure 18. Slow external crystal oscillator (32 kHz) timing diagram

Table 40. Slow external crystal oscillator (32 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{SXOSC}	SR	—	Slow external crystal oscillator frequency	—	32	32.768	40	kHz
V_{SXOSC}	CC	T	Oscillation amplitude	—	—	2.1	—	V
$I_{SXOSCBIAS}$	CC	T	Oscillation bias current	—	—	2.5	—	µA
I_{SXOSC}	CC	T	Slow external crystal oscillator consumption	—	—	—	8	µA
$T_{SXOSCSU}$	CC	T	Slow external crystal oscillator start-up time	—	—	—	2[2]	s

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified. Values are specified for no neighbor GPIO pin activity. If oscillator is enabled (OSC32K_XTAL and OSC32K_EXTAL pins), neighboring pins should not toggle.

2 Start-up time has been measured with EPSON TOYOCOM MC306 crystal. Variation may be seen with other crystal.

3.23 FMPLL electrical characteristics

The device provides a frequency-modulated phase-locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.

possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: being C_S and C_{p2} substantially two switched capacitances, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S+C_{p2} equal to 3 pF, a resistance of 330 kΩ is obtained ($R_{EQ} = 1 / (f_c \times (C_S+C_{p2}))$, where f_c represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S+C_{p2}) and the sum of $R_S + R_F$, the external circuit must be designed to respect the Equation 4:

Eqn. 4

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 4 generates a constraint for external network design, in particular on a resistive path.

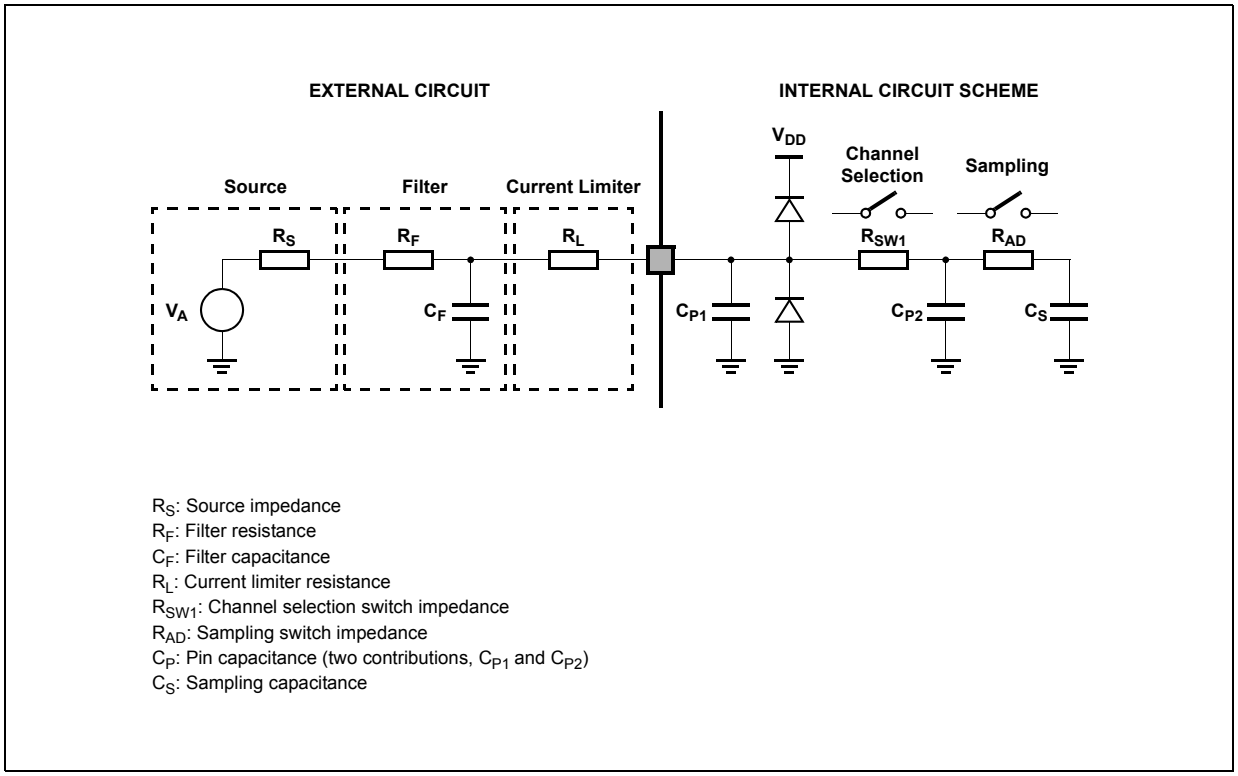

Figure 20. Input equivalent circuit (precise channels)

Table 47. DSPI characteristics[1] (continued)

No.	Symbol		C	Parameter		DSPI0/DSPI1			DSPI2			Unit
						Min	Typ	Max	Min	Typ	Max	
10	t_{HI}	SR	D	Data hold time for inputs	Master mode	0	—	—	0	—	—	ns
					Slave mode	2^6	—	—	2^6	—	—	
11	t_{SUO}[7]	CC	D	Data valid after SCK edge	Master mode	—	—	32	—	—	50	ns
					Slave mode	—	—	52	—	—	160	
12	t_{HO}[7]	CC	D	Data hold time for outputs	Master mode	0	—	—	0	—	—	ns
					Slave mode	8	—	—	13	—	—	

1 Operating conditions: C_L = 10 to 50 pF, $Slew_{IN}$ = 3.5 to 15 ns.

2 Maximum value is reached when CSn pad is configured as SLOW pad while SCK pad is configured as MEDIUM. A positive value means that SCK starts before CSn is asserted. DSPI2 has only SLOW SCK available.

3 Maximum value is reached when CSn pad is configured as MEDIUM pad while SCK pad is configured as SLOW. A positive value means that CSn is deasserted before SCK. DSPI0 and DSPI1 have only MEDIUM SCK available.

4 The t_{CSC} delay value is configurable through a register. When configuring t_{CSC} (using PCSSCK and CSSCK fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{CSC} to ensure positive t_{CSCext}.

5 The t_{ASC} delay value is configurable through a register. When configuring t_{ASC} (using PASC and ASC fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{ASC} to ensure positive t_{ASCext}.

6 This delay value corresponds to SMPL_PT = 00b which is bit field 9 and 8 of the DSPI_MCR.

7 SCK and SOUT configured as MEDIUM pad

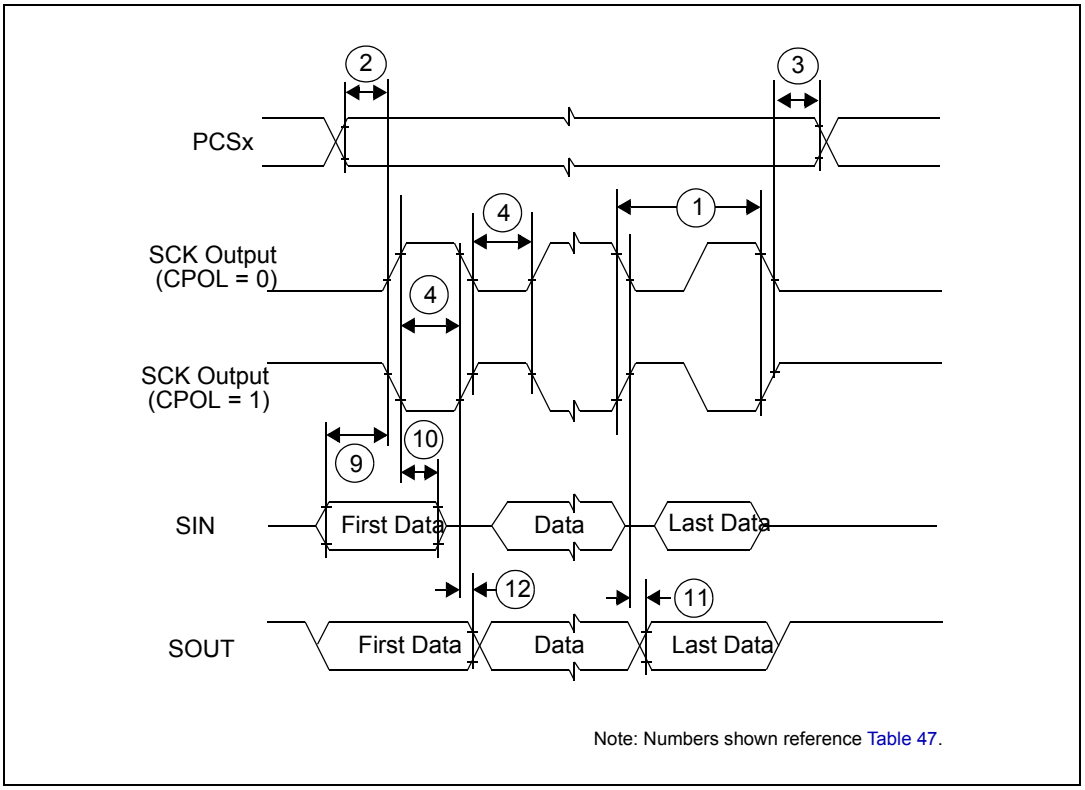

Figure 24. DSPI classic SPI timing – master, CPHA = 0

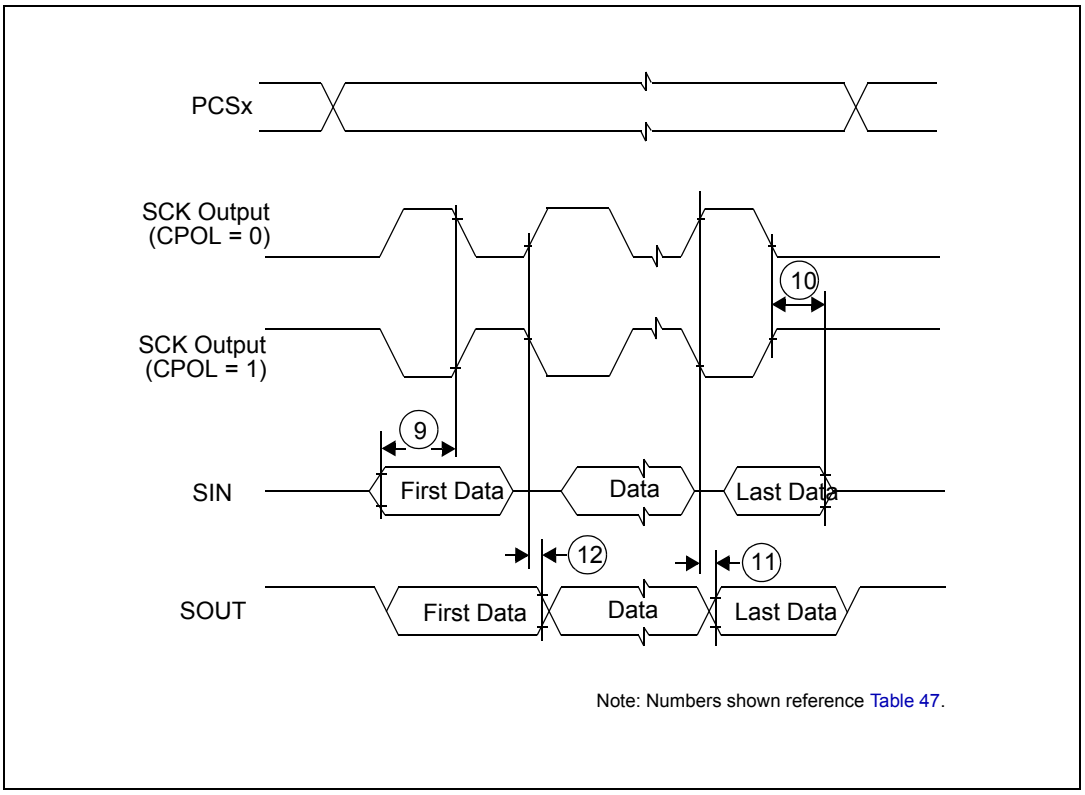

Figure 25. DSPI classic SPI timing – master, CPHA = 1

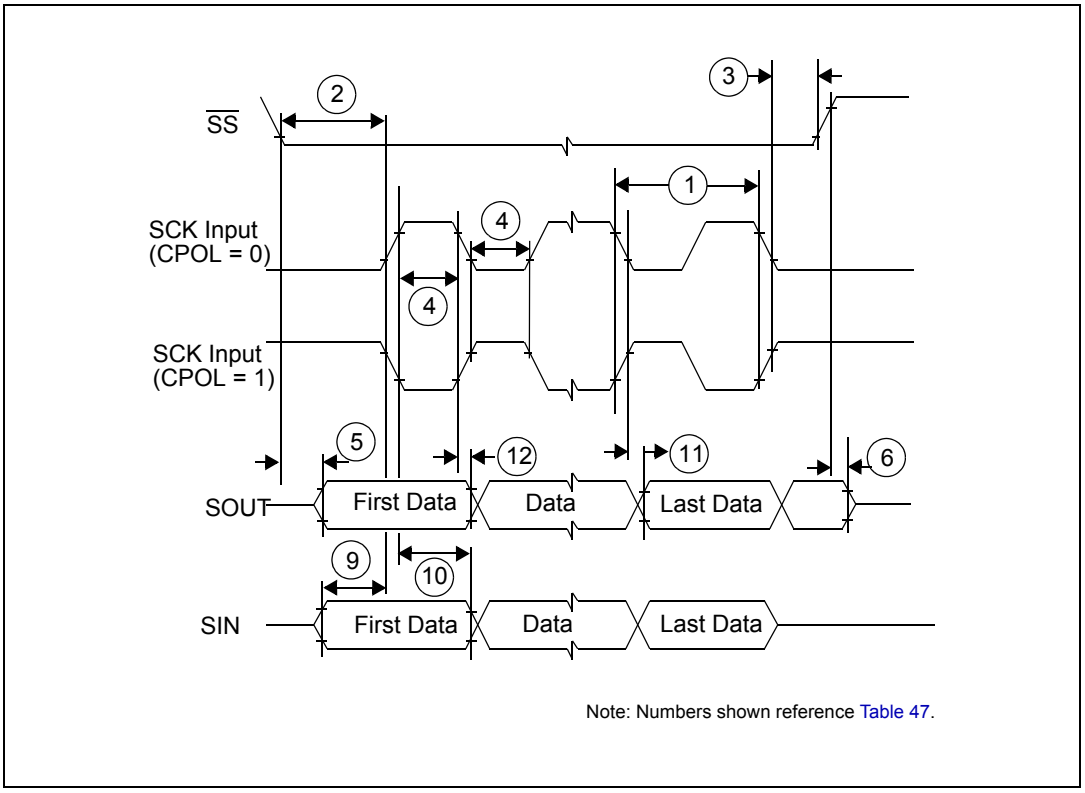

Figure 26. DSPI classic SPI timing – slave, CPHA = 0

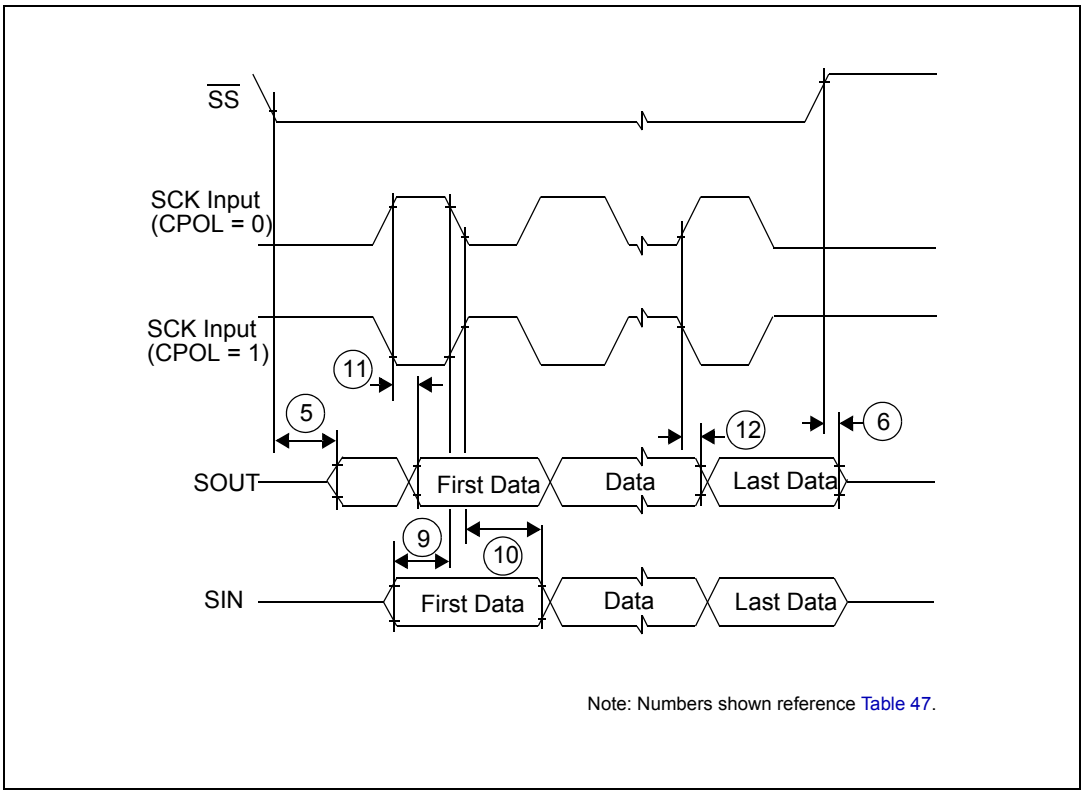

Figure 27. DSPI classic SPI timing – slave, CPHA = 1

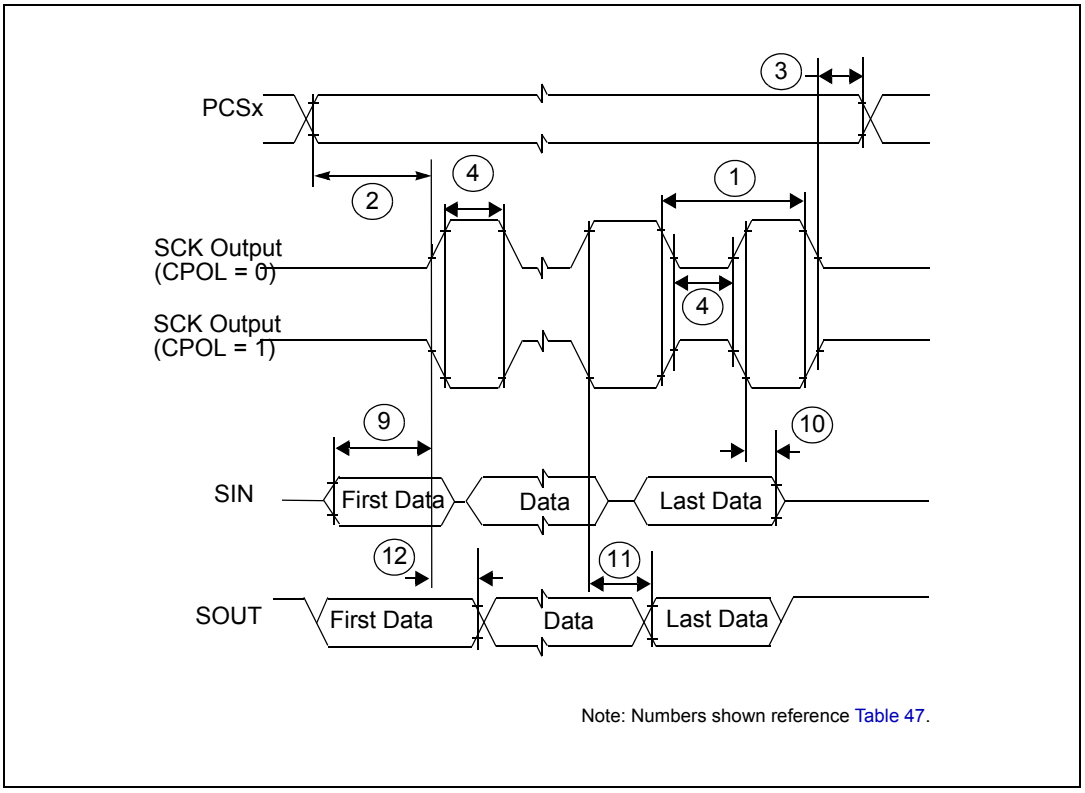

Figure 28. DSPI modified transfer format timing – master, CPHA = 0

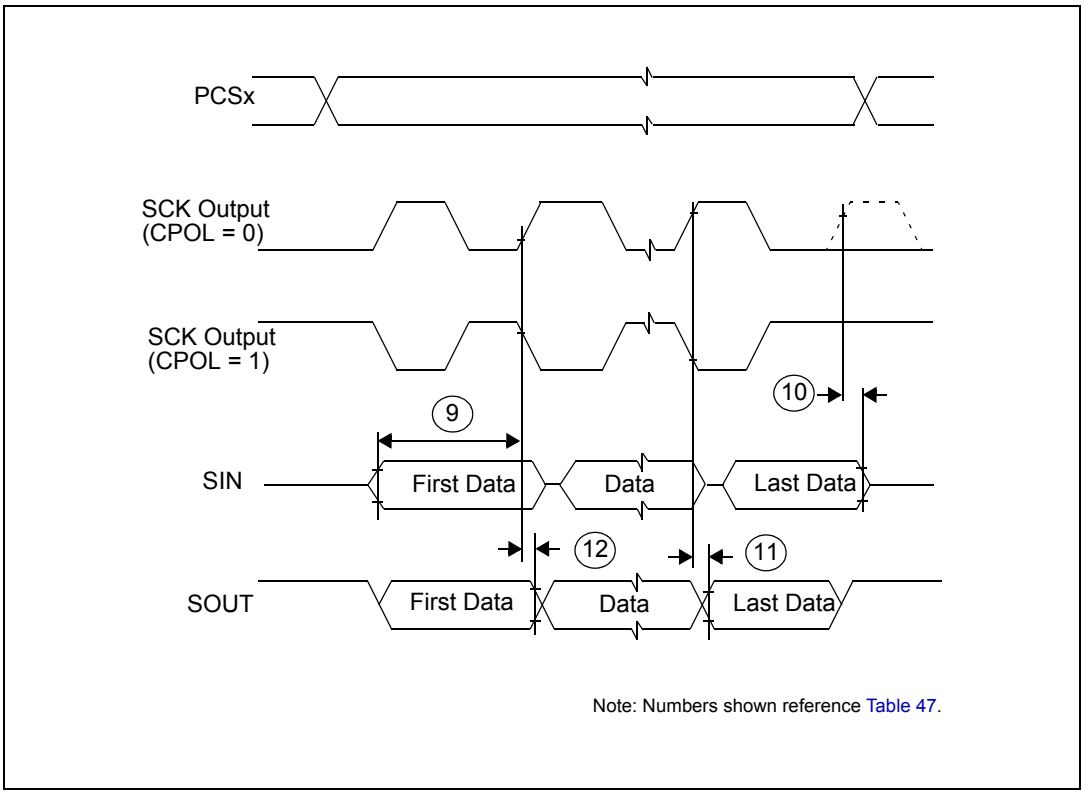

Figure 29. DSPI modified transfer format timing – master, CPHA = 1

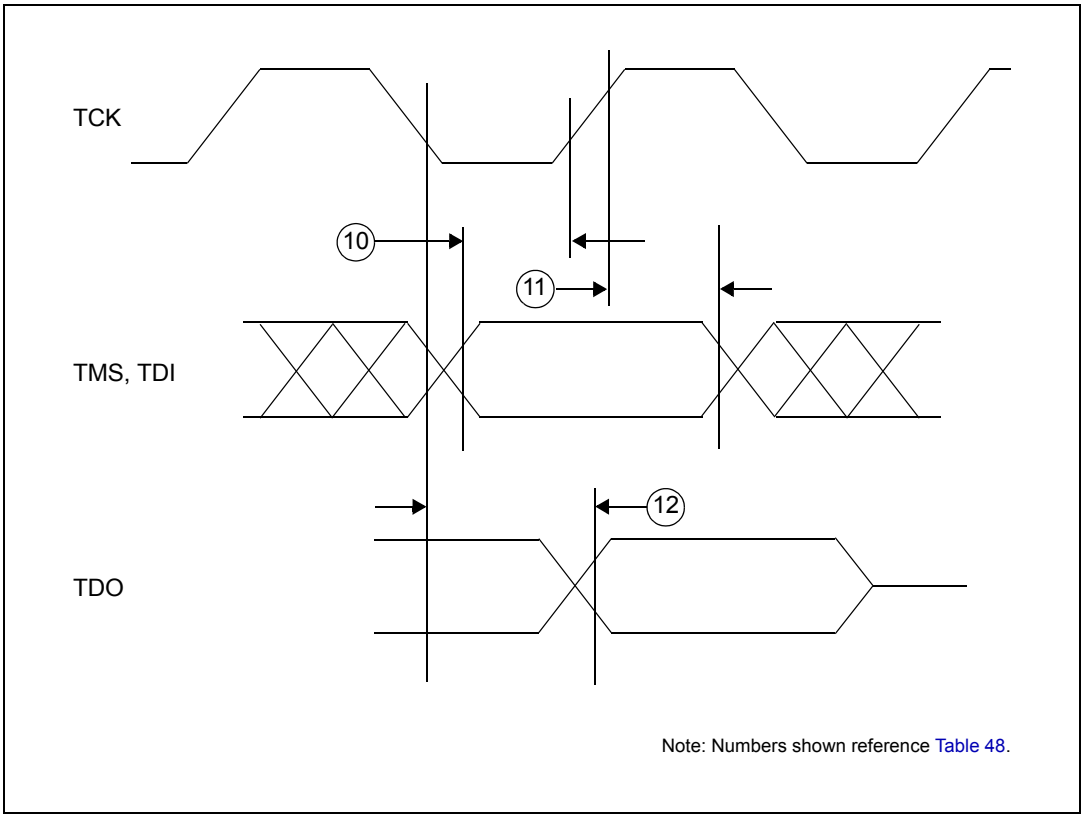

Figure 33. Nexus TDI, TMS, TDO timing

3.27.4 JTAG characteristics

Table 49. JTAG characteristics

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{JCYC}	CC	D	TCK cycle time	64	—	—	ns
2	t_{TDIS}	CC	D	TDI setup time	15	—	—	ns
3	t_{TDIH}	CC	D	TDI hold time	5	—	—	ns
4	t_{TMSS}	CC	D	TMS setup time	15	—	—	ns
5	t_{TMSH}	CC	D	TMS hold time	5	—	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO valid	—	—	33	ns
7	t_{TDOI}	CC	D	TCK low to TDO invalid	6	—	—	ns

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NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F–02	
	STANDARD: JEDEC MS–026 BCD	
	PACKAGE CODE: 8426	SHEET: 3

Figure 37. 64 LQFP package mechanical drawing (3 of 3)