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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I ² C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	79
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5604cf2mll6

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	PC[8]	PC[13]	NC	NC	PH[8]	PH[4]	PC[5]	PC[0]	NC	NC	PC[2]	NC	PE[15]	NC	NC	NC	A
B	PC[9]	PB[2]	NC	PC[12]	PE[6]	PH[5]	PC[4]	PH[9]	PH[10]	NC	PC[3]	PG[11]	PG[15]	PG[14]	PA[11]	PA[10]	B
C	PC[14]	VDD_HV	PB[3]	PE[7]	PH[7]	PE[5]	PE[3]	VSS_LV	PC[1]	NC	PA[5]	NC	PE[14]	PE[12]	PA[9]	PA[8]	C
D	NC	NC	PC[15]	NC	PH[6]	PE[4]	PE[2]	VDD_LV	VDD_HV	NC	PA[6]	NC	PG[10]	PF[14]	PE[13]	PA[7]	D
E	PG[4]	PG[5]	PG[3]	PG[2]									PG[1]	PG[0]	PF[15]	VDD_HV	E
F	PE[0]	PA[2]	PA[1]	PE[1]									PH[0]	PH[1]	PH[3]	PH[2]	F
G	PE[9]	PE[8]	PE[10]	PA[0]									VDD_HV	NC	NC	MSEO	G
H	VSS_HV	PE[11]	VDD_HV	NC									MDO3	MDO2	MDO0	MDO1	H
J	RESET	VSS_LV	NC	NC									NC	NC	NC	NC	J
K	EVTI	NC	VDD_BV	VDD_LV									NC	PG[12]	PA[3]	PG[13]	K
L	PG[9]	PG[8]	NC	EVTO									PB[15]	PD[15]	PD[14]	PB[14]	L
M	PG[7]	PG[6]	PC[10]	PC[11]									PB[13]	PD[13]	PD[12]	PB[12]	M
N	PB[1]	PF[9]	PB[0]	NC	NC	PA[4]	VSS_LV	EXTAL	VDD_HV	PF[0]	PF[4]	NC	PB[11]	PD[10]	PD[9]	PD[11]	N
P	PF[8]	NC	PC[7]	NC	NC	PA[14]	VDD_LV	XTAL	PB[10]	PF[1]	PF[5]	PD[0]	PD[3]	VDD_HV_ADC	PB[6]	PB[7]	P
R	PF[12]	PC[6]	PF[10]	PF[11]	VDD_HV	PA[15]	PA[13]	NC	OSC32K_XTAL	PF[3]	PF[7]	PD[2]	PD[4]	PD[7]	VSS_HV_ADC	PB[5]	R
T	NC	NC	NC	MCKO	NC	PF[13]	PA[12]	NC	OSC32K_EXTAL	PF[2]	PF[6]	PD[1]	PD[5]	PD[6]	PD[8]	PB[4]	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Note: 208 MAPBGA available only as development package for Nexus 2+.

NC = Not connected

Figure 6. 208 MAPBGA configuration

3.2 Pad configuration during reset phases

All pads have a fixed configuration under reset.

During the power-up phase, all pads are forced to tristate.

After power-up phase, all pads are forced to tristate with the following exceptions:

- PA[9] (FAB) is pull-down. Without external strong pull-up the device starts fetching from flash.
- PA[8] (ABS[0]) is pull-up.
- RESET pad is driven low. This is pull-up only after PHASE2 reset completion.
- JTAG pads (TCK, TMS and TDI) are pull-up whilst TDO remains tristate.
- Precise ADC pads (PB[7:4] and PD[11:0]) are left tristate (no output buffer available).
- Main oscillator pads (EXTAL, XTAL) are tristate.
- Nexus output pads (MDO[n], MCKO, EVTO, MSEO) are forced to output.

3.5 System pins

The system pins are listed in [Table 5](#).

Table 5. System pin descriptions

System pin	Function	I/O direction	Pad type	RESET configuration	Pin number			
					64 LQFP ¹	100 LQFP	144 LQFP	208 MAPBGA ²
RESET	Bidirectional reset with Schmitt-Trigger characteristics and noise filter.	I/O	M	Input, weak pull-up only after PHASE2	9	17	21	J1
EXTAL	Analog output of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode. ³	I/O	X	Tristate	27	36	50	N8
XTAL	Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator is used in bypass mode. ³	I	X	Tristate	25	34	48	P8

¹ Pin numbers apply to both the MPC560xB and MPC560xC packages.

² 208 MAPBGA available only as development package for Nexus2+

³ See the relevant section of the datasheet

3.6 Functional ports

The functional port pins are listed in [Table 6](#).

Table 6. Functional port pin descriptions

Port pin	PCR	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA ³
PA[0]	PCR[0]	AF0 AF1 AF2 AF3 —	GPIO[0] E0UC[0] CLKOUT — WKPU[19] ⁴	SIUL eMIOS_0 CGL — WKPU	I/O I/O O — I	M	Tristate	5	5	12	16	G4
PA[1]	PCR[1]	AF0 AF1 AF2 AF3 — —	GPIO[1] E0UC[1] — — NMI ⁵ WKPU[2] ⁴	SIUL eMIOS_0 — — WKPU WKPU	I/O I/O — — I I	S	Tristate	4	4	7	11	F3

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA ³
PA[10]	PCR[10]	AF0 AF1 AF2 AF3	GPIO[10] E0UC[10] SDA —	SIUL eMIOS_0 I2C_0 —	I/O I/O I/O —	S	Tristate	47	47	74	107	B16
PA[11]	PCR[11]	AF0 AF1 AF2 AF3	GPIO[11] E0UC[11] SCL —	SIUL eMIOS_0 I2C_0 —	I/O I/O I/O —	S	Tristate	48	48	75	108	B15
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 —	GPIO[12] — — — SIN_0	SIUL — — — DSPI0	I/O — — — I	S	Tristate	22	22	31	45	T7
PA[13]	PCR[13]	AF0 AF1 AF2 AF3	GPIO[13] SOUT_0 — —	SIUL DSPI_0 — —	I/O O — —	M	Tristate	21	21	30	44	R7
PA[14]	PCR[14]	AF0 AF1 AF2 AF3 —	GPIO[14] SCK_0 CS0_0 — EIRQ[4]	SIUL DSPI_0 DSPI_0 — SIUL	I/O I/O I/O — I	M	Tristate	19	19	28	42	P6
PA[15]	PCR[15]	AF0 AF1 AF2 AF3 —	GPIO[15] CS0_0 SCK_0 — WKPU[10] ⁴	SIUL DSPI_0 DSPI_0 — WKPU	I/O I/O I/O — I	M	Tristate	18	18	27	40	R6
PB[0]	PCR[16]	AF0 AF1 AF2 AF3	GPIO[16] CAN0TX — —	SIUL FlexCAN_0 — —	I/O O — —	M	Tristate	14	14	23	31	N3
PB[1]	PCR[17]	AF0 AF1 AF2 AF3 — —	GPIO[17] — — — WKPU[4] ⁴ CAN0RX	SIUL — — — WKPU FlexCAN_0	I/O — — — I I	S	Tristate	15	15	24	32	N1
PB[2]	PCR[18]	AF0 AF1 AF2 AF3	GPIO[18] LIN0TX SDA —	SIUL LINFlex_0 I2C_0 —	I/O O I/O —	M	Tristate	64	64	100	144	B2

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA ³
PB[3]	PCR[19]	AF0 AF1 AF2 AF3 — —	GPIO[19] — SCL — WKPU[11] ⁴ LIN0RX	SIUL — I2C_0 — WKPU LINFlex_0	I/O — I/O — I I	S	Tristate	1	1	1	1	C3
PB[4]	PCR[20]	AF0 AF1 AF2 AF3 —	GPIO[20] — — — GPIO[0]	SIUL — — — ADC	I — — — I	I	Tristate	32	32	50	72	T16
PB[5]	PCR[21]	AF0 AF1 AF2 AF3 —	GPIO[21] — — — GPIO[1]	SIUL — — — ADC	I — — — I	I	Tristate	35	—	53	75	R16
PB[6]	PCR[22]	AF0 AF1 AF2 AF3 —	GPIO[22] — — — GPIO[2]	SIUL — — — ADC	I — — — I	I	Tristate	36	—	54	76	P15
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 —	GPIO[23] — — — GPIO[3]	SIUL — — — ADC	I — — — I	I	Tristate	37	35	55	77	P16
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 — —	GPIO[24] — — — ANS[0] OSC32K_XTAL ⁷	SIUL — — — ADC SXOSC	I — — — I I/O	I	Tristate	30	30	39	53	R9
PB[9]	PCR[25]	AF0 AF1 AF2 AF3 — —	GPIO[25] — — — ANS[1] OSC32K_EXTAL ⁷	SIUL — — — ADC SXOSC	I — — — I I/O	I	Tristate	29	29	38	52	T9

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA ³
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — —	GPIO[26] — — — ANS[2] WKPU[8] ⁴	SIUL — — — ADC WKPU	I/O — — — I I	J	Tristate	31	31	40	54	P9
PB[11] ⁸	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ANS[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — I/O I	J	Tristate	38	36	59	81	N13
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ANX[0]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	39	—	61	83	M16
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ANX[1]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	40	—	63	85	M13
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ANX[2]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	41	37	65	87	L16
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ANX[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	42	38	67	89	L13
PC[0] ⁹	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M	Input, weak pull-up	59	59	87	126	A8
PC[1] ⁹	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO ¹⁰ —	SIUL — JTAGC —	I/O — O —	M	Tristate	54	54	82	121	C9

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA ³
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — — — LIN2RX WKPU[13] ⁴	SIUL — — — LINFlex_2 WKPU	I/O — — — I I	S	Tristate	2	2	2	2	B1
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] CAN1TX CAN4TX ¹¹ MA[1]	SIUL FlexCAN_1 FlexCAN_4 ADC	I/O O O O	M	Tristate	13	13	22	28	M3
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — — — CAN1RX CAN4RX ¹¹ WKPU[5] ⁴	SIUL — — — FlexCAN_1 FlexCAN_4 WKPU	I/O — — — I I I	S	Tristate	—	—	21	27	M4
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 —	GPIO[44] E0UC[12] — — SIN_2	SIUL eMIOS_0 — — DSPI_2	I/O I/O — — I	M	Tristate	—	—	97	141	B4
PC[13]	PCR[45]	AF0 AF1 AF2 AF3	GPIO[45] E0UC[13] SOUT_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O O —	S	Tristate	—	—	98	142	A2
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 —	GPIO[46] E0UC[14] SCK_2 — EIRQ[8]	SIUL eMIOS_0 DSPI_2 — SIUL	I/O I/O I/O — I	S	Tristate	—	—	3	3	C1
PC[15]	PCR[47]	AF0 AF1 AF2 AF3	GPIO[47] E0UC[15] CS0_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O I/O —	M	Tristate	—	—	4	4	D3
PD[0]	PCR[48]	AF0 AF1 AF2 AF3 —	GPIO[48] — — — GPI[4]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	41	63	P12

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ¹	Function	Peripheral	I/O direction ²	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA ³
PD[9]	PCR[57]	AF0 AF1 AF2 AF3 —	GPIO[57] — — — GPIO[13]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	56	78	N15
PD[10]	PCR[58]	AF0 AF1 AF2 AF3 —	GPIO[58] — — — GPIO[14]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	57	79	N14
PD[11]	PCR[59]	AF0 AF1 AF2 AF3 —	GPIO[59] — — — GPIO[15]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	58	80	N16
PD[12] ⁸	PCR[60]	AF0 AF1 AF2 AF3 —	GPIO[60] CS5_0 E0UC[24] — ANS[4]	SIUL DSPI_0 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	—	60	82	M15
PD[13]	PCR[61]	AF0 AF1 AF2 AF3 —	GPIO[61] CS0_1 E0UC[25] — ANS[5]	SIUL DSPI_1 eMIOS_0 — ADC	I/O I/O I/O — I	J	Tristate	—	—	62	84	M14
PD[14]	PCR[62]	AF0 AF1 AF2 AF3 —	GPIO[62] CS1_1 E0UC[26] — ANS[6]	SIUL DSPI_1 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	—	64	86	L15
PD[15]	PCR[63]	AF0 AF1 AF2 AF3 —	GPIO[63] CS2_1 E0UC[27] — ANS[7]	SIUL DSPI_1 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	—	66	88	L14
PE[0]	PCR[64]	AF0 AF1 AF2 AF3 — —	GPIO[64] E0UC[16] — — CAN5RX ¹¹ WKPU[6] ⁴	SIUL eMIOS_0 — — FlexCAN_5 WKPU	I/O I/O — — I I	S	Tristate	—	—	6	10	F1

Package pinouts and signal descriptions

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid applying any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

3.10 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in [Table 8](#) are used and the parameters are tagged accordingly in the tables where appropriate.

Table 8. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.11 NVUSRO register

Bit values in the Non-Volatile User Options (NVUSRO) Register control portions of the device configuration, namely electrical parameters such as high voltage supply and oscillator margin, as well as digital functionality (watchdog enable/disable after reset).

For a detailed description of the NVUSRO register, please refer to the device reference manual.

3.11.1 NVUSRO[PAD3V5V] field description

The DC electrical characteristics are dependent on the PAD3V5V bit value. [Table 9](#) shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 9. PAD3V5V field description

Value ¹	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

3.12 Absolute maximum ratings

Table 12. Absolute maximum ratings

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V _{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V _{DD}	SR	Voltage on VDD_HV pins with respect to ground (V _{SS})	—	−0.3	6.0	V
V _{SS_LV}	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V _{SS})	—	V _{SS} −0.1	V _{SS} +0.1	V
V _{DD_BV}	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V _{SS})	—	−0.3	6.0	V
			Relative to V _{DD}	−0.3	V _{DD} +0.3	
V _{SS_ADC}	SR	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V _{SS})	—	V _{SS} −0.1	V _{SS} +0.1	V
V _{DD_ADC}	SR	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V _{SS})	—	−0.3	6.0	V
			Relative to V _{DD}	V _{DD} −0.3	V _{DD} +0.3	
V _{IN}	SR	Voltage on any GPIO pin with respect to ground (V _{SS})	—	−0.3	6.0	V
			Relative to V _{DD}	—	V _{DD} +0.3	
I _{INJPAD}	SR	Injected input current on any pin during overload condition	—	−10	10	mA
I _{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	−50	50	
I _{AVGSEG}	SR	Sum of all the static I/O current within a supply segment	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	70	mA
			V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	64	
I _{CORELV}	SR	Low voltage static current sink through VDD_BV	—	—	150	mA
T _{STORAGE}	SR	Storage temperature	—	−55	150	°C

NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

Table 14. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V _{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V _{DD} ¹	SR	Voltage on VDD_HV pins with respect to ground (V _{SS})	—	4.5	5.5	V
			Voltage drop ²	3.0	5.5	
V _{SS_LV} ³	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V _{SS})	—	V _{SS} -0.1	V _{SS} +0.1	V
V _{DD_BV} ⁴	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V _{SS})	—	4.5	5.5	V
			Voltage drop ²	3.0	5.5	
			Relative to V _{DD}	V _{DD} -0.1	V _{DD} +0.1	
V _{SS_ADC}	SR	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V _{SS})	—	V _{SS} -0.1	V _{SS} +0.1	V
V _{DD_ADC} ⁵	SR	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V _{SS})	—	4.5	5.5	V
			Voltage drop ²	3.0	5.5	
			Relative to V _{DD}	V _{DD} -0.1	V _{DD} +0.1	
V _{IN}	SR	Voltage on any GPIO pin with respect to ground (V _{SS})	—	V _{SS} -0.1	—	V
			Relative to V _{DD}	—	V _{DD} +0.1	
I _{INJPAD}	SR	Injected input current on any pin during overload condition	—	-5	5	mA
I _{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	-50	50	
TV _{DD}	SR	V _{DD} slope to ensure correct power up ⁶	—	—	0.25	V/μs
T _A C-Grade Part	SR	Ambient temperature under bias	f _{CPU} ≤ 64 MHz	-40	85	°C
T _J C-Grade Part	SR	Junction temperature under bias		-40	110	
T _A V-Grade Part	SR	Ambient temperature under bias		-40	105	
T _J V-Grade Part	SR	Junction temperature under bias		-40	130	
T _A M-Grade Part	SR	Ambient temperature under bias		-40	125	
T _J M-Grade Part	SR	Junction temperature under bias		-40	150	

¹ 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.

² Full device operation is guaranteed by design when the voltage drops below 4.5 V down to 3.0 V. However, certain analog electrical characteristics will not be guaranteed to stay within the stated limits.

³ 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.

⁴ 100 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics).

⁵ 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.

⁶ Guaranteed by device validation

NOTE

RAM data retention is guaranteed with V_{DD_LV} not below 1.08 V.

Table 24. I/O weight¹ (continued)

Supply segment			Pad	144/100 LQFP				64 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
144 LQFP	100 LQFP	64 LQFP ²		SRC ³ = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
4	—	—	PG[2]	8%	12%	10%	10%	—	—	—	—
	4	3	PA[2]	8%	—	9%	—	8%	—	9%	—
		—	PE[0]	8%	—	9%	—	—	—	—	—
		3	PA[1]	7%	—	9%	—	7%	—	9%	—
		—	PE[1]	7%	10%	8%	9%	—	—	—	—
		—	PE[8]	7%	9%	8%	8%	—	—	—	—
		—	PE[9]	6%	—	7%	—	—	—	—	—
		—	PE[10]	6%	—	7%	—	—	—	—	—
		3	PA[0]	5%	8%	6%	7%	5%	8%	6%	7%
		—	PE[11]	5%	—	6%	—	—	—	—	—
1	—	—	PG[9]	9%	—	10%	—	—	—	—	—
	—	—	PG[8]	9%	—	11%	—	—	—	—	—
	1	—	PC[11]	9%	—	11%	—	—	—	—	—
		1	PC[10]	9%	13%	11%	12%	9%	13%	11%	12%
	—	—	PG[7]	10%	14%	11%	12%	—	—	—	—
	—	—	PG[6]	10%	14%	12%	12%	—	—	—	—
	1	1	PB[0]	10%	14%	12%	12%	10%	14%	12%	12%
			PB[1]	10%	—	12%	—	10%	—	12%	—
	—	—	PF[9]	10%	—	12%	—	—	—	—	—
	—	—	PF[8]	10%	15%	12%	13%	—	—	—	—
	—	—	PF[12]	10%	15%	12%	13%	—	—	—	—
	1	1	PC[6]	10%	—	12%	—	10%	—	12%	—
			PC[7]	10%	—	12%	—	10%	—	12%	—
	—	—	PF[10]	10%	14%	12%	12%	—	—	—	—
	—	—	PF[11]	10%	—	11%	—	—	—	—	—
	1	1	PA[15]	9%	12%	10%	11%	9%	12%	10%	11%
	—	—	PF[13]	8%	—	10%	—	—	—	—	—
	1	1	PA[14]	8%	11%	9%	10%	8%	11%	9%	10%
			PA[4]	8%	—	9%	—	8%	—	9%	—
			PA[13]	7%	10%	9%	9%	7%	10%	9%	9%
			PA[12]	7%	—	8%	—	7%	—	8%	—

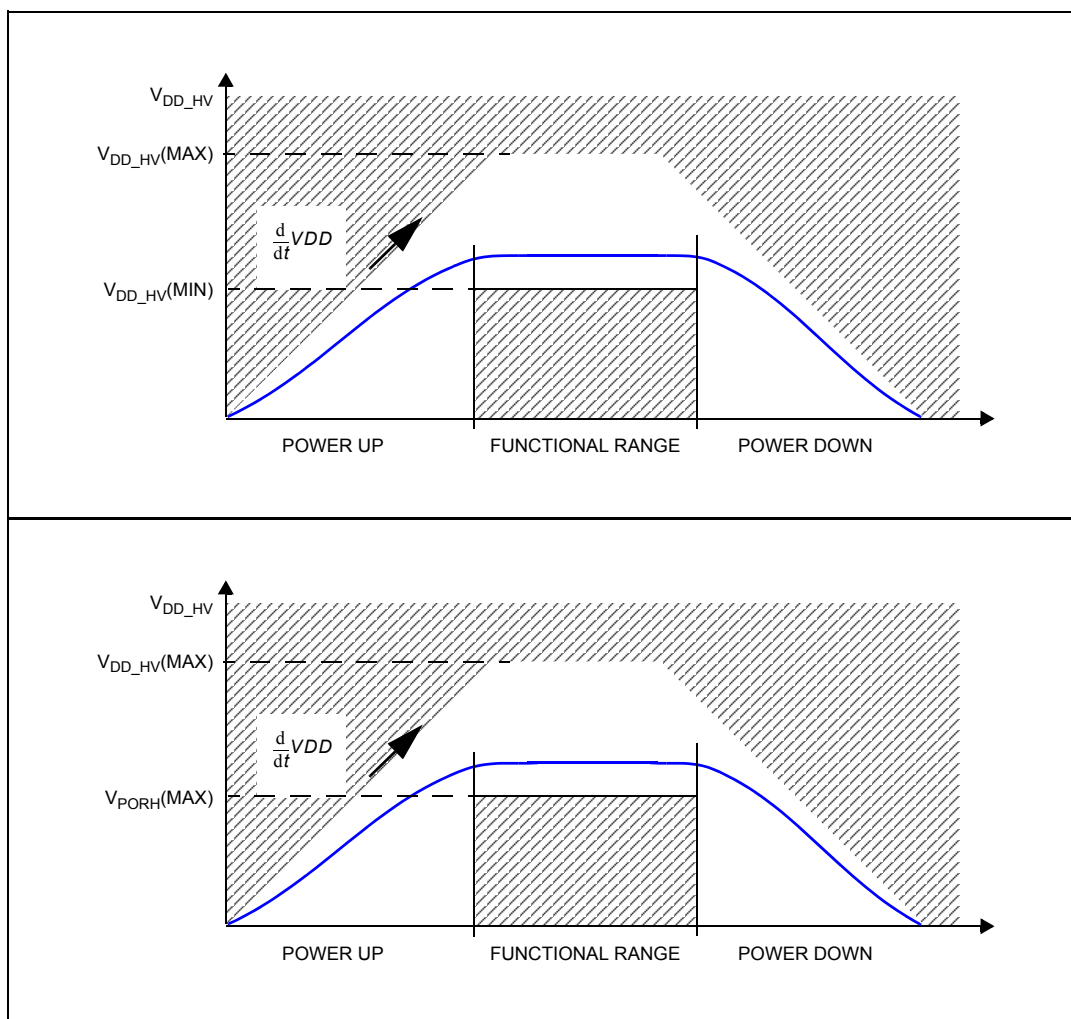


Figure 11. V_{DD_HV} and V_{DD_BV} maximum slope

When STANDBY mode is used, further constraints are applied to the both V_{DD_HV} and V_{DD_BV} in order to guarantee correct regulator function during STANDBY exit. This is described on [Figure 12](#).

STANDBY regulator constraints should normally be guaranteed by implementing equivalent of CSTDBY capacitance on application board (capacitance and ESR typical values), but would actually depend on exact characteristics of application external regulator.

3.26 ADC electrical characteristics

3.26.1 Introduction

The device provides a 10-bit Successive Approximation Register (SAR) analog-to-digital converter.

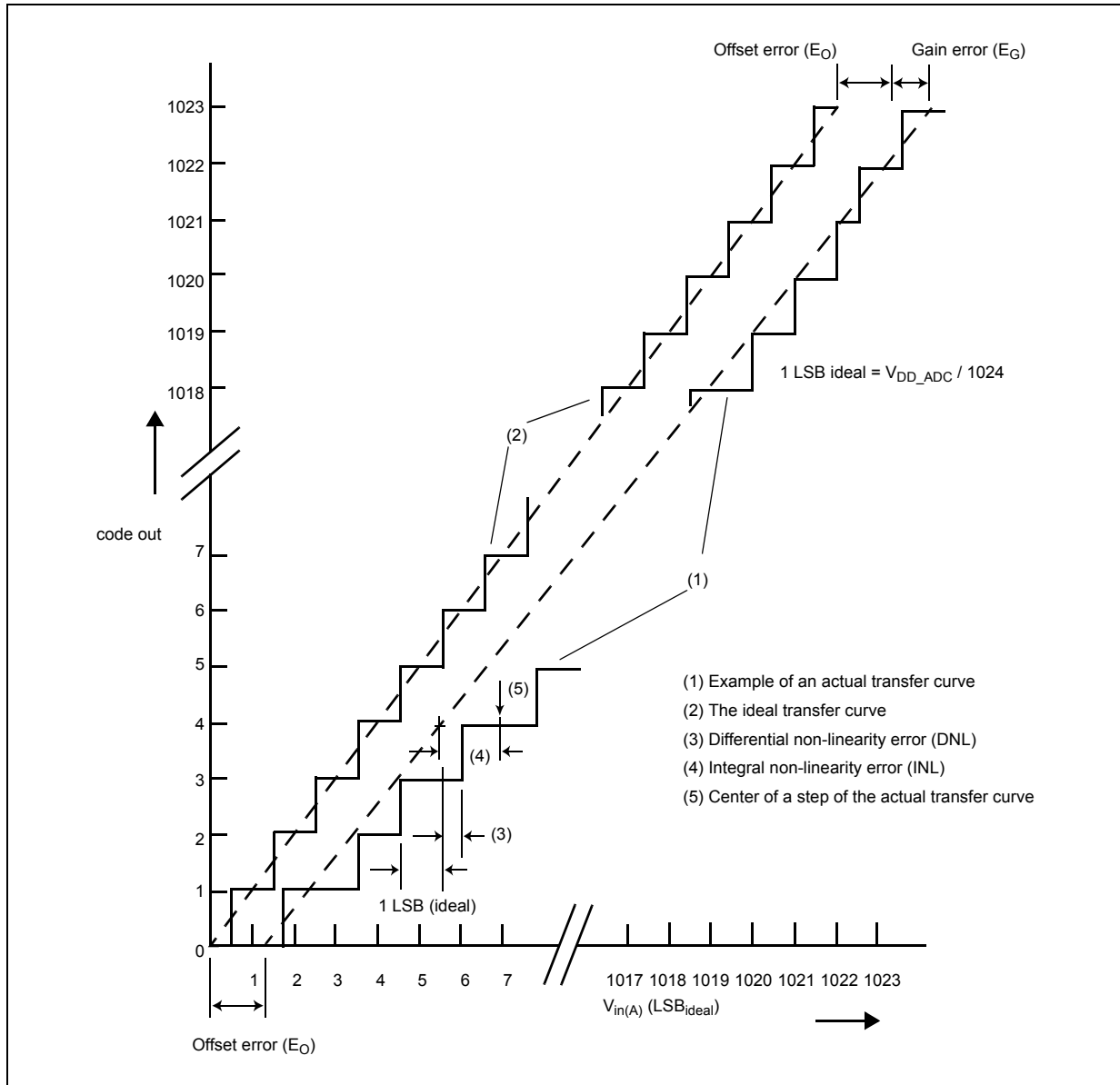


Figure 19. ADC characteristic and error definitions

3.26.2 Input impedance and ADC accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as

1. A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Eqn. 5

$$\tau_1 = (R_{SW} + R_{AD}) \cdot \frac{C_P \cdot C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time t_s is always much longer than the internal time constant:

Eqn. 6

$$\tau_1 < (R_{SW} + R_{AD}) \cdot C_S \ll t_s$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S , determining a new value of the voltage V_{A1} on the capacitance according to Equation 7:

Eqn. 7

$$V_{A1} \cdot (C_S + C_{P1} + C_{P2}) = V_A \cdot (C_{P1} + C_{P2})$$

2. A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L : again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Eqn. 8

$$\tau_2 < R_L \cdot (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time t_s , a constraints on R_L sizing is obtained:

Eqn. 9

$$8.5 \cdot \tau_2 = 8.5 \cdot R_L \cdot (C_S + C_{P1} + C_{P2}) < t_s$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1} , C_{P2} and C_S , then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1} . Equation 10 must be respected (charge balance assuming now C_S already charged at V_{A1}):

Eqn. 10

$$V_{A2} \cdot (C_S + C_{P1} + C_{P2} + C_F) = V_A \cdot C_F + V_{A1} \cdot (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A ; the time constant $R_F C_F$ of the filter is very high with respect to the sampling time (t_s). The filter is typically designed to act as anti-aliasing.

Table 47. DSPI characteristics¹ (continued)

No.	Symbol		C	Parameter		DSPI0/DSPI1			DSPI2			Unit
						Min	Typ	Max	Min	Typ	Max	
10	t _{HI}	SR	D	Data hold time for inputs	Master mode	0	—	—	0	—	—	ns
					Slave mode	2 ⁶	—	—	2 ⁶	—	—	
11	t _{SUO} ⁷	CC	D	Data valid after SCK edge	Master mode	—	—	32	—	—	50	ns
					Slave mode	—	—	52	—	—	160	
12	t _{HO} ⁷	CC	D	Data hold time for outputs	Master mode	0	—	—	0	—	—	ns
					Slave mode	8	—	—	13	—	—	

¹ Operating conditions: $C_L = 10$ to 50 pF, $Slew_{IN} = 3.5$ to 15 ns.

² Maximum value is reached when CSn pad is configured as SLOW pad while SCK pad is configured as MEDIUM. A positive value means that SCK starts before CSn is asserted. DSPI2 has only SLOW SCK available.

³ Maximum value is reached when CSn pad is configured as MEDIUM pad while SCK pad is configured as SLOW. A positive value means that CSn is deasserted before SCK. DSPI0 and DSPI1 have only MEDIUM SCK available.

⁴ The t_{CSC} delay value is configurable through a register. When configuring t_{CSC} (using PCSSCK and CSSCK fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{CSC} to ensure positive t_{CSCext} .

⁵ The t_{ASC} delay value is configurable through a register. When configuring t_{ASC} (using PASC and ASC fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{ASC} to ensure positive t_{ASCext} .

⁶ This delay value corresponds to SMPL_PT = 00b which is bit field 9 and 8 of the DSPI_MCR.

⁷ SCK and SOUT configured as MEDIUM pad

4.1.2 100 LQFP

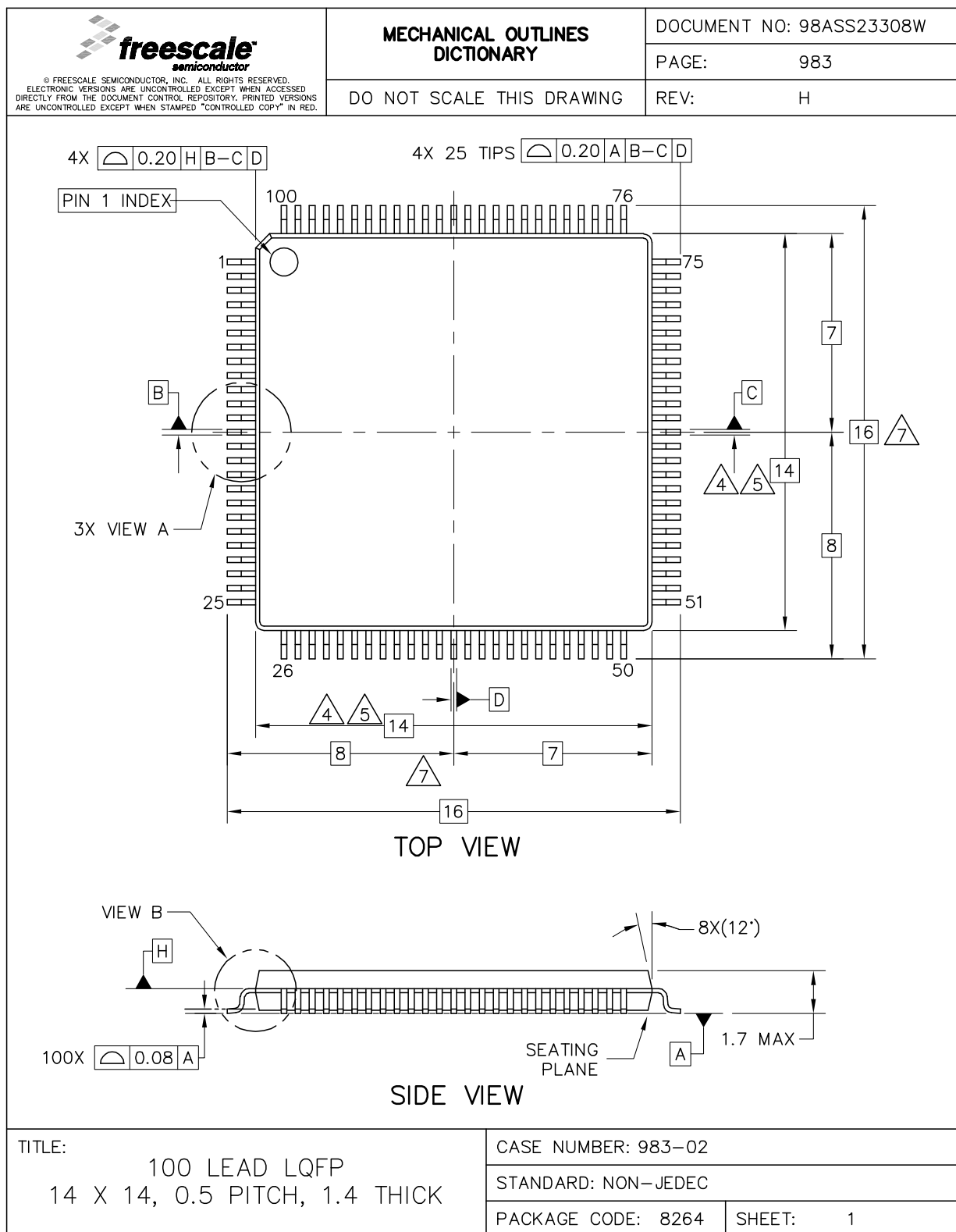


Figure 38. 100 LQFP package mechanical drawing (1 of 3)

Table 50. Revision history (continued)

Revision	Date	Description of Changes
4	06-Aug-2009	<p>Updated Figure 6</p> <p>Table 12</p> <ul style="list-style-type: none"> • V_{DD_ADC}: changed min value for “relative to V_{DD}” condition • V_{IN}: changed min value for “relative to V_{DD}” condition • I_{CORELV}: added new row <p>Table 14</p> <ul style="list-style-type: none"> • $T_{A\ C-Grade\ Part}$, $T_{J\ C-Grade\ Part}$, $T_{A\ V-Grade\ Part}$, $T_{J\ V-Grade\ Part}$, $T_{A\ M-Grade\ Part}$, $T_{J\ M-Grade\ Part}$: added new rows • Changed capacitance value in footnote <p>Table 21</p> <ul style="list-style-type: none"> • MEDIUM configuration: added condition for $PAD3V5V = 0$ <p>Updated Figure 10</p> <p>Table 26</p> <ul style="list-style-type: none"> • C_{DEC1}: changed min value • I_{MREG}: changed max value • I_{DD_BV}: added max value footnote <p>Table 27</p> <ul style="list-style-type: none"> • $V_{LVDHV3H}$: changed max value • $V_{LVDHV3L}$: added max value • $V_{LVDHV5H}$: changed max value • $V_{LVDHV5L}$: added max value <p>Updated Table 28</p> <p>Table 30</p> <ul style="list-style-type: none"> • Retention: deleted min value footnote for “Blocks with 100,000 P/E cycles” <p>Table 38</p> <ul style="list-style-type: none"> • I_{FXOSC}: added typ value <p>Table 40</p> <ul style="list-style-type: none"> • V_{SXOSC}: changed typ value • $T_{SXOSCSU}$: added max value footnote <p>Table 41</p> <ul style="list-style-type: none"> • Δt_{LTJIT}: added max value <p>Updated Figure 38</p>

Table 50. Revision history (continued)

Revision	Date	Description of Changes
5	02-Nov-2009	<p>In the “MPC5604B/C series block summary” table, added a new row.</p> <p>In the “Absolute maximum ratings” table, changed max value of V_{DD_BV}, V_{DD_ADC}, and V_{IN}.</p> <p>In the “Recommended operating conditions (3.3 V)” table, deleted min value of T_{VDD}.</p> <p>In the “Reset electrical characteristics” table, changed footnotes 3 and 5.</p> <p>In the “Voltage regulator electrical characteristics” table:</p> <ul style="list-style-type: none"> • C_{REGn}: changed max value. • C_{DEC1}: split into 2 rows. • Updated voltage values in footnote 4 <p>In the “Low voltage monitor electrical characteristics” table:</p> <ul style="list-style-type: none"> • Updated column Conditions. • $V_{LVDLVCORL}$, $V_{LVDLVBKPL}$: changed min/max value. <p>In the “Program and erase specifications” table, added initial max value of $T_{dwp\text{rogram}}$.</p> <p>In the “Flash module life” table, changed min value for blocks with 100K P/E cycles</p> <p>In the “Flash power supply DC electrical characteristics” table:</p> <ul style="list-style-type: none"> • I_{FREAD}, I_{FMODE}: added typ value. • Added footnote 1. <p>Added “<i>NVUSRO[WATCHDOG_EN] field description</i>” section.</p> <p>Section 4.18: “ADC electrical characteristics” has been moved up in hierarchy (it was Section 4.18.5).</p> <p>In the “ADC conversion characteristics” table, changed initial max value of R_{AD}.</p> <p>In the “On-chip peripherals current consumption” table:</p> <ul style="list-style-type: none"> • Removed min/max from the heading. • Changed unit of measurement and consequently rounded the values.

Table 50. Revision history (continued)

Revision	Date	Description of Changes
9	16 June 2011	<p>Formatting and minor editorial changes throughout</p> <p>Harmonized oscillator nomenclature</p> <p>Removed all instances of note “All 64 LQFP information is indicative and must be confirmed during silicon validation.”</p> <p>Device comparison table: changed temperature value in footnote 2 from 105 °C to 125 °C</p> <p>MPC560xB LQFP 64-pin configuration and MPC560xC LQFP 64-pin configuration: renamed pin 6 from VPP_TEST to VSS_HV</p> <p>Removed “Pin Muxing” section; added sections “Pad configuration during reset phases”, “Voltage supply pins”, “Pad types”, “System pins”, “Functional ports”, and “Nexus 2+ pins”</p> <p>Section “NVUSRO register”: edited content to separate configuration into electrical parameters and digital functionality; updated footnote describing default value of ‘1’ in field descriptions NVUSRO[PAD3V5V] and NVUSRO[OSCILLATOR_MARGIN]</p> <p>Added section “NVUSRO[WATCHDOG_EN] field description”</p> <p>Recommended operating conditions (3.3 V) and Recommended operating conditions (5.0 V): updated conditions for ambient and junction temperature characteristics</p> <p>I/O input DC electrical characteristics: updated I_{LKG} characteristics</p> <p>Section “I/O pad current specification”: removed content referencing the I_{DYNSEG} maximum value</p> <p>I/O consumption: replaced instances of “Root medium square” with “Root mean square”</p> <p>I/O weight: replaced instances of bit “SRE” with “SRC”; added pads PH[9] and PH[10]; added supply segments; removed weight values in 64-pin LQFP for pads that do not exist in that package</p> <p>Reset electrical characteristics: updated parameter classification for I_{WPU}</p> <p>Updated Voltage regulator electrical characteristics</p> <p>Section “Low voltage detector electrical characteristics”: changed title (was “Voltage monitor electrical characteristics”); added event status flag names found in RGM chapter of device reference manual to POR module and LVD descriptions; replaced instances of “Low voltage monitor” with “Low voltage detector”; updated values for $V_{LVDLVBKPL}$ and $V_{LVDLVCORL}$; replaced “LVD_DIGBKP” with “LVDLVBKP” in note</p> <p>Updated section “Power consumption”</p> <p>Fast external crystal oscillator (4 to 16 MHz) electrical characteristics: updated parameter classification for $V_{FXOSCOP}$</p> <p>Crystal oscillator and resonator connection scheme: added footnote about possibility of adding a series resistor</p> <p>Slow external crystal oscillator (32 kHz) electrical characteristics: updated footnote 1</p> <p>FMPLL electrical characteristics: added short term jitter characteristics; inserted “—” in empty min value cell of t_{lock} row</p> <p>Section “Input impedance and ADC accuracy”: changed “V_A/V_{A2}” to “V_{A2}/V_A” in Equation 11</p> <p>ADC input leakage current: updated I_{LKG} characteristics</p> <p>ADC conversion characteristics: updated symbols</p> <p>On-chip peripherals current consumption: changed “supply current on “$V_{DD_HV_ADC}$” to “supply current on” V_{DD_HV}” in $I_{DD_HV(FLASH)}$ row; updated $I_{DD_HV(PLL)}$ value—was $3 * f_{periph}$, is $30 * f_{periph}$; updated footnotes</p> <p>DSPI characteristics: added rows t_{PCSC} and t_{PASC}</p> <p>Added DSPI PCS strobe (PCSS) timing diagram</p>

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