NXP USA Inc. - SPC5604CK0MLH6 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	45
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5604ck0mlh6

1 Introduction

1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device. To ensure a complete understanding of the device functionality, refer also to the device reference manual and errata sheet.

1.2 Description

The MPC5604B/C is a family of next generation microcontrollers built on the Power Architecture® embedded category.

The MPC5604B/C family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding family of automotive-focused products designed to address the next wave of body electronics applications within the vehicle. The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category and only implements the VLE (variable-length encoding) APU, providing improved code density. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

Table 1. MPC5604B/C device comparison[1]

Feature	Device															
	MPC56 02BxLH	MPC56 02BxLL	MPC56 02BxLQ	MPC56 02CxLH	MPC56 02CxLL	MPC56 03BxLH	MPC56 03BxLL	MPC56 03BxLQ	MPC56 03CxLH	MPC56 03CxLL	MPC56 04BxLH	MPC56 04BxLL	MPC56 04BxLQ	MPC56 04CxLH	MPC56 04CxLL	MPC5604 BxMG
CPU	e200z0h															
Execution speed[2]	Static – up to 64 MHz															
Code Flash	256 KB					384 KB					512 KB					
Data Flash	64 KB (4 × 16 KB)															
RAM	24 KB			32 KB		28 KB			40 KB		32 KB			48 KB		
MPU	8-entry															
ADC (10-bit)	12 ch	28 ch	36 ch	8 ch	28 ch	12 ch	28 ch	36 ch	8 ch	28 ch	12 ch	28 ch	36 ch	8 ch	28 ch	36 ch
CTU	Yes															
Total timer I/O[3] eMIOS	12 ch, 16-bit	28 ch, 16-bit	56 ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	56 ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	56 ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	56 ch, 16-bit
• PWM + MC + IC/OC[4]	2 ch	5 ch	10 ch	2 ch	5 ch	2 ch	5 ch	10 ch	2 ch	5 ch	2 ch	5 ch	10 ch	2 ch	5 ch	10 ch
• PWM + IC/OC[4]	10 ch	20 ch	40 ch	10 ch	20 ch	10 ch	20 ch	40 ch	10 ch	20 ch	10 ch	20 ch	40 ch	10 ch	20 ch	40 ch
• IC/OC[4]	—	3 ch	6 ch	—	3 ch	—	3 ch	6 ch	—	3 ch	—	3 ch	6 ch	—	3 ch	6 ch
SCI (LINFlex)	3[5]			4												
SPI (DSPI)	2	3		2	3	2	3		2	3	2	3		2	3	
CAN (FlexCAN)	2[6]			5	6	3[7]			5	6	3[7]			5	6	
I^{2}C	1															
32 kHz oscillator	Yes															
GPIO[8]	45	79	123	45	79	45	79	123	45	79	45	79	123	45	79	123
Debug	JTAG															Nexus2+
Package	64 LQFP	100 LQFP	144 LQFP	64 LQFP	100 LQFP	64 LQFP	100 LQFP	144 LQFP	64 LQFP	100 LQFP	64 LQFP	100 LQFP	144 LQFP	64 LQFP	100 LQFP	208 MAPBGA[9]

[1] Feature set dependent on selected peripheral multiplexing—table shows example implementation

[2] Based on 125 °C ambient operating temperature

[3] See the eMIOS section of the device reference manual for information on the channel configuration and functions.

[4] IC – Input Capture; OC – Output Compare; PWM – Pulse Width Modulation; MC – Modulus counter

[5] SCI0, SCI1 and SCI2 are available. SCI3 is not available.

[6] CAN0, CAN1 are available. CAN2, CAN3, CAN4 and CAN5 are not available.

[7] CAN0, CAN1 and CAN2 are available. CAN3, CAN4 and CAN5 are not available.

[8] I/O count based on multiplexing with peripherals

[9] 208 MAPBGA available only as development package for Nexus2+

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 —	GPIO[2] E0UC[2] — — WKPU[3][4]	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	3	3	5	9	F2
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 —	GPIO[3] E0UC[3] — — EIRQ[0]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	43	39	68	90	K15
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 —	GPIO[4] E0UC[4] — — WKPU[9][4]	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	20	20	29	43	N6
PA[5]	PCR[5]	AF0 AF1 AF2 AF3	GPIO[5] E0UC[5] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	51	51	79	118	C11
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 —	GPIO[6] E0UC[6] — — EIRQ[1]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	52	52	80	119	D11
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 —	GPIO[7] E0UC[7] LIN3TX — EIRQ[2]	SIUL eMIOS_0 LINFlex_3 — SIUL	I/O I/O O — I	S	Tristate	44	44	71	104	D16
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — N/A[6] —	GPIO[8] E0UC[8] — — EIRQ[3] ABS[0] LIN3RX	SIUL eMIOS_0 — — SIUL BAM LINFlex_3	I/O I/O — — I I I	S	Input, weak pull-up	45	45	72	105	C16
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 N/A[6]	GPIO[9] E0UC[9] — — FAB	SIUL eMIOS_0 — — BAM	I/O I/O — — I	S	Pull-down	46	46	73	106	C15

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — —	GPIO[26] — — — ANS[2] WKPU[8][4]	SIUL — — — ADC WKPU	I/O — — — I I	J	Tristate	31	31	40	54	P9
PB[11][8]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ANS[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — I/O I	J	Tristate	38	36	59	81	N13
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ANX[0]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	39	—	61	83	M16
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ANX[1]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	40	—	63	85	M13
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ANX[2]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	41	37	65	87	L16
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ANX[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	42	38	67	89	L13
PC[0][9]	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M	Input, weak pull-up	59	59	87	126	A8
PC[1][9]	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO[10] —	SIUL — JTAGC —	I/O — O —	M	Tristate	54	54	82	121	C9

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number				
								MPC560xB 64 LQFP	MPC560xC 64 LQFP	100 LQFP	144 LQFP	208 MAPBGA[3]
PC[2]	PCR[34]	AF0	GPIO[34]	SIUL	I/O	M	Tristate	50	50	78	117	A11
		AF1	SCK_1	DSPI_1	I/O							
		AF2	CAN4TX[11]	FlexCAN_4	O							
		AF3	—	—	—							
		—	EIRQ[5]	SIUL	I							
PC[3]	PCR[35]	AF0	GPIO[35]	SIUL	I/O	S	Tristate	49	49	77	116	B11
		AF1	CS0_1	DSPI_1	I/O							
		AF2	MA[0]	ADC	O							
		AF3	—	—	—							
		—	CAN1RX	FlexCAN_1	I							
		—	CAN4RX[11]	FlexCAN_4	I							
		—	EIRQ[6]	SIUL	I							
PC[4]	PCR[36]	AF0	GPIO[36]	SIUL	I/O	M	Tristate	62	62	92	131	B7
		AF1	—	—	—							
		AF2	—	—	—							
		AF3	—	—	—							
		—	SIN_1	DSPI_1	I							
		—	CAN3RX[11]	FlexCAN_3	I							
PC[5]	PCR[37]	AF0	GPIO[37]	SIUL	I/O	M	Tristate	61	61	91	130	A7
		AF1	SOUT_1	DSPI1	O							
		AF2	CAN3TX[11]	FlexCAN_3	O							
		AF3	—	—	—							
		—	EIRQ[7]	SIUL	I							
PC[6]	PCR[38]	AF0	GPIO[38]	SIUL	I/O	S	Tristate	16	16	25	36	R2
		AF1	LIN1TX	LINFlex_1	O							
		AF2	—	—	—							
		AF3	—	—	—							
PC[7]	PCR[39]	AF0	GPIO[39]	SIUL	I/O	S	Tristate	17	17	26	37	P3
		AF1	—	—	—							
		AF2	—	—	—							
		AF3	—	—	—							
		—	LIN1RX	LINFlex_1	I							
		—	WKPU[12][4]	WKPU	I							
PC[8]	PCR[40]	AF0	GPIO[40]	SIUL	I/O	S	Tristate	63	63	99	143	A1
		AF1	LIN2TX	LINFlex_2	O							
		AF2	—	—	—							
		AF3	—	—	—							

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid applying any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

3.10 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in Table 8 are used and the parameters are tagged accordingly in the tables where appropriate.

Table 8. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.11 NVUSRO register

Bit values in the Non-Volatile User Options (NVUSRO) Register control portions of the device configuration, namely electrical parameters such as high voltage supply and oscillator margin, as well as digital functionality (watchdog enable/disable after reset).

For a detailed description of the NVUSRO register, please refer to the device reference manual.

3.11.1 NVUSRO[PAD3V5V] field description

The DC electrical characteristics are dependent on the PAD3V5V bit value. Table 9 shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 9. PAD3V5V field description

Value[1]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

3.15.2 I/O input DC characteristics

Table 16 provides input DC electrical characteristics as described in Figure 7.

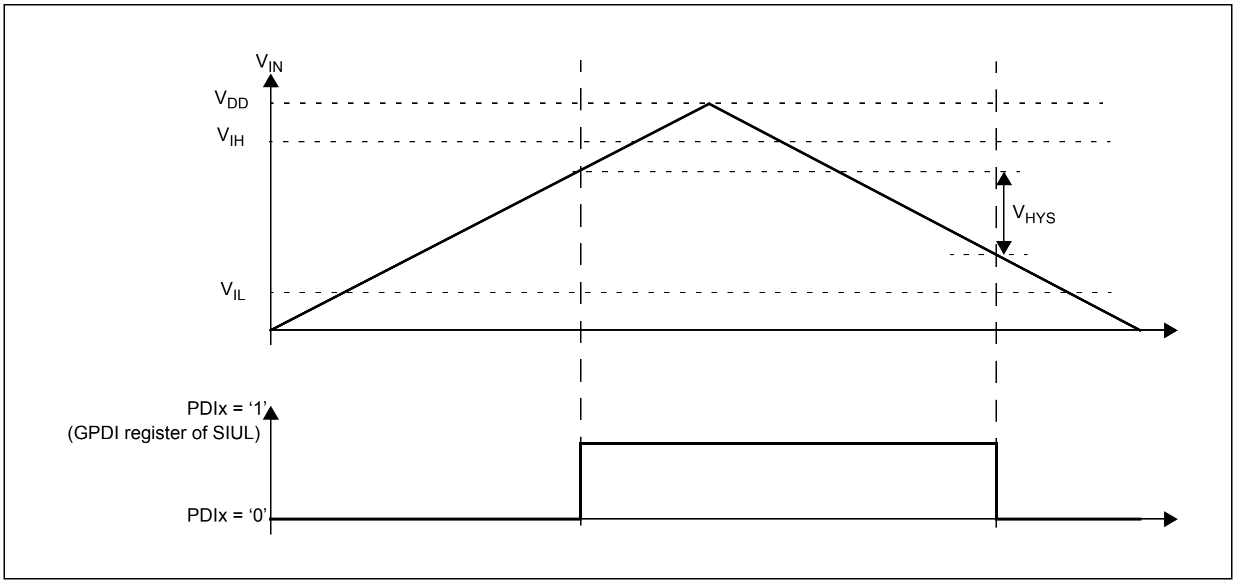


Figure 7. I/O input DC electrical characteristics definition

Table 16. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	—		$0.65V_{DD}$	—	$V_{DD}+0.4$	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	—		–0.4	—	$0.35V_{DD}$	
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—		$0.1V_{DD}$	—	—	
I_{LKG}	CC	D	Digital input leakage	No injection on adjacent pin	T_A = –40 °C	—	2	200	nA
		D			T_A = 25 °C	—	2	200	
		D			T_A = 85 °C	—	5	300	
		D			T_A = 105 °C	—	12	500	
		P			T_A = 125 °C	—	70	1000	
W_{FI}[2]	SR	P	Wakeup input filtered pulse	—		—	—	40	ns
W_{NFI}[2]	SR	P	Wakeup input not filtered pulse	—		1000	—	—	ns

---

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

[2] In the range from 40 to 1000 ns, pulses can be filtered or not filtered, according to operating temperature and voltage.

Table 24. I/O weight[1] (continued)

Supply segment			Pad	144/100 LQFP				64 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
144 LQFP	100 LQFP	64 LQFP[2]		SRC[3] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
2	2	2	PB[9]	1%	—	1%	—	1%	—	1%	—
			PB[8]	1%	—	1%	—	1%	—	1%	—
			PB[10]	6%	—	7%	—	6%	—	7%	—
	—	—	PF[0]	6%	—	7%	—	—	—	—	—
	—	—	PF[1]	7%	—	8%	—	—	—	—	—
	—	—	PF[2]	7%	—	8%	—	—	—	—	—
	—	—	PF[3]	7%	—	9%	—	—	—	—	—
	—	—	PF[4]	8%	—	9%	—	—	—	—	—
	—	—	PF[5]	8%	—	10%	—	—	—	—	—
	—	—	PF[6]	8%	—	10%	—	—	—	—	—
	—	—	PF[7]	9%	—	10%	—	—	—	—	—
	2	—	PD[0]	1%	—	1%	—	—	—	—	—
		—	PD[1]	1%	—	1%	—	—	—	—	—
		—	PD[2]	1%	—	1%	—	—	—	—	—
		—	PD[3]	1%	—	1%	—	—	—	—	—
		—	PD[4]	1%	—	1%	—	—	—	—	—
		—	PD[5]	1%	—	1%	—	—	—	—	—
		—	PD[6]	1%	—	1%	—	—	—	—	—
		—	PD[7]	1%	—	1%	—	—	—	—	—
		—	PD[8]	1%	—	1%	—	—	—	—	—
		2	PB[4]	1%	—	1%	—	1%	—	1%	—
			PB[5]	1%	—	1%	—	1%	—	2%	—
			PB[6]	1%	—	1%	—	1%	—	2%	—
			PB[7]	1%	—	1%	—	1%	—	2%	—
		—	PD[9]	1%	—	1%	—	—	—	—	—
		—	PD[10]	1%	—	1%	—	—	—	—	—
		—	PD[11]	1%	—	1%	—	—	—	—	—
		2	PB[11]	11%	—	13%	—	17%	—	21%	—
		—	PD[12]	11%	—	13%	—	—	—	—	—
		2	PB[12]	11%	—	13%	—	18%	—	21%	—
		—	PD[13]	10%	—	12%	—	—	—	—	—

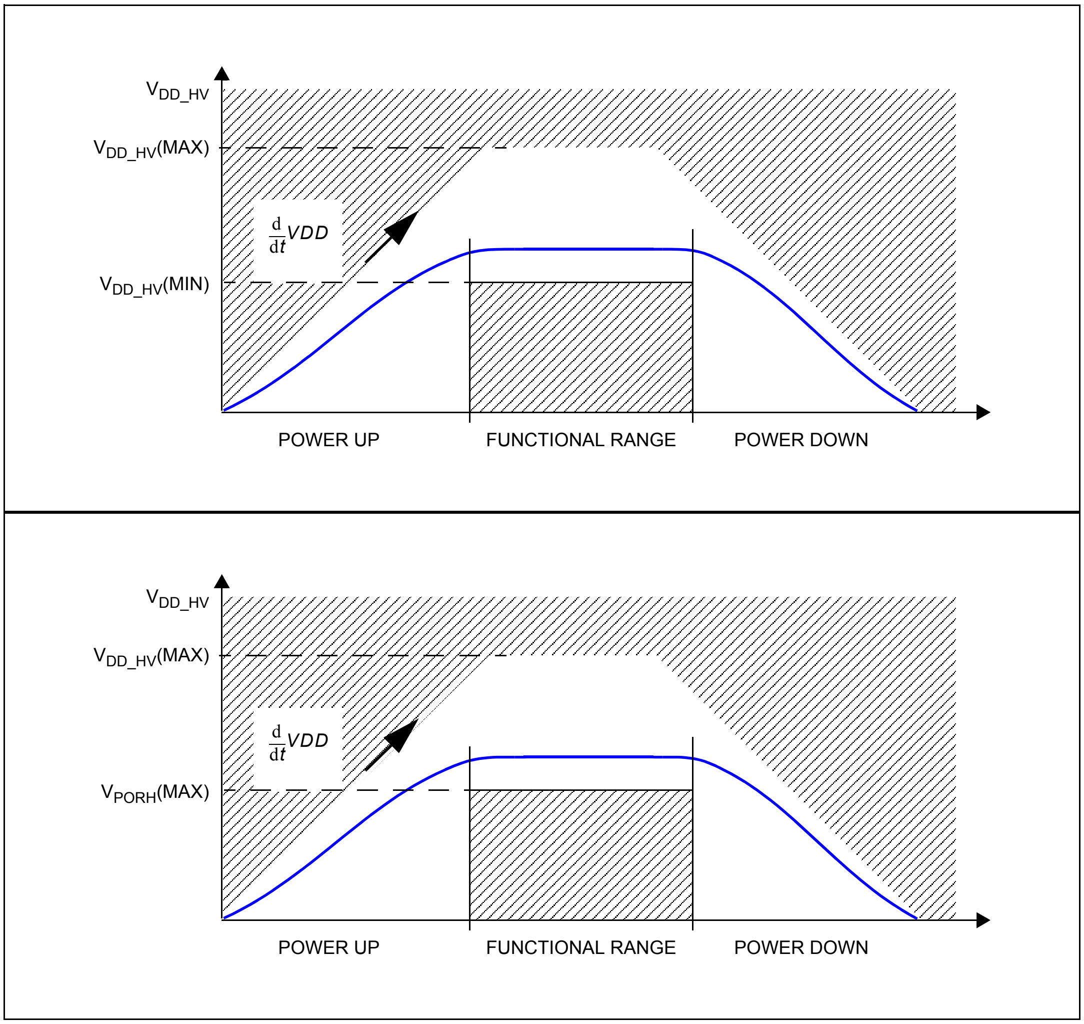


Figure 11. V_{DD_HV} and V_{DD_BV} maximum slope

When STANDBY mode is used, further constraints are applied to the both V_{DD_HV} and V_{DD_BV} in order to guarantee correct regulator function during STANDBY exit. This is described on Figure 12.

STANDBY regulator constraints should normally be guaranteed by implementing equivalent of CSTDBY capacitance on application board (capacitance and ESR typical values), but would actually depend on exact characteristics of application external regulator.

Table 30. Flash module life

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
P/E	CC	C	Number of program/erase cycles per block over the operating temperature range (T_J)	16 KB blocks	100,000	—	—	cycles
				32 KB blocks	10,000	100,000	—	
				128 KB blocks	1,000	100,000	—	
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature[1]	Blocks with 0–1,000 P/E cycles	20	—	—	years
				Blocks with 1,001–10,000 P/E cycles	10	—	—	
				Blocks with 10,001–100,000 P/E cycles	5	—	—	

[1] Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 31. Flash read access timing

Symbol		C	Parameter	Conditions[1]	Max	Unit
f_{READ}	CC	P	Maximum frequency for Flash reading	2 wait states	64	MHz
		C		1 wait state	40	
		C		0 wait states	20	

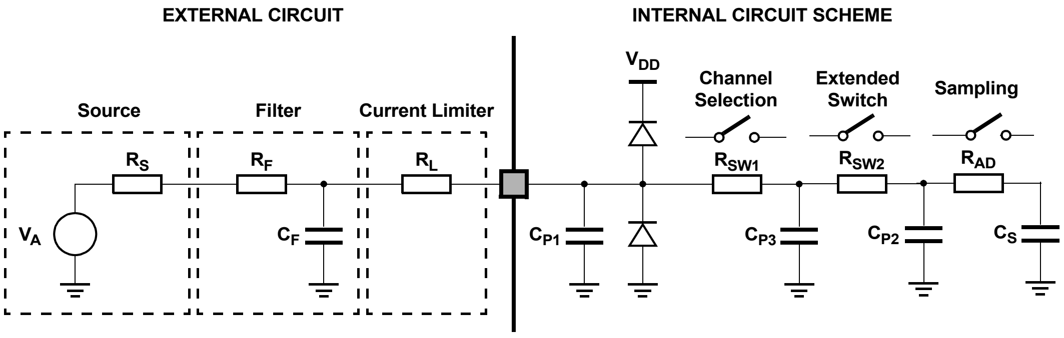
[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

3.19.2 Flash power supply DC characteristics

Table 32 shows the power supply DC characteristics on external supply.

Table 32. Flash memory power supply DC electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
I_{FREAD}[2]	CC	D	Sum of the current consumption on VDD_HV and VDD_BV on read access	Code flash memory module read f_{CPU} = 64 MHz[3]	—	15	33	mA
				Data flash memory module read f_{CPU} = 64 MHz[3]	—	15	33	
I_{FMOD}[2]	CC	D	Sum of the current consumption on VDD_HV and VDD_BV on matrix modification (program/erase)	Program/Erase ongoing while reading code flash memory registers f_{CPU} = 64 MHz[3]	—	15	33	mA
				Program/Erase ongoing while reading data flash memory registers f_{CPU} = 64 MHz[3]	—	15	33	



R_S: Source impedance
R_F: Filter resistance
C_F: Filter capacitance
R_L: Current limiter resistance
R_{SW1}: Channel selection switch impedance (two contributions, R_{SW1} and R_{SW2})
R_{AD}: Sampling switch impedance
C_P: Pin capacitance (two contributions, C_{P1}, C_{P2} and C_{P3})
C_S: Sampling capacitance

Figure 21. Input equivalent circuit (extended channels)

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit in Figure 20): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

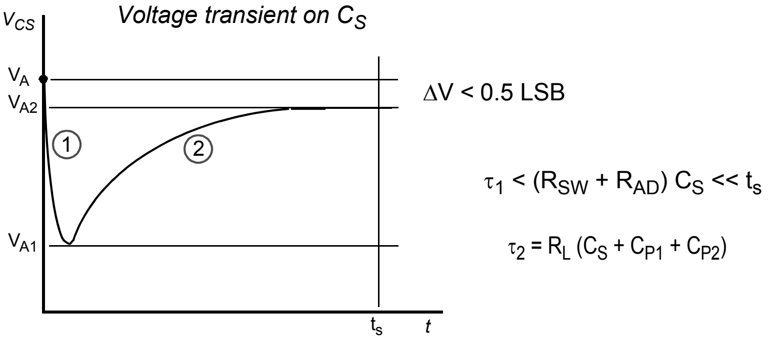


Figure 22. Transient behavior during sampling phase

In particular two different transient periods can be distinguished:

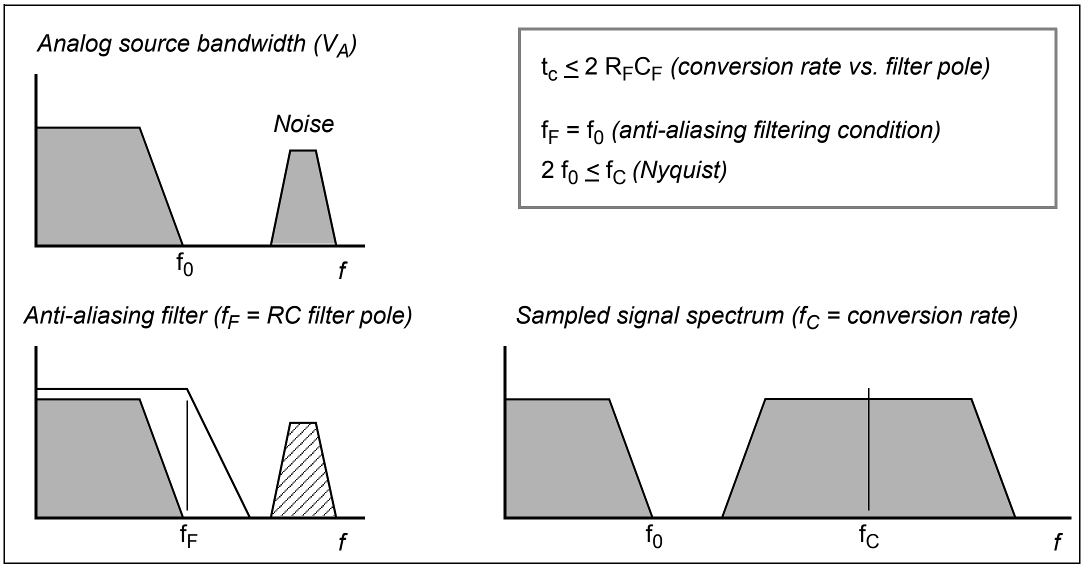


Figure 23. Spectral representation of input signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (t_c). Again the conversion period t_c is longer than the sampling time t_s, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter $R_F C_F$ is definitively much higher than the sampling time t_s, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive Equation 11 between the ideal and real sampled voltage on C_S:

Eqn. 11

$$\frac{V_{A2}}{V_A} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Eqn. 12

$$C_F > 2048 \bullet C_S$$

[3] During the conversion, the total current consumption is given from the sum of the static and dynamic consumption, i.e., (41 + 5) * f_{periph}.

Table 47. DSPI characteristics[1] (continued)

No.	Symbol		C	Parameter		DSPI0/DSPI1			DSPI2			Unit
						Min	Typ	Max	Min	Typ	Max	
10	t_{HI}	SR	D	Data hold time for inputs	Master mode	0	—	—	0	—	—	ns
					Slave mode	2[6]	—	—	2[6]	—	—	
11	t_{SUO}[7]	CC	D	Data valid after SCK edge	Master mode	—	—	32	—	—	50	ns
					Slave mode	—	—	52	—	—	160	
12	t_{HO}[7]	CC	D	Data hold time for outputs	Master mode	0	—	—	0	—	—	ns
					Slave mode	8	—	—	13	—	—	

[1] Operating conditions: C_L = 10 to 50 pF, $Slew_{IN}$ = 3.5 to 15 ns.

[2] Maximum value is reached when CSn pad is configured as SLOW pad while SCK pad is configured as MEDIUM. A positive value means that SCK starts before CSn is asserted. DSPI2 has only SLOW SCK available.

[3] Maximum value is reached when CSn pad is configured as MEDIUM pad while SCK pad is configured as SLOW. A positive value means that CSn is deasserted before SCK. DSPI0 and DSPI1 have only MEDIUM SCK available.

[4] The t_{CSC} delay value is configurable through a register. When configuring t_{CSC} (using PCSSCK and CSSCK fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{CSC} to ensure positive t_{CSCext}.

[5] The t_{ASC} delay value is configurable through a register. When configuring t_{ASC} (using PASC and ASC fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{ASC} to ensure positive t_{ASCext}.

[6] This delay value corresponds to SMPL_PT = 00b which is bit field 9 and 8 of the DSPI_MCR.

[7] SCK and SOUT configured as MEDIUM pad

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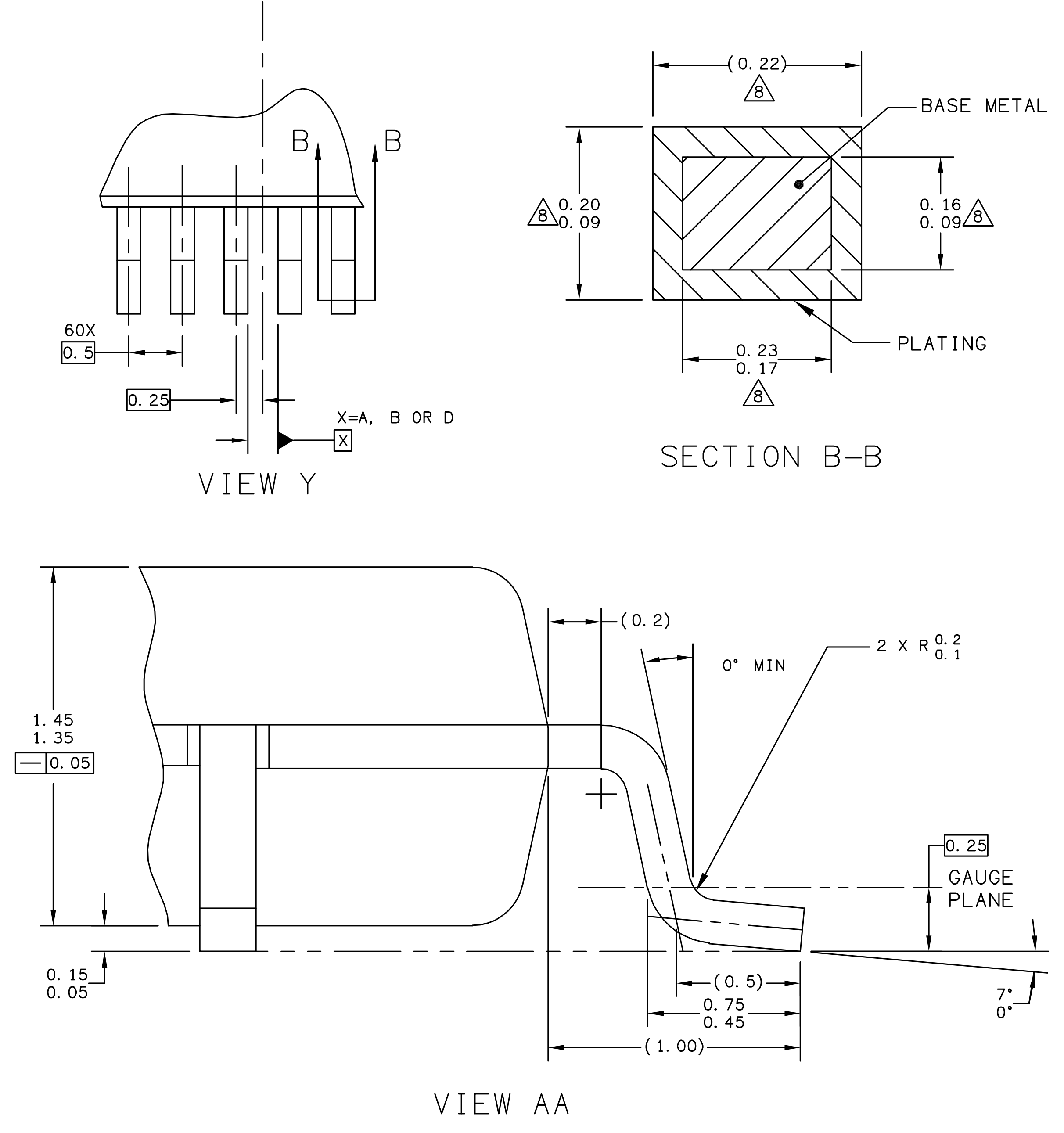

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F-02	
	STANDARD: JEDEC MS-026 BCD	
	PACKAGE CODE: 8426	SHEET: 2

Figure 36. 64 LQFP package mechanical drawing (2 of 3)

4.1.4 208 MAPBGA

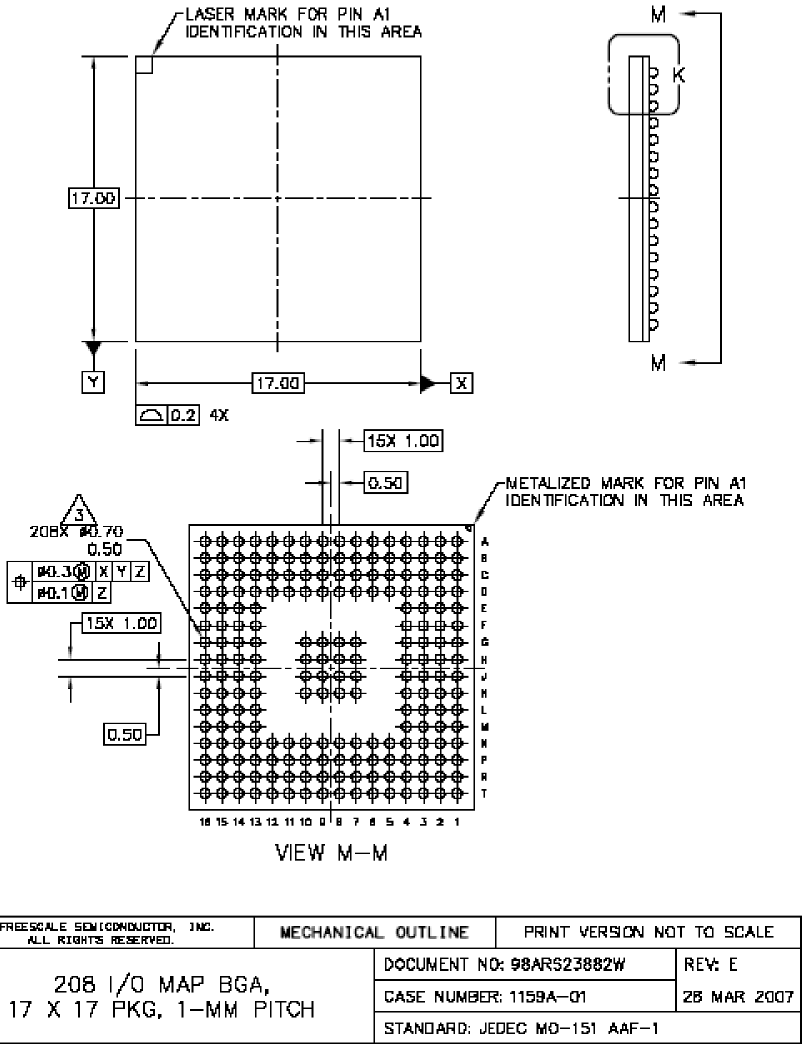

Figure 43. 208 MAPBGA package mechanical drawing (1 of 2)

Table 50. Revision history (continued)

Revision	Date	Description of Changes
7	05-Jul-2010	Added 64 LQFP package information Updated the “Features” section. Figures “LQFP 100-pin configuration” and “LQFP 100-pin configuration”: removed alternate function information Added “Functional port pin descriptions” table Added eDMA block in the “MPC5604B/C series block diagram” figure Deleted the “NVUSRO[WATCHDOG_EN] field description” section In the “Recommended operating conditions (3.3 V)” and “Recommended operating conditions (5.0 V)” tables, deleted the conditions of $T_{A\ \text{C-Grade Part}}$, $T_{A\ \text{V-Grade Part}}$, $T_{A\ \text{M-Grade Part}}$ In the “LQFP thermal characteristics” table, rounded the values. In the “$\overline{\text{RESET}}$ electrical characteristics” section, replaced “nRSTIN” with “$\overline{\text{RESET}}$”. In the “I/O input DC electrical characteristics” table: • W_{FI}: inserted a footnote • W_{NFI}: inserted a footnote In the “Low voltage monitor electrical characteristics” table: • changed min value $V_{LVDHV3L}$, from 2.7 to 2.6 • Inserted max value of $V_{LVDLVCORL}$ In the “FMPLL electrical characteristics” table, rounded the values of $f_{VCO.}$ In the “DSPI characteristics” table: • Added Δt_{ASC} row • Update values of t_A In the “ADC conversion characteristics” table, added “I_{ADCPWD}” and “I_{ADCRUN}” rows Removed “Orderable part number summary” table.
8	25-Nov-2010	Editorial changes and improvements. In the “MPC5604B/C device comparison” table, changed the temperature value from 105 to 125 °C, in the footnote regarding “Execution speed”. In the “Recommended operating conditions (3.3 V)” and “Recommended operating conditions (5.0 V)” tables, restored the conditions of $T_{A\ \text{C-Grade Part}}$, $T_{A\ \text{V-Grade Part}}$, $T_{A\ \text{M-Grade Part}}$ In the “LQFP thermal characteristics” table, added values concerning 64 LQFP package. In the “MEDIUM configuration output buffer electrical characteristics” table: fixed a typo in last row of conditions column, there was I_{OH} that now is I_{OL}. In the “Reset electrical characteristics” table, changed the parameter classification tag for V_{OL} and $\|I_{WPU}\|$. In the “Low voltage monitor electrical characteristics” table, changed the max value of $V_{LVDLVCORL}$ from 1.5V to 1.15V. In the “Program and erase specifications” table, replaced “T_{eslat}” with “T_{esus}”. In the “FMPLL electrical characteristics” table, changed the parameter classification tag for f_{VCO}.

Table 50. Revision history (continued)

Revision	Date	Description of Changes
9	16 June 2011	Formatting and minor editorial changes throughout Harmonized oscillator nomenclature Removed all instances of note “All 64 LQFP information is indicative and must be confirmed during silicon validation.” Device comparison table: changed temperature value in footnote 2 from 105 °C to 125 °C MPC560xB LQFP 64-pin configuration and MPC560xC LQFP 64-pin configuration: renamed pin 6 from VPP_TEST to VSS_HV Removed “Pin Muxing” section; added sections “Pad configuration during reset phases”, “Voltage supply pins”, “Pad types”, “System pins,” “Functional ports”, and “Nexus 2+ pins” Section “NVUSRO register”: edited content to separate configuration into electrical parameters and digital functionality; updated footnote describing default value of ‘1’ in field descriptions NVUSRO[PAD3V5V] and NVUSRO[OSCILLATOR_MARGIN] Added section “NVUSRO[WATCHDOG_EN] field description” Recommended operating conditions (3.3 V) and Recommended operating conditions (5.0 V): updated conditions for ambient and junction temperature characteristics I/O input DC electrical characteristics: updated I_{LKG} characteristics Section “I/O pad current specification”: removed content referencing the I_{DYNSEG} maximum value I/O consumption: replaced instances of “Root medium square” with “Root mean square” I/O weight: replaced instances of bit “SRE” with “SRC”; added pads PH[9] and PH[10]; added supply segments; removed weight values in 64-pin LQFP for pads that do not exist in that package Reset electrical characteristics: updated parameter classification for $\vert I_{WPU}\vert$ Updated Voltage regulator electrical characteristics Section “Low voltage detector electrical characteristics”: changed title (was “Voltage monitor electrical characteristics”); added event status flag names found in RGM chapter of device reference manual to POR module and LVD descriptions; replaced instances of “Low voltage monitor” with “Low voltage detector”; updated values for $V_{LVDLVBKPL}$ and $V_{LVDLVCORL}$; replaced “LVD_DIGBKP” with “LVDLVBKP” in note Updated section “Power consumption” Fast external crystal oscillator (4 to 16 MHz) electrical characteristics: updated parameter classification for $V_{FXOSCOP}$ Crystal oscillator and resonator connection scheme: added footnote about possibility of adding a series resistor Slow external crystal oscillator (32 kHz) electrical characteristics: updated footnote 1 FMPLL electrical characteristics: added short term jitter characteristics; inserted “—” in empty min value cell of t_{lock} row Section “Input impedance and ADC accuracy”: changed “V_A/V_{A2}” to “V_{A2}/V_A” in Equation 11 ADC input leakage current: updated I_{LKG} characteristics ADC conversion characteristics: updated symbols On-chip peripherals current consumption: changed “supply current on “$V_{DD\_HV\_ADC}$” to “supply current on” V_{DD_HV}” in $I_{DD\_HV(FLASH)}$ row; updated $I_{DD\_HV(PLL)}$ value—was 3 * f_{periph}, is 30 * f_{periph}; updated footnotes DSPI characteristics: added rows t_{PCSC} and t_{PASC} Added DSPI PCS strobe (PCSS) timing diagram

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