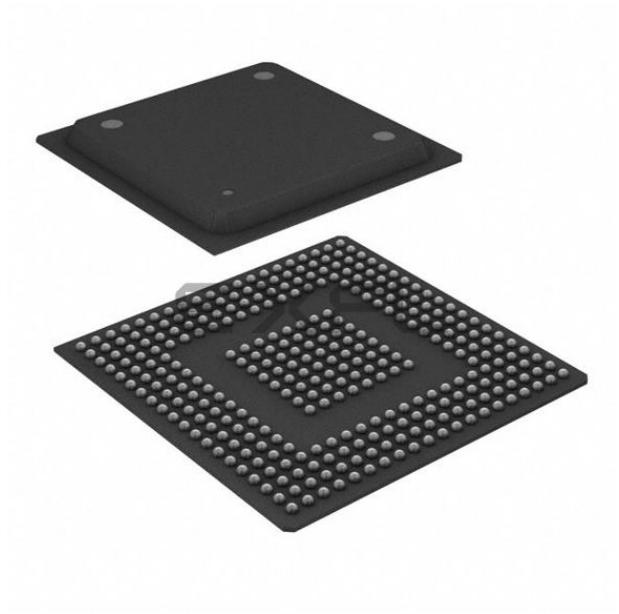


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

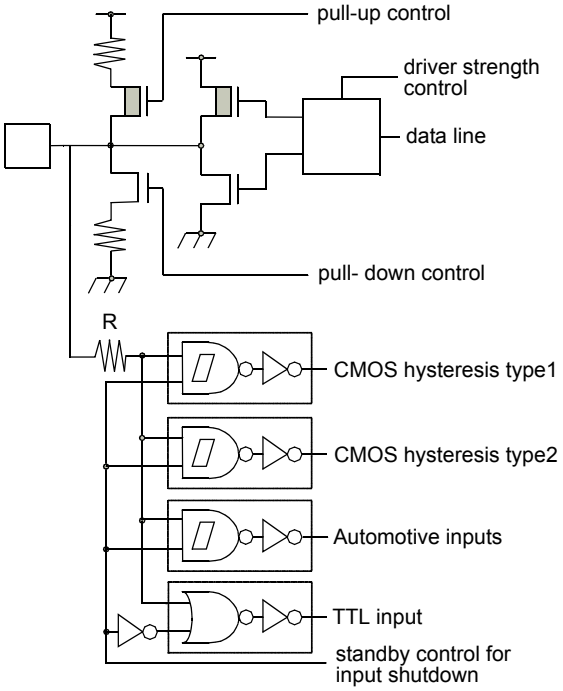
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, WDT
Number of I/O	205
Program Memory Size	2.112MB (2.112M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	112K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	320-BBGA
Supplier Device Package	320-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f469gapb-gs-k6

Contents

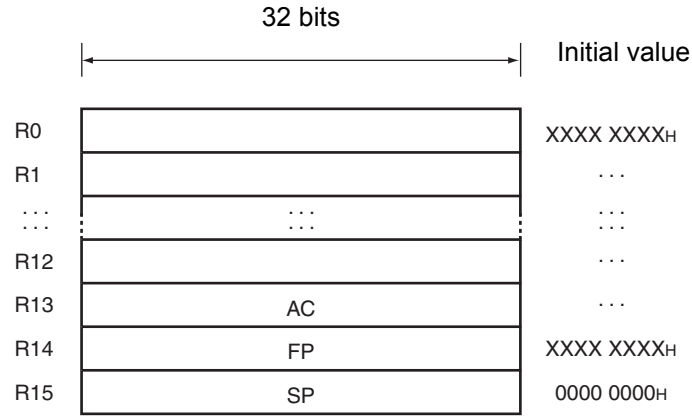
JEDEC	Pin no.	Pin name	I/O	I/O circuit type[1]	Description
C11	197	P22_5	I/O	C	General-purpose input/output port
		SCL0			I^2C bus clock input/output pin (open drain)
C10	198	P14_0	I/O	A	General-purpose input/output port
		ICU0			Input capture input pin
		TIN0			External trigger input pin of reload timer
		TTG8/0			External trigger input pin of PPG timer
C9	199	P14_4	I/O	A	General-purpose input/output port
		ICU4			Input capture input pin
		TIN4			External trigger input pin of reload timer
		TTG12/4			External trigger input pin of PPG timer
C8	200	P16_0	I/O	A	General-purpose input/output port
		PPG8			Output pin of PPG timer
C7	201	P16_3	I/O	A	General-purpose input/output port
		PPG11			Output pin of PPG timer
C6	202	P16_7	I/O	A	General-purpose input/output port
		PPG15			Output pin of PPG timer
		ATGX			A/D converter external trigger input pin
C5	203	P15_2	I/O	A	General-purpose input/output port
		OCU2			Output compare output pin
		TOT2			Reload timer output pin
C4	204	P15_6	I/O	A	General-purpose input/output port
		OCU6			Output compare output pin
		TOT6			Reload timer output pin
E4	206	P24_7	I/O	C	General-purpose input/output port
		INT7			External interrupt input pin
		SCL3			I^2C bus clock input/output pin (open drain)
G4	208	P09_2	I/O	A	General-purpose input/output port
		CSX2			Chip select output pin
J4	210	P08_1	I/O	A	General-purpose input/output port
		WRX1			External write strobe output pin
L4	212	P07_0	I/O	A	General-purpose input/output port
		A0			Signal pin of external address bus (bit0)
M4	213	P07_4	I/O	A	General-purpose input/output port
		A4			Signal pin of external address bus (bit4)

4. I/O Circuit Types

Type	Circuit	Remarks
A		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.

8.4 Registers

8.4.1 General-Purpose Register



Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

Of the 16 registers, enhanced commands are provided for the following registers to enable their use for particular applications.

R13: Virtual accumulator

R14: Frame pointer

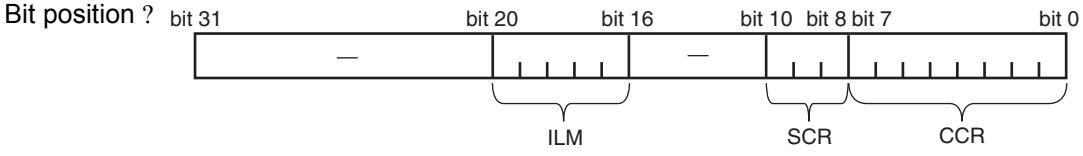
R15: Stack pointer

Initial values at reset are undefined for R0 to R14. The value for R15 is 00000000_H (SSP value).

8.4.2 PS (Program Status)

This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

All undefined bits (-) in the diagram are Reserved bits. The read values are always “0”. Write access to these bits is invalid.



9.4 Parallel Flash Programming Mode

9.4.1 Flash configuration in Parallel Flash Programming Mode

9.4.1.1 Parallel Flash programming mode (MD[2:0] = 111):

MB91F469Gx

FA[21:0]	
003F:FFFFh 003F:0000h	SA39 (64KB)
003E:FFFFh 003E:0000h	SA38 (64KB)
003D:FFFFh 003D:0000h	SA37 (64KB)
003C:FFFFh 003C:0000h	SA36 (64KB)
003B:FFFFh 003B:0000h	SA35 (64KB)
003A:FFFFh 003A:0000h	SA34 (64KB)
0039:FFFFh 0039:0000h	SA33 (64KB)
0038:FFFFh 0038:0000h	SA32 (64KB)
0037:FFFFh 0037:0000h	SA31 (64KB)
0036:FFFFh 0036:0000h	SA30 (64KB)
0035:FFFFh 0035:0000h	SA29 (64KB)
0034:FFFFh 0034:0000h	SA28 (64KB)
0033:FFFFh 0033:0000h	SA27 (64KB)
0032:FFFFh 0032:0000h	SA26 (64KB)
0031:FFFFh 0031:0000h	SA25 (64KB)
0030:FFFFh 0030:0000h	SA24 (64KB)
002F:FFFFh 002F:0000h	SA23 (64KB)
002E:FFFFh 002E:0000h	SA22 (64KB)
002D:FFFFh 002D:0000h	SA21 (64KB)
002C:FFFFh 002C:0000h	SA20 (64KB)
002B:FFFFh 002B:0000h	SA19 (64KB)

002A:FFFFh 002A:0000h	SA18 (64KB)
0029:FFFFh 0029:0000h	SA17 (64KB)
0028:FFFFh 0028:0000h	SA16 (64KB)
0027:FFFFh 0027:0000h	SA15 (64KB)
0026:FFFFh 0026:0000h	SA14 (64KB)
0025:FFFFh 0025:0000h	SA13 (64KB)
0024:FFFFh 0024:0000h	SA12 (64KB)
0023:FFFFh 0023:0000h	SA11 (64KB)
0022:FFFFh 0022:0000h	SA10 (64KB)
0021:FFFFh 0021:0000h	SA9 (64KB)
0020:FFFFh 0020:0000h	SA8 (64KB)
001F:FFFFh 001F:E000h	SA7 (8KB)
001F:DFFFh 001F:C000h	SA6 (8KB)
001F:BFFFh 001F:A000h	SA5 (8KB)
001F:9FFFh 001F:8000h	SA4 (8KB)
001F:7FFFh 001F:6000h	SA3 (8KB)
001F:5FFFh 001F:4000h	SA2 (8KB)
001F:3FFFh 001F:2000h	SA1 (8KB)
001F:1FFFh 001F:0000h	SA0 (8KB)

	FA[1:0]=00	FA[1:0]=10
I6bit write mod	DQ[15:0]	DQ[15:0]

Remark: Always keep FA[0] = 0 and FA[22] = 1

10. Memory Space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

■ Direct addressing area

The following address space area is used for I/O.

This area is called direct addressing area, and the address of an operand can be specified directly in an instruction.

The size of directly addressable area depends on the length of the data being accessed as shown below.

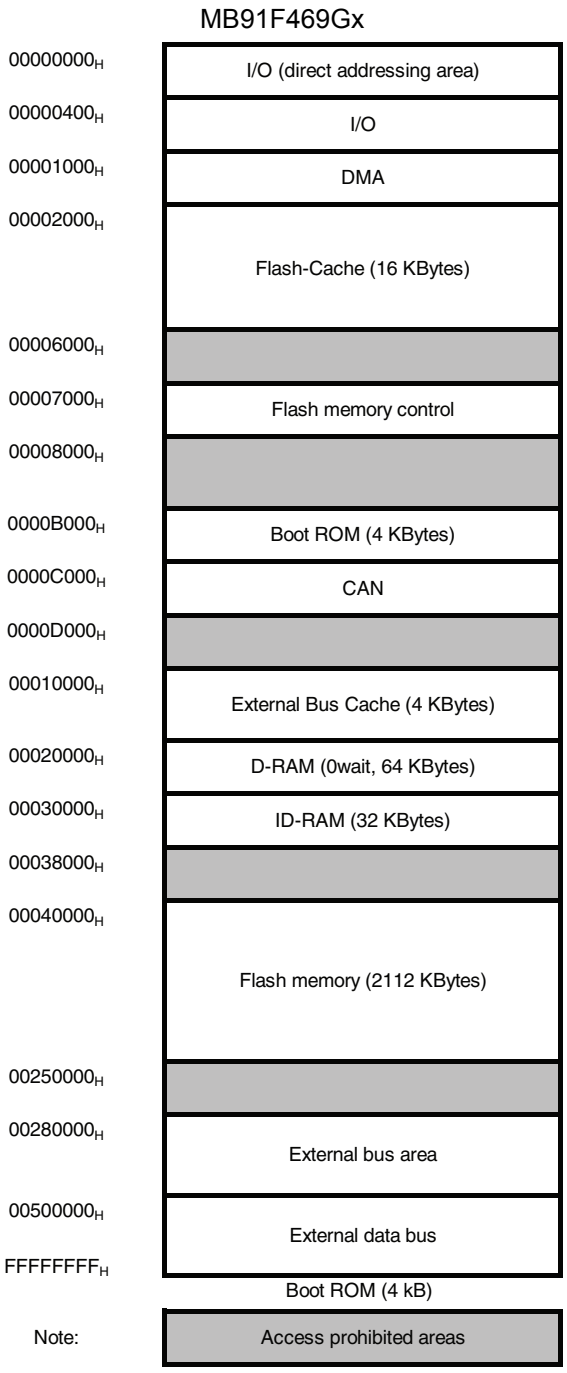
Byte data access : 000_H to $0FF_H$

Half word access : 000_H to $1FF_H$

Word data access : 000_H to $3FF_H$

11. Memory Maps

11.1 MB91F469Gx



	Register				
Address	**+1**	**+2**	**+3**	**+4**	**Block**
000000_H	PDR00 [R/W] XXXXXXXX	PDR01 [R/W] XXXXXXXX	PDR02 [R/W] XXXXXXXX	PDR03 [R/W] XXXXXXXX	General Purpose IO Port Data Register
000004_H	PDR04 [R/W] - - - - XXXX	PDR05 [R/W] XXXXXXXX	PDR06 [R/W] XXXXXXXX	PDR07 [R/W] XXXXXXXX	
000008_H	PDR08 [R/W] XXXXXXXX	PDR09 [R/W] XXXXXXXX	PDR10 [R/W] - XXXXXXX	PDR11 [R/W] - - - - - - XX	
$00000C_H$	Reserved	PDR13 [R/W] XXXXXXXX	PDR14 [R/W] XXXXXXXX	PDR15 [R/W] XXXXXXXX	
000010_H	PDR16 [R/W] XXXXXXXX	PDR17 [R/W] XXXXXXXX	PDR18 [R/W] - XXX - XXX	PDR19 [R/W] - XXX - XXX	
000014_H	PDR20 [R/W] - XXX - XXX	PDR21 [R/W] - XXX - XXX	PDR22 [R/W] XXXXXXXX	PDR23 [R/W] XXXXXXXX	
000018_H	PDR24 [R/W] XXXXXXXX	Reserved	PDR26 [R/W] XXXXXXXX	PDR27 [R/W] XXXXXXXX	
$00001C_H$	PDR28 [R/W] XXXXXXXX	PDR29 [R/W] XXXXXXXX	Reserved	Reserved	
000020_H - $00002C_H$	Reserved				Reserved
000030_H	EIRR0 [R/W] XXXXXXXX	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		Ext. INT 0-7 NMI
000034_H	EIRR1 [R/W] XXXXXXXX	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		Ext. INT 8-15
000038_H	DICR [R/W] - - - - - - - 0	HRCL [R/W] 0 - - 11111	Reserved		DLYI/I-unit
$00003C_H$	Reserved				Reserved
000040_H	SCR00 [R/W,W] 00000000	SMR00 [R/W,W] 00000000	SSR00 [R/W,R] 00001000	RDR00/TDR00 [R/W] 00000000	LIN-USART 0
000044_H	ESCR00 [R/W] 00000X00	ECCR00 [R/W,R,W] -00000XX	Reserved		
000048_H	SCR01 [R/W,W] 00000000	SMR01 [R/W,W] 00000000	SSR01 [R/W,R] 00001000	RDR01/TDR01 [R/W] 00000000	LIN-USART 1
$00004C_H$	ESCR01 [R/W] 00000X00	ECCR01 [R/W,R,W] -00000XX	Reserved		
000050_H	SCR02 [R/W,W] 00000000	SMR02 [R/W,W] 00000000	SSR02 [R/W,R] 00001000	RDR02/TDR02 [R/W] 00000000	LIN-USART 2
000054_H	ESCR02 [R/W] 00000X00	ECCR02 [R/W,R,W] -00000XX	Reserved		
000058_H	SCR03[R/W,W] 00000000	SMR03 [R/W,W] 00000000	SSR03 [R/W,R] 00001000	RDR03/TDR02 [R/W] 00000000	LIN-USART 3
$00005C_H$	ESCR03 [R/W] 00000X00	ECCR03 [R/W,R,W] -00000XX	Reserved		

	Register				
Address	**+1**	**+2**	**+3**	**+4**	**Block**
000104_H	GCN11 [R/W] 00110010 00010000		Reserved	GCN21 [R/W] - - - - 0000	PPG Control 4-7
000108_H	GCN12 [R/W] 00110010 00010000		Reserved	GCN22 [R/W] - - - - 0000	PPG Control 8-11
$00010C_H$	Reserved				Reserved
000110_H	PTMR00 [R] 11111111 11111111		PCSR00 [W] XXXXXXXX XXXXXXXX		PPG 0
000114_H	PDUT00 [W] XXXXXXXX XXXXXXXX		PCNH00 [R/W] 0000000 -	PCNL00 [R/W] 000000 - 0	
000118_H	PTMR01 [R] 11111111 11111111		PCSR01 [W] XXXXXXXX XXXXXXXX		PPG 1
$00011C_H$	PDUT01 [W] XXXXXXXX XXXXXXXX		PCNH01 [R/W] 0000000 -	PCNL01 [R/W] 000000 - 0	
000120_H	PTMR02 [R] 11111111 11111111		PCSR02 [W] XXXXXXXX XXXXXXXX		PPG 2
000124_H	PDUT02 [W] XXXXXXXX XXXXXXXX		PCNH02 [R/W] 0000000 -	PCNL02 [R/W] 000000 - 0	
000128_H	PTMR03 [R] 11111111 11111111		PCSR03 [W] XXXXXXXX XXXXXXXX		PPG 3
$00012C_H$	PDUT03 [W] XXXXXXXX XXXXXXXX		PCNH03 [R/W] 0000000 -	PCNL03 [R/W] 000000 - 0	
000130_H	PTMR04 [R] 11111111 11111111		PCSR04 [W] XXXXXXXX XXXXXXXX		PPG 4
000134_H	PDUT04 [W] XXXXXXXX XXXXXXXX		PCNH04 [R/W] 0000000 -	PCNL04 [R/W] 000000 - 0	
000138_H	PTMR05 [R] 11111111 11111111		PCSR05 [W] XXXXXXXX XXXXXXXX		PPG 5
$00013C_H$	PDUT05 [W] XXXXXXXX XXXXXXXX		PCNH05 [R/W] 0000000 -	PCNL05 [R/W] 000000 - 0	
000140_H	PTMR06 [R] 11111111 11111111		PCSR06 [W] XXXXXXXX XXXXXXXX		PPG 6
000144_H	PDUT06 [W] XXXXXXXX XXXXXXXX		PCNH06 [R/W] 0000000 -	PCNL06 [R/W] 000000 - 0	
000148_H	PTMR07 [R] 11111111 11111111		PCSR07 [W] XXXXXXXX XXXXXXXX		PPG 7
$00014C_H$	PDUT07 [W] XXXXXXXX XXXXXXXX		PCNH07 [R/W] 0000000 -	PCNL07 [R/W] 000000 - 0	
000150_H	PTMR08 [R] 11111111 11111111		PCSR08 [W] XXXXXXXX XXXXXXXX		PPG 8
000154_H	PDUT08 [W] XXXXXXXX XXXXXXXX		PCNH08 [R/W] 0000000 -	PCNL08 [R/W] 000000 - 0	
000158_H	PTMR09 [R] 11111111 11111111		PCSR09 [W] XXXXXXXX XXXXXXXX		PPG 9
$00015C_H$	PDUT09 [W] XXXXXXXX XXXXXXXX		PCNH09 [R/W] 0000000 -	PCNL09 [R/W] 000000 - 0	

	Register				
Address	**+1**	**+2**	**+3**	**+4**	**Block**
000440_H	ICR00 [R/W] - - - 11111	ICR01 [R/W] - - - 11111	ICR02 [R/W] - - - 11111	ICR03 [R/W] - - - 11111	Interrupt Control register
000444_H	ICR04 [R/W] - - - 11111	ICR05 [R/W] - - - 11111	ICR06 [R/W] - - - 11111	ICR07 [R/W] - - - 11111	
000448_H	ICR08 [R/W] - - - 11111	ICR09 [R/W] - - - 11111	ICR10 [R/W] - - - 11111	ICR11 [R/W] - - - 11111	
$00044C_H$	ICR12 [R/W] - - - 11111	ICR13 [R/W] - - - 11111	ICR14 [R/W] - - - 11111	ICR15 [R/W] - - - 11111	
000450_H	ICR16 [R/W] - - - 11111	ICR17 [R/W] - - - 11111	ICR18 [R/W] - - - 11111	ICR19 [R/W] - - - 11111	
000454_H	ICR20 [R/W] - - - 11111	ICR21 [R/W] - - - 11111	ICR22 [R/W] - - - 11111	ICR23 [R/W] - - - 11111	
000458_H	ICR24 [R/W] - - - 11111	ICR25 [R/W] - - - 11111	ICR26 [R/W] - - - 11111	ICR27 [R/W] - - - 11111	
$00045C_H$	ICR28 [R/W] - - - 11111	ICR29 [R/W] - - - 11111	ICR30 [R/W] - - - 11111	ICR31 [R/W] - - - 11111	
000460_H	ICR32 [R/W] - - - 11111	ICR33 [R/W] - - - 11111	ICR34 [R/W] - - - 11111	ICR35 [R/W] - - - 11111	
000464_H	ICR36 [R/W] - - - 11111	ICR37 [R/W] - - - 11111	ICR38 [R/W] - - - 11111	ICR39 [R/W] - - - 11111	
000468_H	ICR40 [R/W] - - - 11111	ICR41 [R/W] - - - 11111	ICR42 [R/W] - - - 11111	ICR43 [R/W] - - - 11111	
$00046C_H$	ICR44 [R/W] - - - 11111	ICR45 [R/W] - - - 11111	ICR46 [R/W] - - - 11111	ICR47 [R/W] - - - 11111	
000470_H	ICR48 [R/W] - - - 11111	ICR49 [R/W] - - - 11111	ICR50 [R/W] - - - 11111	ICR51 [R/W] - - - 11111	
000474_H	ICR52 [R/W] - - - 11111	ICR53 [R/W] - - - 11111	ICR54 [R/W] - - - 11111	ICR55 [R/W] - - - 11111	
000478_H	ICR56 [R/W] - - - 11111	ICR57 [R/W] - - - 11111	ICR58 [R/W] - - - 11111	ICR59 [R/W] - - - 11111	
$00047C_H$	ICR60 [R/W] - - - 11111	ICR61 [R/W] - - - 11111	ICR62 [R/W] - - - 11111	ICR63 [R/W] - - - 11111	
000480_H	RSRR [R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] 00XXX – 00	CTBR [W] XXXXXXXX	Clock Control Unit
000484_H	CLKR [R/W] ---- 0000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488_H	Reserved				Reserved
$00048C_H$	PLLDIVM [R/W] - - - - 0000	PLLDIVN [R/W] - - 000000	PLLDIVG [R/W] - - - - 0000	PLLMULG [W] 00000000	PLL Clock Gear Unit
000490_H	PLLCTRL [R/W] - - - - 0000	Reserved			
000494_H	OSCC1 [R/W] - - - - - 010	OSCS1 [R/W] 00001111	OSCC2 [R/W] - - - - - 010	OSCS2 [R/W] 00001111	Main/Sub Oscillator Control
000498_H	PORTEN [R/W] - - - - - - 00	Reserved			Port Input Enable Control
$00049C_H$	Reserved				Reserved

	Register				
Address	**+1**	**+2**	**+3**	**+4**	**Block**
$000EC0_H$	PPER00 [R/W] 00000000	PPER01 [R/W] 00000000	PPER02 [R/W] 00000000	PPER03 [R/W] 00000000	Port Pull-Up/Down Enable register
$000EC4_H$	PPER04 [R/W] - - - - 0000	PPER05 [R/W] 00000000	PPER06 [R/W] 00000000	PPER07 [R/W] 00000000	
$000EC8_H$	PPER08 [R/W] 00000000	PPER09 [R/W] 00000000	PPER10 [R/W] - 0000000	PPER11 [R/W] - - - - - - 00	
$000ECC_H$	Reserved	PPER13 [R/W] 00000000	PPER14 [R/W] 00000000	PPER15 [R/W] 00000000	
$000ED0_H$	PPER16 [R/W] 00000000	PPER17 [R/W] 00000000	PPER18 [R/W] - 000 - 000	PPER19 [R/W] - 000 - 000	
$000ED4_H$	PPER20 [R/W] - 000 - 000	PPER21 [R/W] - 000 - 000	PPER22 [R/W] 00000000	PPER23 [R/W] 00000000	
$000ED8_H$	PPER24 [R/W] 00000000	Reserved	PPER26 [R/W] 00000000	PPER27 [R/W] 00000000	
$000EDC_H$	PPER28 [R/W] 00000000	PPER29 [R/W] 00000000	Reserved		
$000EE0_H$ - $000EFC_H$	Reserved				Reserved
$000F00_H$	PPCR00 [R/W] 11111111	PPCR01 [R/W] 11111111	PPCR02 [R/W] 11111111	PPCR03 [R/W] 11111111	Port Pull-Up/Down Control register
$000F04_H$	PPCR04 [R/W] - - - - 1111	PPCR05 [R/W] 11111111	PPCR06 [R/W] 11111111	PPCR07 [R/W] 11111111	
$000F08_H$	PPCR08 [R/W] 11111111	PPCR09 [R/W] 11111111	PPCR10 [R/W] - 1111111	PPCR11 [R/W] - - - - - - 11	
$000F0C_H$	Reserved	PPCR13 [R/W] 11111111	PPCR14 [R/W] 11111111	PPCR15 [R/W] 11111111	
$000F10_H$	PPCR16 [R/W] 11111111	PPCR17 [R/W] 11111111	PPCR18 [R/W] - 111 - 111	PPCR19 [R/W] - 111 - 111	
$000F14_H$	PPCR20 [R/W] - 111 - 111	PPCR21 [R/W] - 111 - 111	PPCR22 [R/W] 11111111	PPCR23 [R/W] 11111111	
$000F18_H$	PPCR24 [R/W] 11111111	Reserved	PPCR26 [R/W] 11111111	PPCR27 [R/W] 11111111	
$000F1C_H$	PPCR28 [R/W] 11111111	PPCR29 [R/W] 11111111	Reserved		
$000F20_H$ - $000FFC_H$	Reserved				Reserved

32bit read/write	dat[31:0]				dat[31:0]				
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
200000_H to $21FFFF_H$	SA36 (64KB)				SA37 (64KB)				ROMS10
220000_H to $23FFFF_H$	SA38 (64KB)				SA39 (64KB)				
240000_H to $243FFF_H$	SA0 (8KB)				SA1 (8KB)				
244000_H to $247FFF_H$	SA2 (8KB)				SA3 (8KB)				
248000_H to $24BFFF_H$	SA4 (8KB)				SA5 (8KB)				
$24C000_H$ to $24FFFF_H$	SA6 (8KB)				SA7 (8KB)				
250000_H to $27FFFF_H$	Reserved								
280000_H to $2FFFF8_H$	External Bus Area								ROMS11
300000_H to $37FFF8_H$									ROMS12
380000_H to $3FFFF8_H$									ROMS13
400000_H to $47FFF8_H$									ROMS14
480000_H to $4FFFF8_H$									ROMS15

Note: Write operations to address $0FFFF8_H$ and $0FFFFC_H$ are not possible. When reading these addresses, the values shown above will be read.

14.2 Clock Modulator Settings

The following table shows all possible settings for the Clock Modulator in a base clock frequency range from 32MHz up to 88MHz.

If Fmax exceeds 88MHz the core supply voltage needs to be set to 1.9V. Please refer to flash access time settings (section 2.3.2.2) to setup the correct voltage according to Fmax in the table below.

The Flash access time settings need to be adjusted according to Fmax while the PLL and clockgear settings should be set according to base clock frequency.

Table 6. Clock Modulator settings, frequency range and supported supply voltage

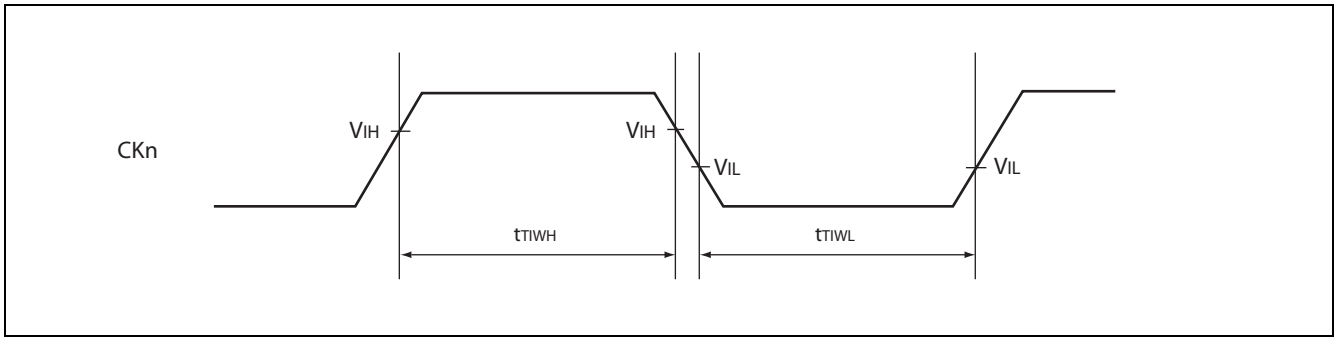
Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	3	026F	88	79.5	98.5	
1	3	026F	84	76.1	93.8	
1	3	026F	80	72.6	89.1	
1	5	02AE	80	68.7	95.8	
2	3	046E	80	68.7	95.8	
1	3	026F	76	69.1	84.5	
1	5	02AE	76	65.3	90.8	
1	7	02ED	76	62	98.1	
2	3	046E	76	65.3	90.8	
3	3	066D	76	62	98.1	
1	3	026F	72	65.5	79.9	
1	5	02AE	72	62	85.8	
1	7	02ED	72	58.8	92.7	
2	3	046E	72	62	85.8	
3	3	066D	72	58.8	92.7	
1	3	026F	68	62	75.3	
1	5	02AE	68	58.7	80.9	
1	7	02ED	68	55.7	87.3	
1	9	032C	68	53	95	
2	3	046E	68	58.7	80.9	
2	5	04AC	68	53	95	
3	3	066D	68	55.7	87.3	
4	3	086C	68	53	95	
1	3	026F	64	58.5	70.7	
1	5	02AE	64	55.3	75.9	
1	7	02ED	64	52.5	82	
1	9	032C	64	49.9	89.1	
1	11	036B	64	47.6	97.6	

15.7.5 Free-Run Timer Clock

($V_{DD}5$ = 3.0 V to 5.5 V, V_{SS5} = AV_{SS5} = 0 V, T_A = − 40 °C to + 125 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	CKn	–	$4t_{CLKP}$	–	ns

Note: t_{CLKP} is the cycle time of the peripheral clock.

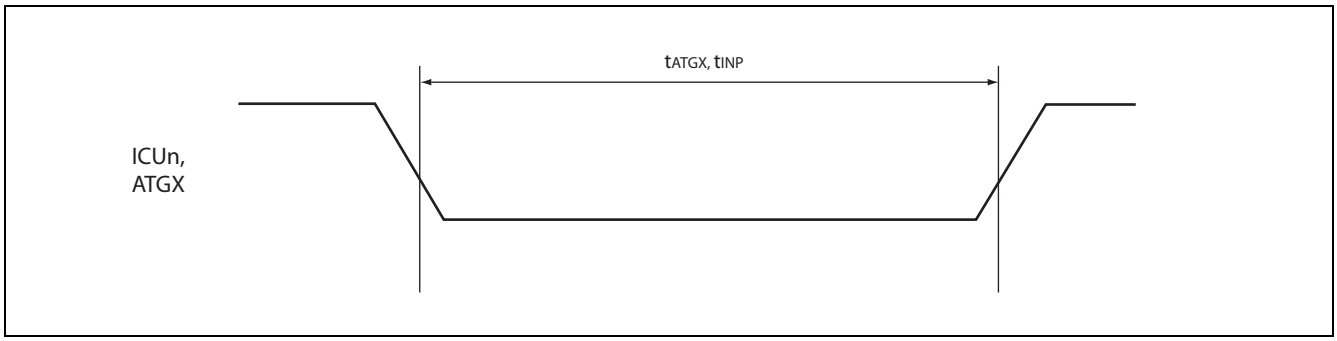


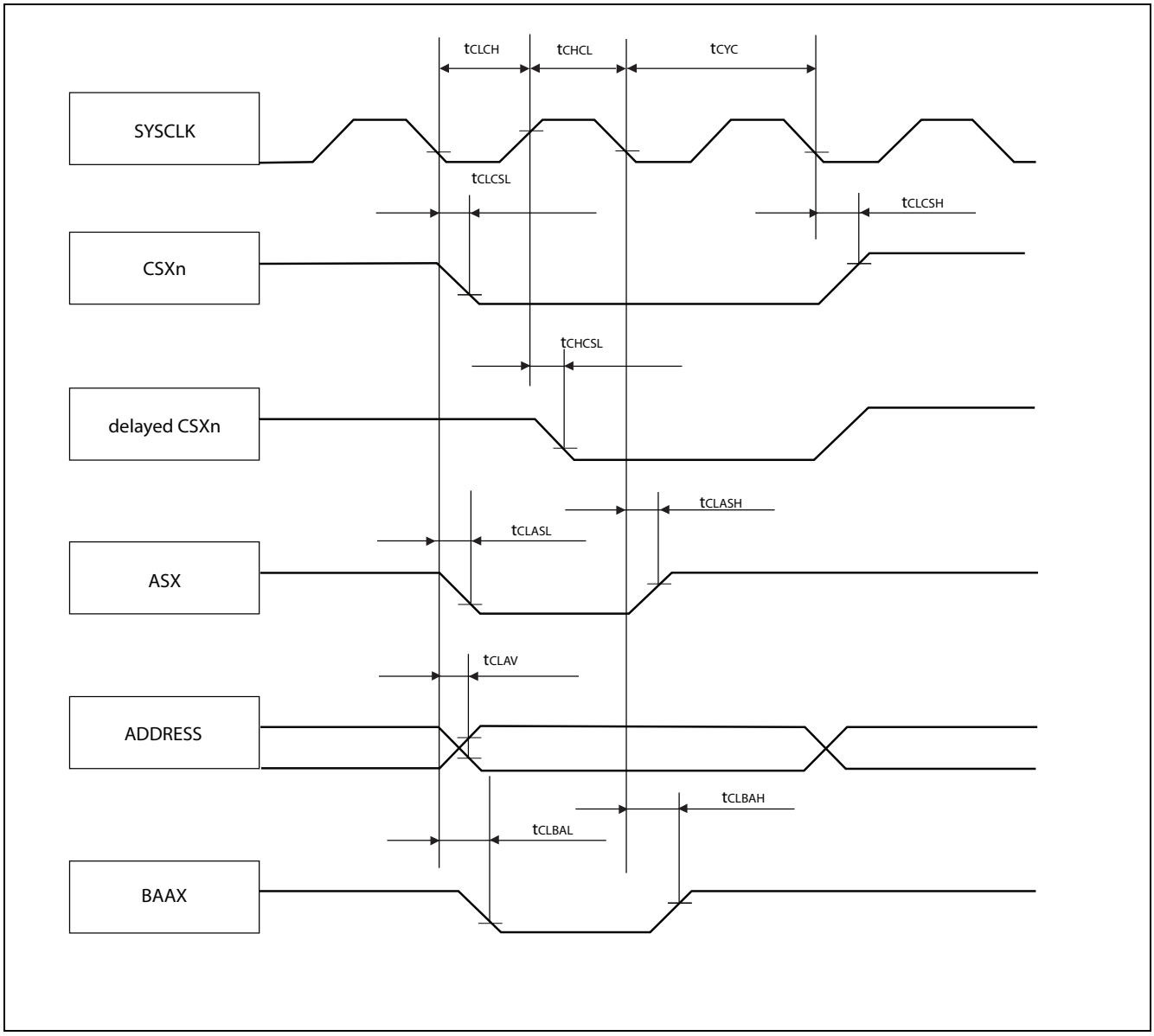
15.7.6 Trigger Input Timing

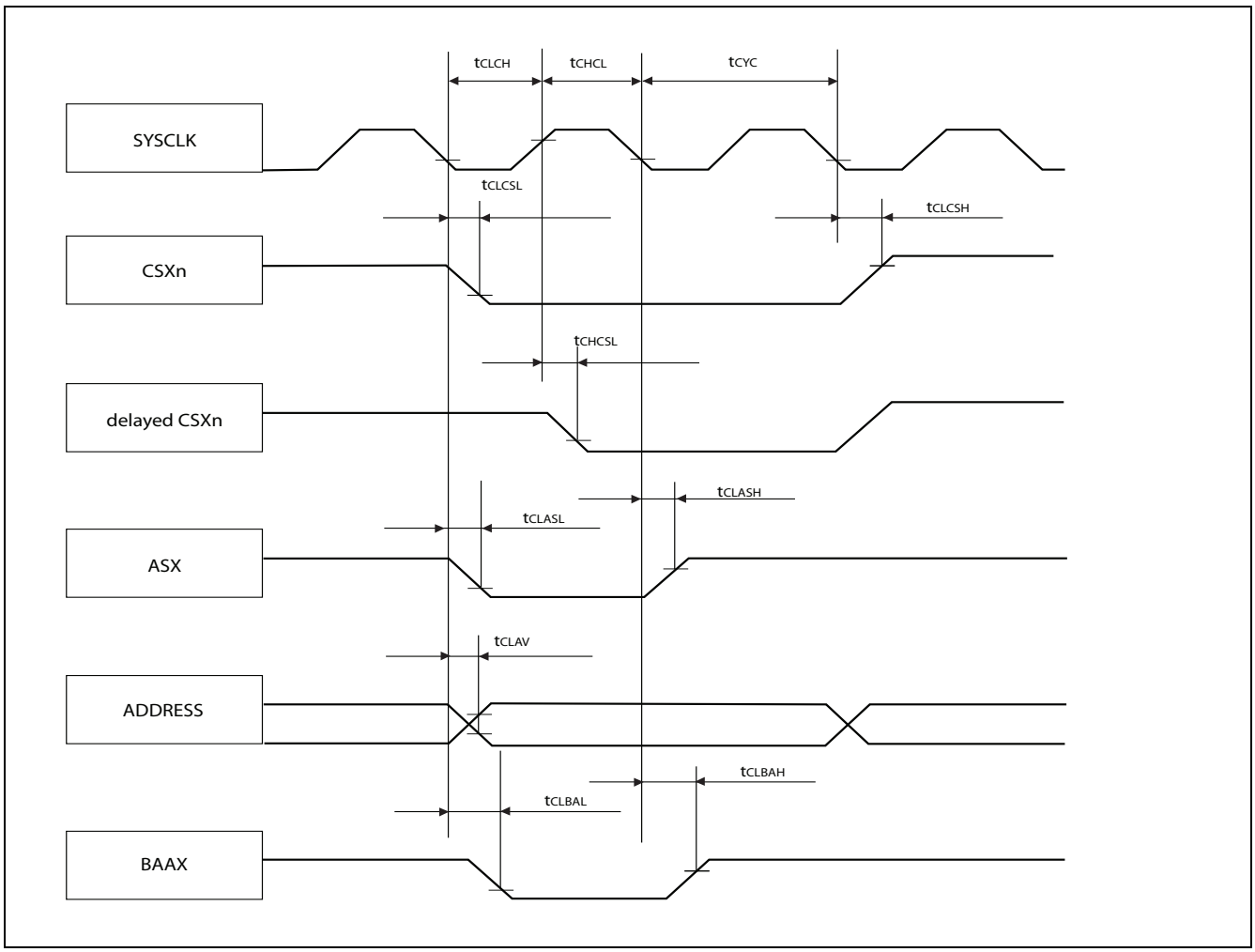
($V_{DD}5$ = 3.0 V to 5.5 V, V_{SS5} = AV_{SS5} = 0 V, T_A = − 40 °C to + 125 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input capture input trigger	t_{INP}	ICUn	–	$5t_{CLKP}$	–	ns
A/D converter trigger	t_{ATGX}	ATGX	–	$5t_{CLKP}$	–	ns

Note: t_{CLKP} is the cycle time of the peripheral clock.



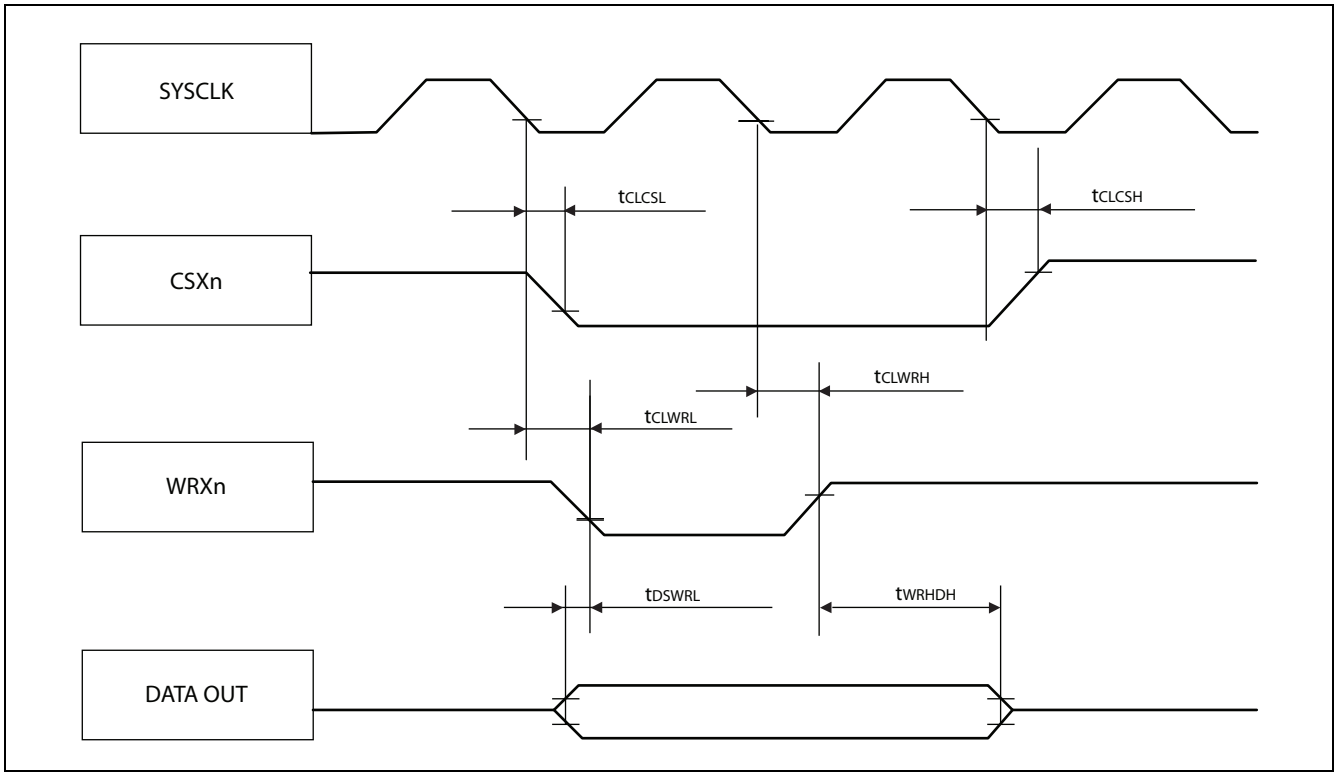

tCLCH
tCHCL
tCYC
SYSCLK
tCLCSL
tCLCSH
CSXn
tCHCSL
delayed CSXn
tCLASH
tCLASL
ASX
tCLAV
ADDRESS
tCLBAH
tCLBAL
BAAX


tCLCH
tCHCL
tCYC
SYSCLK
tCLCSL
tCLCSH
CSXn
tCHCSL
delayed CSXn
tCLASH
tCLASL
ASX
tCLAV
ADDRESS
tCLBAH
tCLBAL
BAAX

15.7.8.5 Synchronous Write Access - No Byte Control Type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = − 40 °C to + 125 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↓ to WRXn delay time	t_{CLWRL}	SYSCLK WRXn	–	5	ns
	t_{CLWRH}		– 1	–	ns
Data valid to WRXn ↓ setup time	t_{DSWRL}	WRXn D31 to D0	– 11	–	ns
WRXn ↑ to Data valid hold time	t_{WRHDH}	WRXn D31 to D0	t_{CLKT} – 13	–	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	–	5	ns
	t_{CLCSH}		–	6	ns

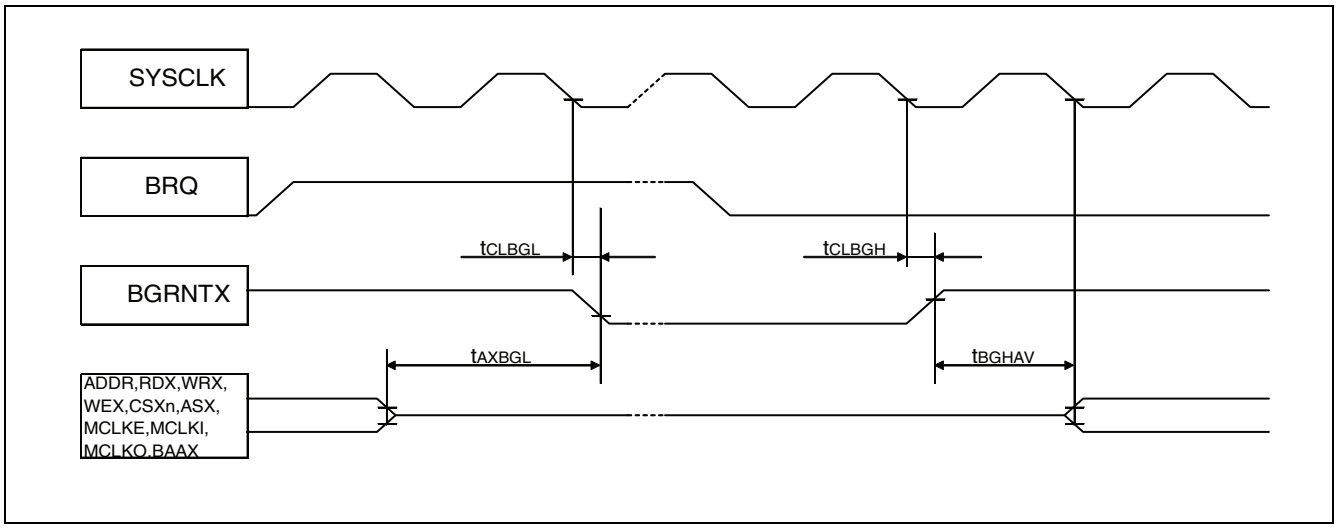


15.7.8.9 Bus Hold Timing

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = − 40 °C to + 125 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↓ to BGRNTX delay time	t_{CLBGL}	SYSCLK BGRNTX	–	5	ns
	t_{CLBGH}		–	6	ns
Bus HIZ to BGRNTX ↓	t_{AXBGL}	BGRNTX MCLK* A0 to An RDX, ASX WRXn,WEX CSXn,BAAX	t_{CLKT} + 2	–	ns
BGRNTX ↑ to Bus drive	t_{BGHAV}		t_{CLKT} − 2	–	ns

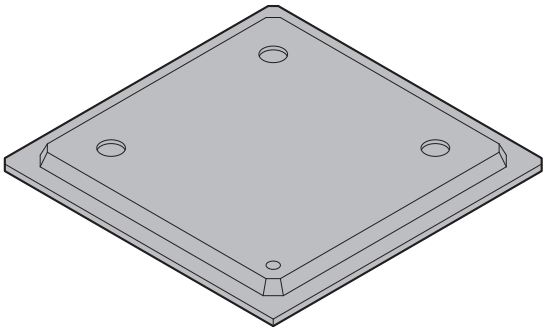
Note: BRQ must be kept High until the bus is granted (this is acknowledged by the falling edge of BGRNTX). It must be kept High as long as the bus shall be hold.After releasing the bus (BRQ set to Low) this is acknowledged by the rising edge of BGRNTX.



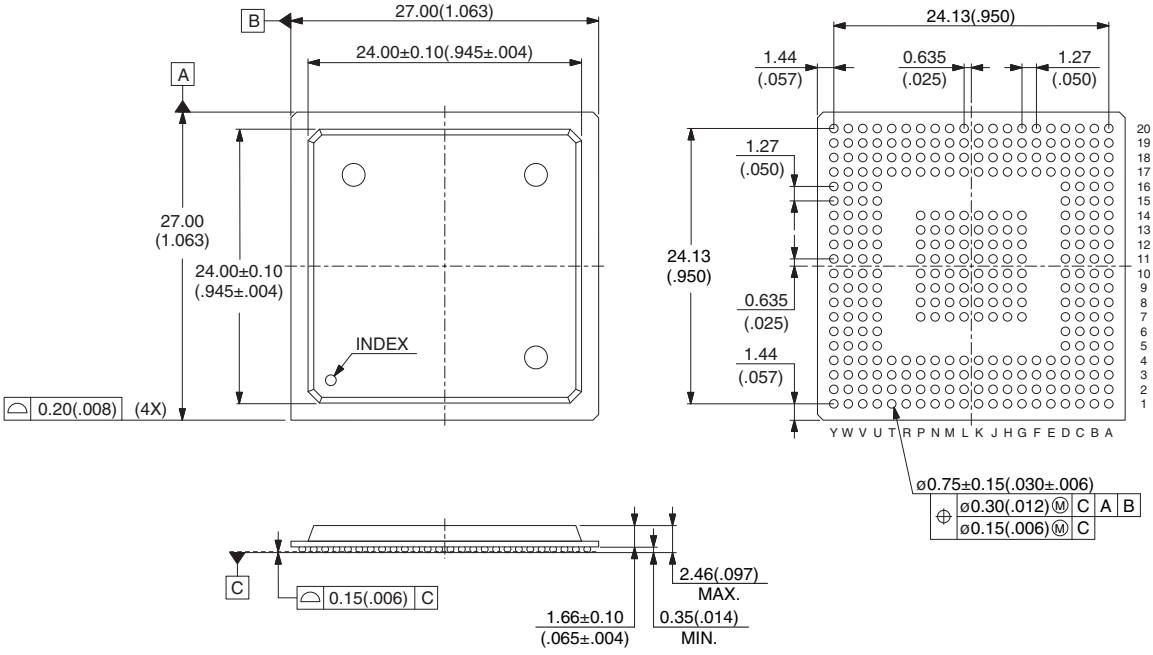
16. Ordering Information

Part number	Package	Remarks
MB91F469GAPB-GS	320-pin plastic BGA (BGA-320P-M06)	not recommended
MB91F469GBPB-GS		not recommended
MB91F469GBPB-GSE1		

17. Package Dimension

320-pin plastic PBGA		
	Lead pitch	1.27 mm
	Package width × package length	27.00 mm × 27.00 mm
	Lead shape	Ball
	Sealing method	Plastic mold
	Mounting height	2.46 mm Max
	Weight	2.90 g
(BGA-320P-M06)		

320-pin plastic PBGA
(BGA-320P-M06)



©2006-2008 FUJITSU MICROELECTRONICS LIMITED BGA320006S-c-2-2

Dimensions in mm (inches).
Note: The values in parentheses are reference values.