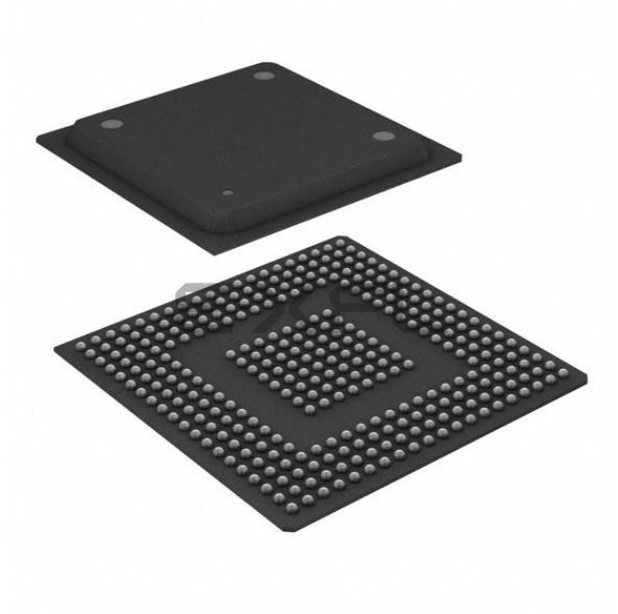

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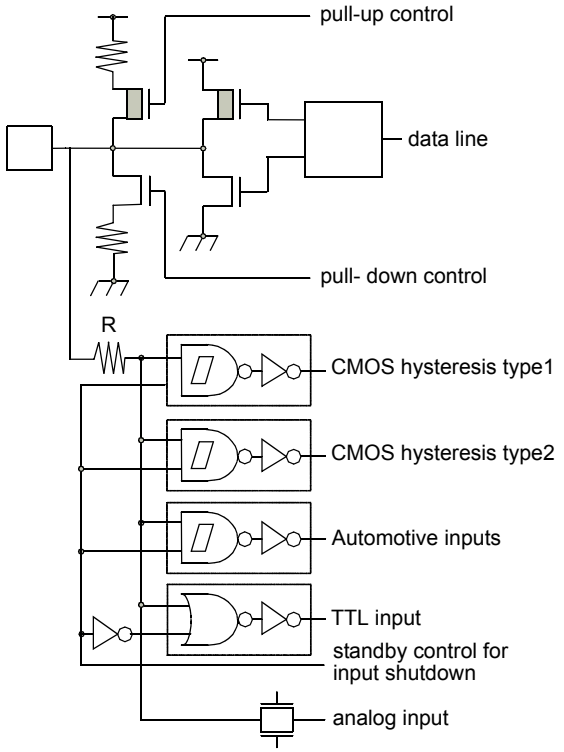
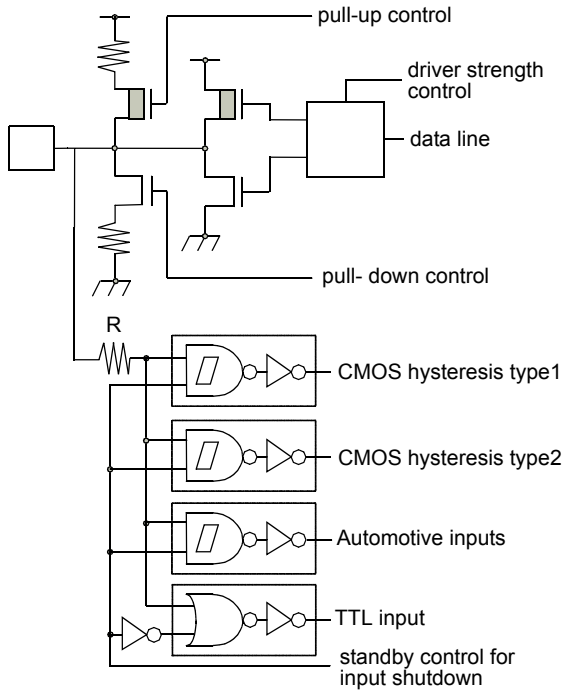
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, WDT
Number of I/O	205
Program Memory Size	2.112MB (2.112M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	112K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	320-BBGA
Supplier Device Package	320-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f469gbpb-gs-k6

Type	Circuit	Remarks
D		CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input
E		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA, and I_{OL} = 30mA, I_{OH} = -30mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.

8. CPU and Control Unit

The FR family CPU is a high performance core that is designed based on the RISC architecture with advanced instructions for embedded applications.

8.1 Features

■ Adoption of RISC architecture
Basic instruction: 1 instruction per cycle

■ General-purpose registers: 32-bit × 16 registers

■ 4 Gbytes linear memory space

■ Multiplier installed
32-bit × 32-bit multiplication: 5 cycles
16-bit × 16-bit multiplication: 3 cycles

■ Enhanced interrupt processing function
Quick response speed (6 cycles)
Multiple-interrupt support
Level mask function (16 levels)

■ Enhanced instructions for I/O operation
Memory-to-memory transfer instruction
Bit processing instruction

■ Basic instruction word length: 16 bits

■ Low-power consumption
Sleep mode/stop mode

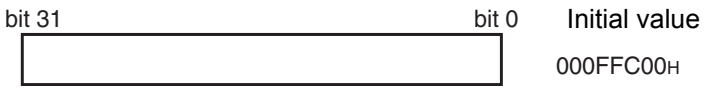
8.2 Internal Architecture

■ The FR family CPU uses the Harvard architecture in which the instruction bus and data bus are independent of each other.

■ A 32-bit ↔ 16-bit buffer is connected to the 32-bit bus (D-bus) to provide an interface between the CPU and peripheral resources.

■ A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus to provide an interface between the CPU and the bus controller.

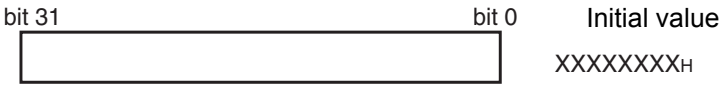
8.4.7 TBR (Table Base Register)



The table base register stores the starting address of the vector table used in EIT processing.

The initial value at reset is $000FFC00_H$.

8.4.8 RP (Return Pointer)



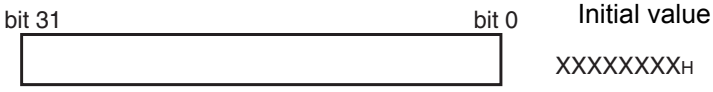
The return pointer stores the address for return from subroutines.

During execution of a CALL instruction, the PC value is transferred to this RP register.

During execution of a RET instruction, the contents of the RP register are transferred to PC.

The initial value at reset is undefined.

8.4.9 USP (User Stack Pointer)

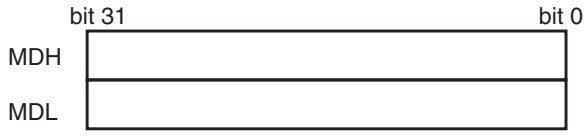


The user stack pointer, when the S flag is “1”, this register functions as the R15 register.

■ The USP register can also be explicitly specified.
The initial value at reset is undefined.

■ This register cannot be used with RETI instructions.

8.4.10 Multiply & divide registers



These registers are for multiplication and division, and are each 32 bits in length.

The initial value at reset is undefined.

9.4.2 Pin Connections in Parallel Programming Mode

Resetting after setting the MD[2:0] pins to [111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to General Purpose Ports. Please see table below for signal mapping.

In this mode, the Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the 16.5 Mbits Flash memory's Auto Algorithms are available.

Table 1. Correspondence between MBM29LV400TC and Flash Memory Control Signals

MBM29LV400TC External pins	FR-CPU mode	MB91F469Gx external pins			Comment
		Flash memory mode	Normal function	Pin number	
–	INITX	–	INITX	U16 (230)	
RESET	–	FRSTX	P00_6	Y12 (31)	
–	–	MD_2	MD_2	V15 (172)	Set to '1'
–	–	MD_1	MD_1	V16 (173)	Set to '1'
–	–	MD_0	MD_0	V17 (174)	Set to '1'
RY/BY	FMCS:RDY bit	RY/BYX	P00_0	W10 (102)	
BYTE	Internally fixed to 'H'	BYTEX	P00_2	U11 (225)	
WE	Internal control signal + control via interface circuit	WEX	P01_2	Y8 (27)	
OE		OEX	P01_1	W8 (100)	
CE		CEX	P01_0	V8 (165)	
–		ATDIN	P01_4	V9 (166)	Set to '0'
–		EQIN	P01_3	U9 (233)	Set to '0'
–		TESTX	P00_3	V11 (168)	Set to '1'
–		RDYI	P00_1	Y10 (29)	Set to '0'
A-1	Internal address bus	FA0	P14_6	A8 (70)	Set to '0'
A0 to A7		FA1 to FA8	P16_0 to P16_7	0: C8 (200) 1: A7(71), 2: B7(140), 3: C7(201), 4: D7(254), 5: A6(72), 6: B6(141), 7: C6(202)	

	Register				
Address	**+1**	**+2**	**+3**	**+4**	**Block**
000104_H	GCN11 [R/W] 00110010 00010000		Reserved	GCN21 [R/W] - - - - 0000	PPG Control 4-7
000108_H	GCN12 [R/W] 00110010 00010000		Reserved	GCN22 [R/W] - - - - 0000	PPG Control 8-11
$00010C_H$	Reserved				Reserved
000110_H	PTMR00 [R] 11111111 11111111		PCSR00 [W] XXXXXXXX XXXXXXXX		PPG 0
000114_H	PDUT00 [W] XXXXXXXX XXXXXXXX		PCNH00 [R/W] 0000000 -	PCNL00 [R/W] 000000 - 0	
000118_H	PTMR01 [R] 11111111 11111111		PCSR01 [W] XXXXXXXX XXXXXXXX		PPG 1
$00011C_H$	PDUT01 [W] XXXXXXXX XXXXXXXX		PCNH01 [R/W] 0000000 -	PCNL01 [R/W] 000000 - 0	
000120_H	PTMR02 [R] 11111111 11111111		PCSR02 [W] XXXXXXXX XXXXXXXX		PPG 2
000124_H	PDUT02 [W] XXXXXXXX XXXXXXXX		PCNH02 [R/W] 0000000 -	PCNL02 [R/W] 000000 - 0	
000128_H	PTMR03 [R] 11111111 11111111		PCSR03 [W] XXXXXXXX XXXXXXXX		PPG 3
$00012C_H$	PDUT03 [W] XXXXXXXX XXXXXXXX		PCNH03 [R/W] 0000000 -	PCNL03 [R/W] 000000 - 0	
000130_H	PTMR04 [R] 11111111 11111111		PCSR04 [W] XXXXXXXX XXXXXXXX		PPG 4
000134_H	PDUT04 [W] XXXXXXXX XXXXXXXX		PCNH04 [R/W] 0000000 -	PCNL04 [R/W] 000000 - 0	
000138_H	PTMR05 [R] 11111111 11111111		PCSR05 [W] XXXXXXXX XXXXXXXX		PPG 5
$00013C_H$	PDUT05 [W] XXXXXXXX XXXXXXXX		PCNH05 [R/W] 0000000 -	PCNL05 [R/W] 000000 - 0	
000140_H	PTMR06 [R] 11111111 11111111		PCSR06 [W] XXXXXXXX XXXXXXXX		PPG 6
000144_H	PDUT06 [W] XXXXXXXX XXXXXXXX		PCNH06 [R/W] 0000000 -	PCNL06 [R/W] 000000 - 0	
000148_H	PTMR07 [R] 11111111 11111111		PCSR07 [W] XXXXXXXX XXXXXXXX		PPG 7
$00014C_H$	PDUT07 [W] XXXXXXXX XXXXXXXX		PCNH07 [R/W] 0000000 -	PCNL07 [R/W] 000000 - 0	
000150_H	PTMR08 [R] 11111111 11111111		PCSR08 [W] XXXXXXXX XXXXXXXX		PPG 8
000154_H	PDUT08 [W] XXXXXXXX XXXXXXXX		PCNH08 [R/W] 0000000 -	PCNL08 [R/W] 000000 - 0	
000158_H	PTMR09 [R] 11111111 11111111		PCSR09 [W] XXXXXXXX XXXXXXXX		PPG 9
$00015C_H$	PDUT09 [W] XXXXXXXX XXXXXXXX		PCNH09 [R/W] 0000000 -	PCNL09 [R/W] 000000 - 0	

	Register				
Address	**+1**	**+2**	**+3**	**+4**	**Block**
000160_H	PTMR10 [R] 11111111 11111111		PCSR10 [W] XXXXXXXX XXXXXXXX		PPG 10
000164_H	PDUT10 [W] XXXXXXXX XXXXXXXX		PCNH10 [R/W] 0000000 -	PCNL10 [R/W] 000000 - 0	
000168_H	PTMR11 [R] 11111111 11111111		PCSR11 [W] XXXXXXXX XXXXXXXX		PPG 11
$00016C_H$	PDUT11 [W] XXXXXXXX XXXXXXXX		PCNH11 [R/W] 0000000 -	PCNL11 [R/W] 000000 - 0	
000170_H	P0TMCSRH [R/W] - 0 - 000 - 0	P0TMCSRL [R/W] - - - 00000	P1TMCSRH [R/W] - 0 - 000 - 0	P1TMCSRL [R/W] - - - 00000	Pulse Frequency Modulator
000174_H	P0TMRLR [W] XXXXXXXX XXXXXXXX		P0TMR [R] XXXXXXXX XXXXXXXX		
000178_H	P1TMRLR [W] XXXXXXXX XXXXXXXX		P1TMR [R] XXXXXXXX XXXXXXXX		
$00017C_H$	Reserved				Reserved
000180_H	Reserved	ICS01 [R/W] 00000000	Reserved	ICS23 [R/W] 00000000	Input Capture 0-3
000184_H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188_H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		
$00018C_H$	OCS01 [R/W] - - - 0 - - 00 0000 - - 00		OCS23 [R/W] - - - 0 - - 00 0000 - - 00		Output Compare 0-3
000190_H	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
000194_H	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
000198_H	SGCRH [R/W] 0000 - - 00	SGCRL [R/W] - - 0 - - 000	SGFR [R/W, R] XXXXXXXX XXXXXXXX		Sound Generator
$00019C_H$	SGAR [R/W] 00000000	Reserved	SGTR [R/W] XXXXXXXX	SGDR [R/W] XXXXXXXX	
$0001A0_H$	ADERH [R/W] 00000000 00000000		ADERL [R/W] 00000000 00000000		A/D Converter
$0001A4_H$	ADCS1 [R/W] 00000000	ADCS0 [R/W] 00000000	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
$0001A8_H$	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] - - - 00000	ADECH [R/W] - - - 00000	
$0001AC_H$	Reserved	ACSR0 [R/W] 011XXX00	Reserved	ACSR1 [R/W] 011XXX00	Alarm Comparator 0-1
$0001B0_H$	TMRLRC0 [W] XXXXXXXX XXXXXXXX		TMRC0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0 (PPG 0-1)
$0001B4_H$	Reserved		TMCSRCH0 [R/W] - - - 00000	TMCSRCL0 [R/W] 0 - 000000	

	Register				
Address	**+1**	**+2**	**+3**	**+4**	**Block**
000200_H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC 0
000204_H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208_H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC 1
$00020C_H$	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000210_H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC 2
000214_H	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218_H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC 3
$00021C_H$	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000220_H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC 4
000224_H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228_H - $00023C_H$	Reserved				Reserved
000240_H	DMACR [R/W] 00 - - 0000	Reserved			DMAC Control
000244_H - $0002CC_H$	Reserved				Reserved
$0002D0_H$	Reserved	ICS45 [R/W] 00000000	Reserved	ICS67 [R/W] 00000000	Input Capture 4-7
$0002D4_H$	IPCP4 [R] XXXXXXXX XXXXXXXX		IPCP5 [R] XXXXXXXX XXXXXXXX		
$0002D8_H$	IPCP6 [R] XXXXXXXX XXXXXXXX		IPCP7 [R] XXXXXXXX XXXXXXXX		
$0002DC_H$	OCS45 [R/W] - - -0 - -00 0000 - -00		OCS67 [R/W] - - -0 - -00 0000 - -00		Output Compare 4-7
$0002E0_H$	OCCP4 [R/W] XXXXXXXX XXXXXXXX		OCCP5 [R/W] XXXXXXXX XXXXXXXX		
$0002E4_H$	OCCP6 [R/W] XXXXXXXX XXXXXXXX		OCCP7 [R/W] XXXXXXXX XXXXXXXX		
$0002E8_H$ - $0002EC_H$	Reserved				Reserved
$0002F0_H$	TCDT4 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS4 [R/W] 00000000	Free Running Timer 4 (ICU 4-5)
$0002F4_H$	TCDT5 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS5 [R/W] 00000000	Free Running Timer 5 (ICU 6-7)

Address	Register +1	+2	+3	+4	Block
$00F0B0_H$	BAD12 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU ch. 3
$00F0B4_H$	BAD13 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B8_H$	BAD14 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0BC_H$	BAD15 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0C0_H$ - $00FFFC_H$	Reserved				Reserved
010000_H - $013FFC_H$	Cache TAG way 1 (010000_H - $0107FC_H$)				2 Way Set Associative I-Cache 4 KB
014000_H - $017FFC_H$	Cache TAG way 2 (014000_H - $0147FC_H$)				
018000_H - $01BFFC_H$	Cache RAM way 1 (018000_H - $0187FC_H$)				
$01C000_H$ - $01FFFC_H$	Cache RAM way 2 $01C000_H$ - $01C7FC_H$)				
020000_H - $02FFFC_H$	MB91F469Gx D-RAM size is 64 KB (data access is 0 waitcycles)				Data-RAM
030000_H - $037FFC_H$	MB91F469Gx I-/D-RAM size is 32 KB (instruction access is 0 waitcycles, data access is 1 waitcycle)				Instruction/ Data RAM
380000_H - $03FFFC_H$	Reserved				

1. depends on the number of available CAN channels
2. ACR0[11:10] depends on bus width setting in Mode vector fetch information
3. TCR[3:0] INIT value = 0000, keeps value after RST

12.2 Flash Memory and External Bus Area

32bit read/write	dat[31:0]				dat[31:0]				
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
040000_H to $05FFFF_H$	SA8 (64KB)				SA9 (64KB)				ROMS0
060000_H to $07FFFF_H$	SA10 (64KB)				SA11 (64KB)				ROMS1
080000_H to $09FFFF_H$	SA12 (64KB)				SA13 (64KB)				ROMS2
$0A0000_H$ to $0BFFFF_H$	SA14 (64KB)				SA15 (64KB)				ROMS3
$0C0000_H$ to $0DFFFF_H$	SA16 (64KB)				SA17 (64KB)				ROMS4
$0E0000_H$ to $0FFFF4_H$	SA18 (64KB)				SA19 (64KB)				ROMS5
$0FFFF8_H$	FMV [R] $06\ 00\ 00\ 00_H$				FRV [R] $00\ 00\ BF\ F8_H$				
100000_H to $11FFFF_H$	SA20 (64KB)				SA21 (64KB)				ROMS6
120000_H to $13FFFF_H$	SA22 (64KB)				SA23 (64KB)				
140000_H to $15FFFF_H$	SA24 (64KB)				SA25 (64KB)				ROMS7
160000_H to $17FFFF_H$	SA26 (64KB)				SA27 (64KB)				
180000_H to $19FFFF_H$	SA28 (64KB)				SA29 (64KB)				ROMS8
$1A0000_H$ to $1BFFFF_H$	SA30 (64KB)				SA31 (64KB)				
$1C0000_H$ to $1DFFFF_H$	SA32 (64KB)				SA33 (64KB)				ROMS9
$1E0000_H$ to $1FFFFF_H$	SA34 (64KB)				SA35 (64KB)				

13. Interrupt Vector Table

Interrupt	Interrupt number		Interrupt level [1]		Interrupt vector [2]		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
Reset	0	00	–	–	$3FC_H$	$000FFFFC_H$	–
Mode vector	1	01	–	–	$3F8_H$	$000FFFF8_H$	–
System Reserved	2	02	–	–	$3F4_H$	$000FFFF4_H$	–
System Reserved	3	03	–	–	$3F0_H$	$000FFFF0_H$	–
System Reserved	4	04	–	–	$3EC_H$	$000FFFEC_H$	–
CPU supervisor mode (INT #5 instruction) [5]	5	05	–	–	$3E8_H$	$000FFFE8_H$	–
Memory Protection exception [5]	6	06	–	–	$3E4_H$	$000FFFE4_H$	–
System Reserved	7	07	–	–	$3E0_H$	$000FFFE0_H$	–
System Reserved	8	08	–	–	$3DC_H$	$000FFFDC_H$	–
System Reserved	9	09	–	–	$3D8_H$	$000FFFD8_H$	–
System Reserved	10	0A	–	–	$3D4_H$	$000FFFD4_H$	–
System Reserved	11	0B	–	–	$3D0_H$	$000FFFD0_H$	–
System Reserved	12	0C	–	–	$3CC_H$	$000FFFCC_H$	–
System Reserved	13	0D	–	–	$3C8_H$	$000FFFC8_H$	–
Undefined instruction exception	14	0E	–	–	$3C4_H$	$000FFFC4_H$	–
NMI request	15	0F	F_H fixed		$3C0_H$	$000FFFC0_H$	–
External Interrupt 0	16	10	ICR00	440_H	$3BC_H$	$000FFFBC_H$	0, 16
External Interrupt 1	17	11			$3B8_H$	$000FFFB8_H$	1, 17
External Interrupt 2	18	12	ICR01	441_H	$3B4_H$	$000FFFB4_H$	2, 18
External Interrupt 3	19	13			$3B0_H$	$000FFFB0_H$	3, 19
External Interrupt 4	20	14	ICR02	442_H	$3AC_H$	$000FFFAC_H$	20
External Interrupt 5	21	15			$3A8_H$	$000FFFA8_H$	21
External Interrupt 6	22	16	ICR03	443_H	$3A4_H$	$000FFFA4_H$	22
External Interrupt 7	23	17			$3A0_H$	$000FFFA0_H$	23
External Interrupt 8	24	18	ICR04	444_H	$39C_H$	$000FFF9C_H$	–
External Interrupt 9	25	19			398_H	$000FFF98_H$	–
External Interrupt 10	26	1A	ICR05	445_H	394_H	$000FFF94_H$	–
External Interrupt 11	27	1B			390_H	$000FFF90_H$	–
External Interrupt 12	28	1C	ICR06	446_H	$38C_H$	$000FFF8C_H$	–
External Interrupt 13	29	1D			388_H	$000FFF88_H$	–
External Interrupt 14	30	1E	ICR07	447_H	384_H	$000FFF84_H$	–
External Interrupt 15	31	1F			380_H	$000FFF80_H$	–

Interrupt	Interrupt number		Interrupt level [1]		Interrupt vector [2]		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
System Reserved [4]	64	40	(ICR24)	(458_H)	$2FC_H$	$000FFEFC_H$	–
System Reserved[4]	65	41			$2F8_H$	$000FFEF8_H$	–
LIN-USART (FIFO) 4 RX	66	42	ICR25	459_H	$2F4_H$	$000FFEF4_H$	10, 56
LIN-USART (FIFO) 4 TX	67	43			$2F0_H$	$000FFEF0_H$	11, 57
LIN-USART (FIFO) 5 RX	68	44	ICR26	$45A_H$	$2EC_H$	$000FFEEC_H$	12, 58
LIN-USART (FIFO) 5 TX	69	45			$2E8_H$	$000FFEE8_H$	13, 59
LIN-USART (FIFO) 6 RX	70	46	ICR27	$45B_H$	$2E4_H$	$000FFEE4_H$	60
LIN-USART (FIFO) 6 TX	71	47			$2E0_H$	$000FFEE0_H$	61
LIN-USART (FIFO) 7 RX	72	48	ICR28	$45C_H$	$2DC_H$	$000FFEDC_H$	62
LIN-USART (FIFO) 7 TX	73	49			$2D8_H$	$000FFED8_H$	63
I^2C 0 / I^2C 2	74	4A	ICR29	$45D_H$	$2D4_H$	$000FFED4_H$	–
I^2C 1 / I^2C 3	75	4B			$2D0_H$	$000FFED0_H$	–
System Reserved	76	4C	ICR30	$45E_H$	$2CC_H$	$000FFECC_H$	64
System Reserved	77	4D			$2C8_H$	$000FFEC8_H$	65
System Reserved	78	4E	ICR31	$45F_H$	$2C4_H$	$000FFEC4_H$	66
System Reserved	79	4F			$2C0_H$	$000FFEC0_H$	67
System Reserved	80	50	ICR32	460_H	$2BC_H$	$000FFEBC_H$	68
System Reserved	81	51			$2B8_H$	$000FFEB8_H$	69
System Reserved	82	52	ICR33	461_H	$2B4_H$	$000FFEB4_H$	70
System Reserved	83	53			$2B0_H$	$000FFEB0_H$	71
System Reserved	84	54	ICR34	462_H	$2AC_H$	$000FFEAC_H$	72
System Reserved	85	55			$2A8_H$	$000FFEA8_H$	73
System Reserved	86	56	ICR35	463_H	$2A4_H$	$000FFEA4_H$	74
System Reserved	87	57			$2A0_H$	$000FFEA0_H$	75
System Reserved	88	58	ICR36	464_H	$29C_H$	$000FFE9C_H$	76
System Reserved	89	59			298_H	$000FFE98_H$	77
System Reserved	90	5A	ICR37	465_H	294_H	$000FFE94_H$	78
System Reserved	91	5B			290_H	$000FFE90_H$	79
Input Capture 0	92	5C	ICR38	466_H	$28C_H$	$000FFE8C_H$	80
Input Capture 1	93	5D			288_H	$000FFE88_H$	81
Input Capture 2	94	5E	ICR39	467_H	284_H	$000FFE84_H$	82
Input Capture 3	95	5F			280_H	$000FFE80_H$	83

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
5	5	0AA6	32	19.5	89.1	
6	3	0C6A	32	23	52.5	
7	3	0E69	32	22	58.6	
8	3	1068	32	21.1	66.1	
9	3	1267	32	20.3	75.9	
10	3	1466	32	19.5	89.1	

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS5} = AV_{SS5} = 0$ V, $T_A = -40$ °C to + 125 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "L" voltage	V_{ILXDF}	X0	–	V_{SS} – 0.3	–	0.2 · V_{DD}	V	External clock in "Fast Clock Input mode"
Output "H" voltage	V_{OH2}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = – 2mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = – 1.6mA	V_{DD} – 0.5	–	–	V	Driving strength set to 2 mA
	V_{OH5}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = – 5mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = – 3mA	V_{DD} – 0.5	–	–	V	Driving strength set to 5 mA
	V_{OH3}	I^2C outputs	3.0V ≤ V_{DD} ≤ 5.5V, I_{OH} = – 3mA	V_{DD} – 0.5	–	–	V	
Output "L" voltage	V_{OL2}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OL} = + 2mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OL} = + 1.6mA	–	–	0.4	V	Driving strength set to 2 mA
	V_{OL5}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OL} = + 5mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OL} = + 3mA	–	–	0.4	V	Driving strength set to 5 mA
	V_{OL3}	I^2C outputs	3.0V ≤ V_{DD} ≤ 5.5V, I_{OL} = + 3mA	–	–	0.4	V	
Input leakage current	I_{IL}	Pnn_m [1]	3.0V ≤ V_{DD} ≤ 5.5V $V_{SS}5 < V_I < V_{DD}$ T_A=25 °C	– 1	–	+ 1	µA	
			3.0V ≤ V_{DD} ≤ 5.5V $V_{SS}5 < V_I < V_{DD}$ T_A=125 °C	– 3	–	+ 3		

1. Pnn_m includes all GPIO pins. Analog (AN) channels and PullUp/PullDown are disabled.

15.7.7 External Bus AC Timings at $V_{DD}35$ = 4.5 to 5.5 V

■ Conditions during AC measurements
All AC tests were measured under the following conditions:
- ❒ -IO_{drive} = 5 mA
- ❒ -$V_{DD}35$ = 4.5 V to 5.5 V, I_{load} = 5 mA
- ❒ -$V_{SS}5$ = 0 V
- ❒ -Ta = − 40 °C to + 125 °C
- ❒ -C_l = 50 pF
- ❒ -VOL = 0.2 · $V_{DD}35$
- ❒ -VOH = 0.8 · $V_{DD}35$
- ❒ -EPILR = 0, PILR = 1 (Automotive Level = worst case)

15.7.7.1 Basic Timing

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = − 40 °C to + 125 °C)

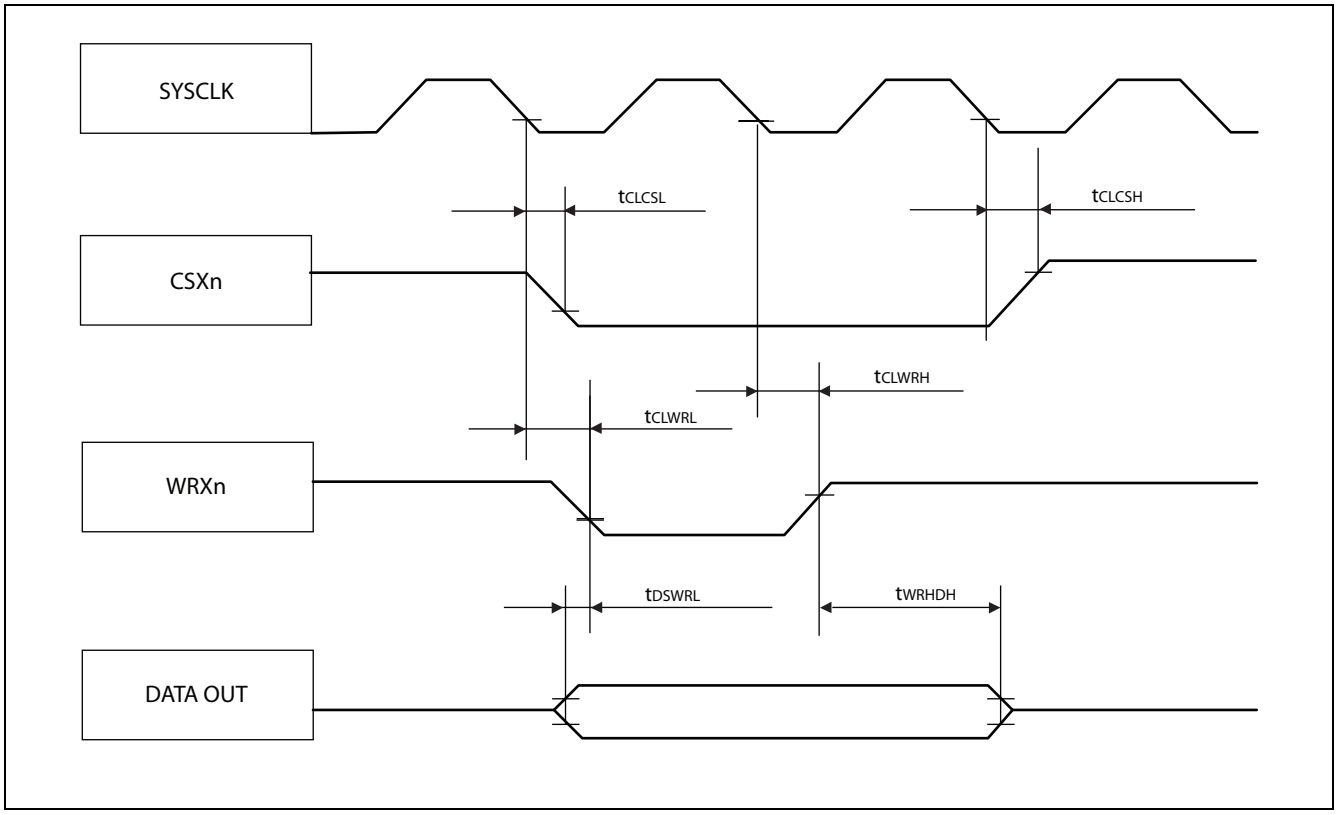
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK	t_{CLCH}	SYSCLK	1/2 · t_{CLKT} − 4	1/2 · t_{CLKT} + 5	ns
	t_{CHCL}		1/2 · t_{CLKT} − 5	1/2 · t_{CLKT} + 4	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	−	9	ns
	t_{CLCSH}		−	8	ns
SYSCLK ↑ to CSXn delay time (Addr → CS delay)	t_{CHCSL}		− 2	8	ns
SYSCLK ↓ to ASX delay time	t_{CLASL}	SYSCLK ASX	−	8	ns
	t_{CLASH}		−	7	ns
SYSCLK ↓ to BAAX delay time	t_{CLBAL}	SYSCLK BAAX	−	5	ns
	t_{CLBAH}		− 2	−	ns
SYSCLK ↓ to Address valid delay time	t_{CLAV}	SYSCLK A27 to A0	−	10	ns

Note: t_{CLKT} is the cycle time of the external bus clock.

15.7.7.5 Synchronous Write Access - No Byte Control Type

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = − 40 °C to + 125 °C)

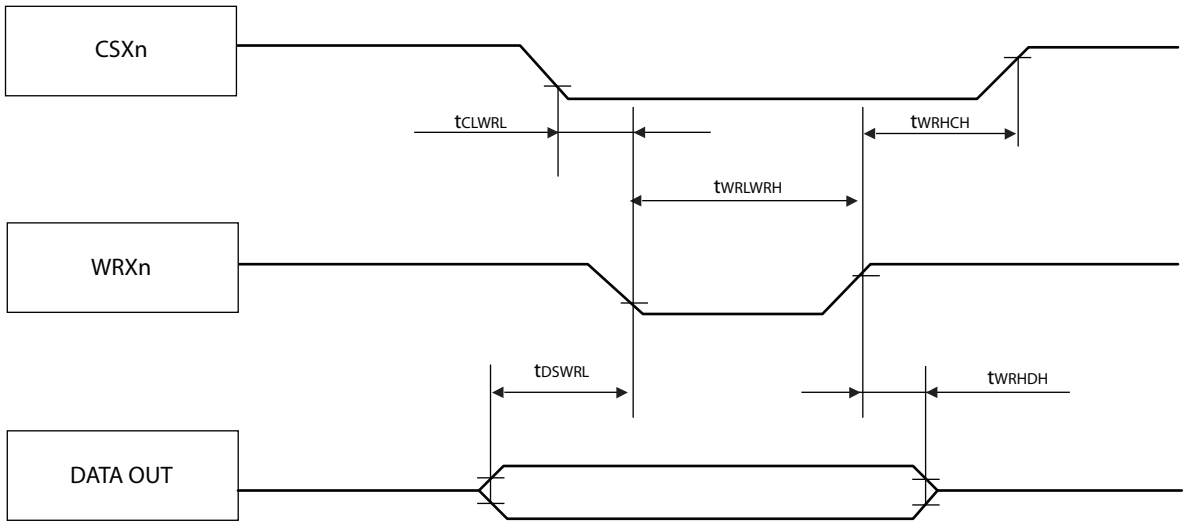
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↓ to WRXn delay time	t_{CLWRL}	SYSCLK WRXn	−	9	ns
	t_{CLWRH}		− 1	−	ns
Data valid to WRXn ↓ setup time	t_{DSWRL}	WRXn D31 to D0	− 6	−	ns
WRXn ↑ to Data valid hold time	t_{WRHDH}	WRXn D31 to D0	t_{CLKT} − 10	−	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	−	9	ns
	t_{CLCSH}		−	8	ns



15.7.7.7 Asynchronous Write Access - No Byte Control Type

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = − 40 °C to + 125 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WRXn ↓ to WRXn ↑ pulse width	t_{WRLWRH}	WRXn	t_{CLKT} − 6	−	ns
Data valid to WRXn ↓ setup time	t^{DSWRL}	WRXn D31 to D0	1/2 · t_{CLKT} − 9	−	ns
WRXn ↑ to Data valid hold time	t_{WRHDH}	WRXn D31 to D0	1/2 · t_{CLKT} − 7	−	ns
WRXn to CSXn delay time	t_{CLWRL}	WRXn CSXn	−	1/2 · t_{CLKT} − 1	ns
	t_{WRHCH}		1/2 · t_{CLKT} + 1	−	ns



15.7.7.11 DMA Transfer

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = − 40 °C to + 125 °C)

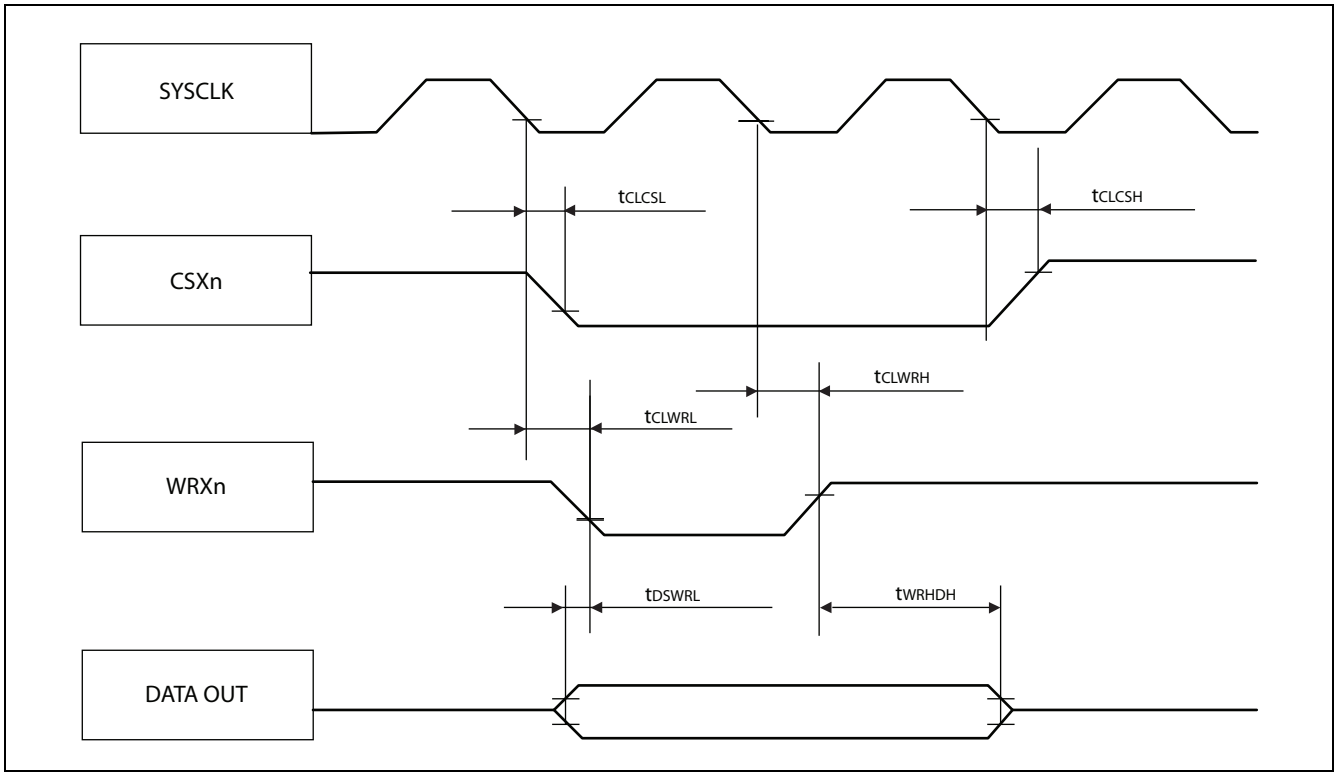
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↓ to DACKX delay time	t_{CLDAL}	SYSCLK DACKXn	−	8	ns
	t_{CLDAH}		−	8	ns
SYSCLK ↓ to DEOP delay time	t_{CLDEL}	SYSCLK DEOPn	−	7	ns
	t_{CLDEH}		−	9	ns
SYSCLK ↑ to DACKX delay time (ADDR → delayed CS)	t_{CHDAL}	SYSCLK DACKXn	− 1	8	ns
SYSCLK ↑ to DEOP delay time (ADDR → delayed CS)	t_{CHDEL}	SYSCLK DEOPn	− 1	8	ns
DREQ setup time	t_{DRQS}	SYSCLK DREQn	19	−	ns
DREQ hold time	t_{DRQH}	SYSCLK DREQn	0	−	ns
DEOTXn setup time	t_{DTXS}	SYSCLK DEOTXn	20	−	ns
DEOTXn hold time	t_{DTXH}	SYSCLK DEOTXn	0	−	ns

Note: DREQ and DEOTX must be applied for at least 5 · t_{CLKT} to ensure that they are really sampled and evaluated.Under best case conditions (DMA not busy) only setup and hold times are required.

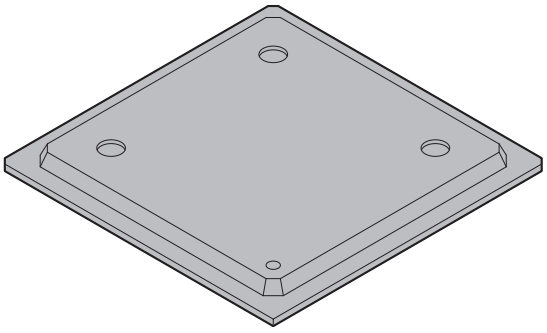
15.7.8.5 Synchronous Write Access - No Byte Control Type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = − 40 °C to + 125 °C)

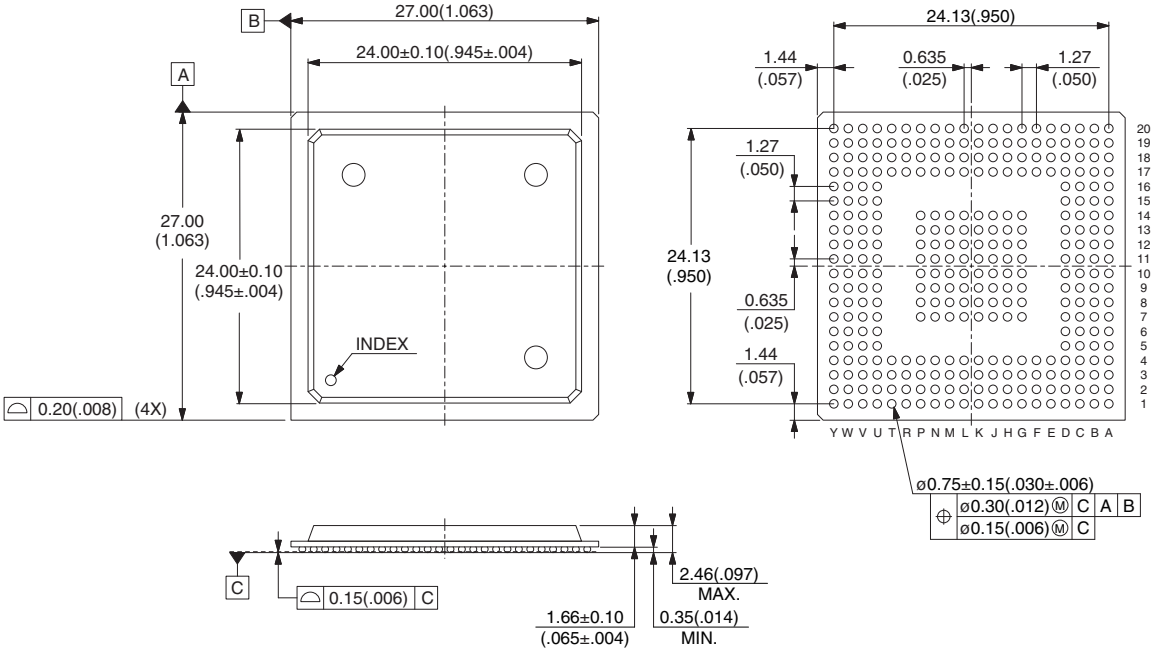
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↓ to WRXn delay time	t_{CLWRL}	SYSCLK WRXn	–	5	ns
	t_{CLWRH}		– 1	–	ns
Data valid to WRXn ↓ setup time	t_{DSWRL}	WRXn D31 to D0	– 11	–	ns
WRXn ↑ to Data valid hold time	t_{WRHDH}	WRXn D31 to D0	t_{CLKT} – 13	–	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	–	5	ns
	t_{CLCSH}		–	6	ns



17. Package Dimension

320-pin plastic PBGA		
	Lead pitch	1.27 mm
	Package width × package length	27.00 mm × 27.00 mm
	Lead shape	Ball
	Sealing method	Plastic mold
	Mounting height	2.46 mm Max
	Weight	2.90 g
(BGA-320P-M06)		

320-pin plastic PBGA
(BGA-320P-M06)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	05/25/2009	Migrated to Cypress and assigned document number 002-04606. No change to document contents or format.
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