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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	PWM, WDT
Number of I/O	13
Program Memory Size	1KB (1K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8e00110hec00tr

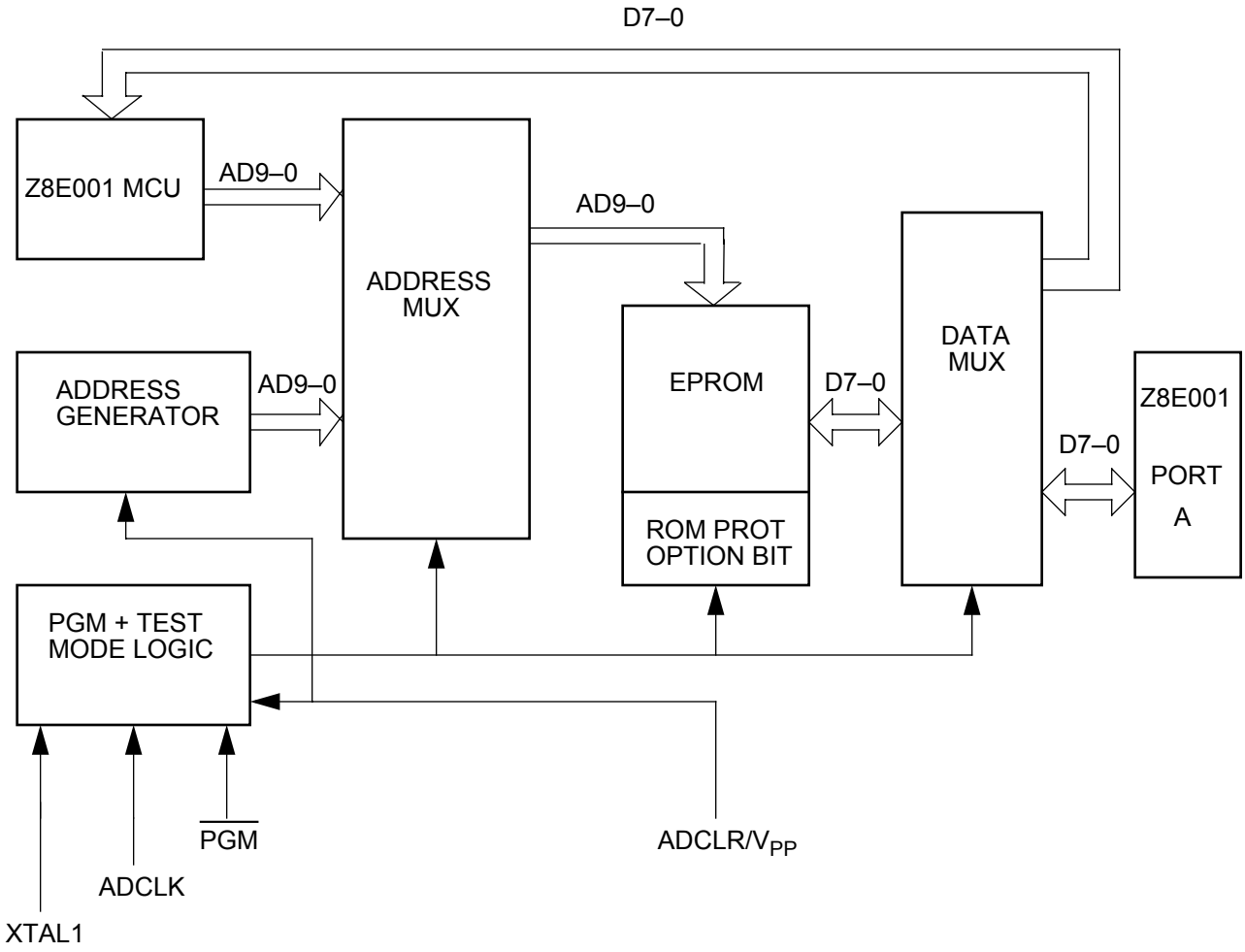


Figure 2. EPROM Programming Mode Block Diagram

PIN DESCRIPTION

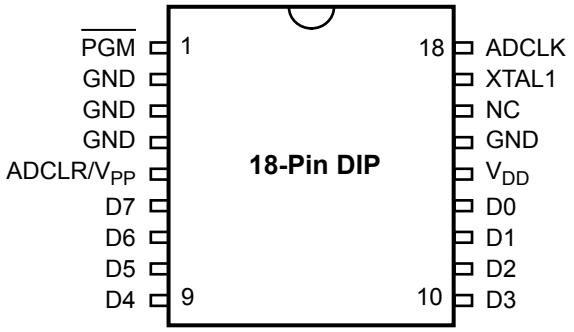


Figure 3. 18-Pin DIP/SOIC Pin Identification/EPROM Programming Mode

EPROM Programming Mode

Pin #	Symbol	Function	Direction
1	$\overline{PGM}$	Prog Mode	Input
2–4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clk./Prog Volt.	Input
6-9	D7–D4	Data 7,6,5,4	Input/Output
10–13	D3–D0	Data 3,2,1,0	Input/Output
14	V_{DD}	Power Supply	
15	GND	Ground	
16	NC	No Connection	
17	XTAL1	1MHz Clock	Input
18	ADCLK	Address Clock	Input

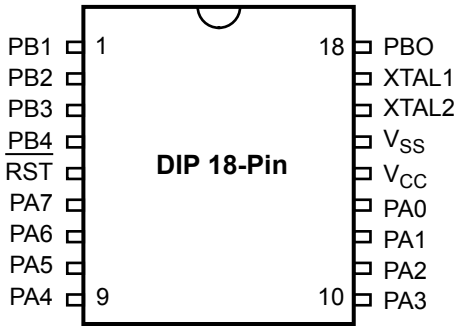


Figure 4. 18-Pin DIP/SOIC Pin Identification

Standard Mode

Pin #	Symbol	Function	Direction
1–4	PB1–PB4	Port B, Pins 1,2,3,4	Input/Output
5	RESET	Reset	Input
6-9	PA7–PA4	Port A, Pins 7,6,5,4	Input/Output
10–13	PA3–PA0	Port A, Pins 3,2,1,0	Input/Output
14	V_{CC}	Power Supply	
15	V_{SS}	Ground	
16	XTAL2	Crystal Osc. Clock	Output
17	XTAL1	Crystal Osc. Clock	Input
18	PB0	Port B, Pin 0	Input/Output

PIN DESCRIPTION (Continued)

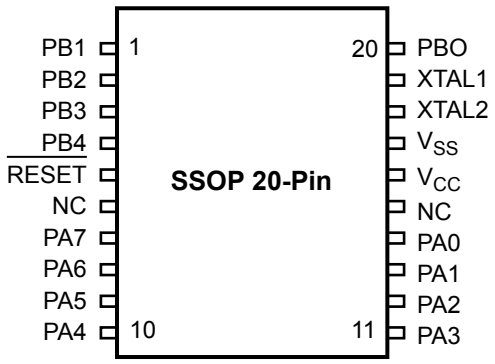


Figure 5. 20-Pin SSOP Pin Identification

Standard Mode

Pin #	Symbol	Function	Direction
1–4	PB1–PB4	Port B, Pins 1,2,3,4	Input/Output
5	RESET	Reset	Input
6	NC	No Connection	
7–10	PA7–PA4	Port A, Pins 7,6,5,4	Input/Output
11–14	PA3–PA0	Port A, Pins 3,2,1,0	Input/Output
15	NC	No Connection	
16	V_{CC}	Power Supply	
17	V_{SS}	Ground	
18	XTAL2	Crystal Osc. Clock	Output
19	XTAL1	Crystal Osc. Clock	Input
20	PB0	Port B, Pin 0	Input/Output

Table 1. DC Electrical Characteristics (Continued)

			pF T_A = 0°C to +70°C Standard Temperatures					
Sym	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Typical[2] @ 25°C**	**Units**	**Conditions**	**Notes**
I_{CC}	Supply Current	3.5V		2.5	2.0	mA	@ 10 MHz	4,5
		5.5V		6.0	3.5	mA	@ 10 MHz	4,5
I_{CC1}	Standby Current	3.5V		2.0	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 10 MHz	4,5
		5.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 10 MHz	4,5
I_{CC2}	Standby Current	3.5V		500	150	nA	STOP Mode V_{IN} = 0V, V_{CC}	6

Notes:
1. The V_{CC} voltage specification of 3.5V guarantees 3.5V and the V_{CC} voltage specification of 5.5 V guarantees 5.0 V ±0.5 V.
2. Typical values are measured at V_{CC} = 3.3V and V_{CC} = 5.0V; V_{SS} = 0V = GND.
3. For analog comparator input when analog comparator is enabled.
4. All outputs unloaded and all inputs are at V_{CC} or V_{SS} level.
5. CL1 = CL2 = 22 pF.
6. Same as note 4 except inputs at V_{CC}.

AC ELECTRICAL CHARACTERISTICS

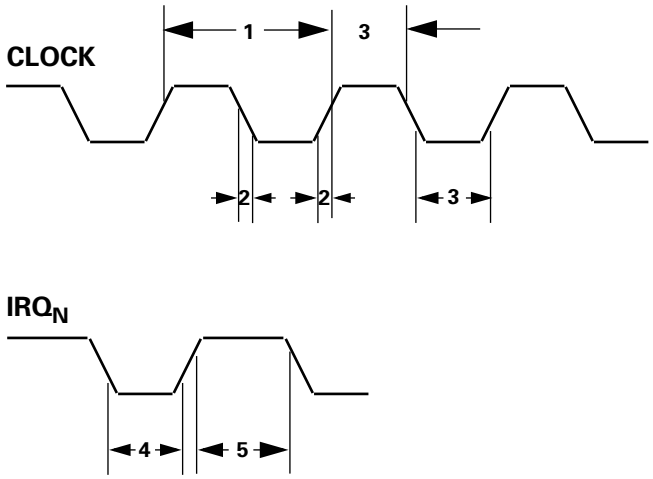


Figure 8. AC Electrical Timing Diagram

Table 3. Additional Timing

				T_A = 0°C to +70°C T_A = –40°C to +105°C @ 10 MHz			
No	**Symbol**	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	3.5V	100	DC	ns	2
			5.5V	100	DC	ns	2
2	TrC,TfC	Clock Input Rise and Fall Times	3.5V		15	ns	2
			5.5V		15	ns	2
3	TwC	Input Clock Width	3.5V	50		ns	2
			5.5V	50		ns	2
4	TwIL	Int. Request Input Low Time	3.5V	70		ns	2
			5.5V	70		ns	2
5	TwIH	Int. Request Input High Time	3.5V	5TpC			2
			5.5V	5TpC			2
6	Twsm	STOP Mode Recovery Width Spec.	3.5V	12		ns	
			5.5V	12		ns	
7	Tost	Oscillator Start-Up Time	3.5V		5TpC		
			5.5V		5TpC		

Notes:
1. The V_{DD} voltage specification of 3.5V guarantees 3.5V. The V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

Z8PLUS CORE

The Z8E001 is based on the ZiLOG Z8Plus Core Architecture. This core is capable of addressing up to 64KBytes of program memory and 4KBytes of RAM. Register RAM is accessed as either 8 or 16 bit registers using a combination of 4, 8, and 12 bit addressing modes. The architecture supports up to 15 vectored interrupts from external and internal sources. The processor decodes 44 CISC instructions using six addressing modes. See the Z8Plus User's Manual for more information.

RESET

This section describes the Z8E001 reset conditions, reset timing, and register initialization procedures. Reset is generated by the Reset Pin, Watch-Dog Timer (WDT), and Stop-Mode Recovery (SMR).

A system reset overrides all other operating conditions and puts the Z8E001 into a known state. To initialize the chip's internal logic, the RESET input must be held Low for at least 30 XTAL clock cycles. The control registers and ports are reset to their default conditions after a reset from the RESET pin. The control registers and ports are not reset to their default conditions after wakeup from Stop Mode or WDT timeout.

During $\overline{\text{RESET}}$, the program counter is loaded with 0020H. I/O ports and control registers are configured to their default reset state. Resetting the Z8E001 does not affect the contents of the general-purpose registers.

RESET PIN OPERATION

The Z8E001 hardware $\overline{\text{RESET}}$ pin initializes the control and peripheral registers, as shown in Table 4. Specific reset values are shown by 1 or 0, while bits whose states are unchanged or unknown from Power-Up are indicated by the letter U.

$\overline{\text{RESET}}$ must be held Low until the oscillator stabilizes, for an additional 30 XTAL clock cycles, in order to be sure that the internal reset is complete. The RESET pin has a Schmitt-Trigger input with a trip point. There is no High side protection diode. The user should place an external diode from $\overline{\text{RESET}}$ to V_{CC}. A pull-up resistor on the $\overline{\text{RESET}}$ pin is approximately 500 KΩ, typical.

Program execution starts 10 XTAL clock cycles after $\overline{\text{RESET}}$ has returned High. The initial instruction fetch is from location 0020H. Figure 9 indicates reset timing.

After a reset, the first routine executed must be one that initializes the TCTLHI control register to the required system configuration, followed by initialization of the remaining control registers.

Table 4. Control and Peripheral Registers

		Bits								
Register (HEX)	**Register Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**
FF	Stack Pointer	0	0	U	U	U	U	U	U	Stack pointer is not affected by RESET
FE	Reserved									
FD	Register Pointer	U	U	U	U	0	0	0	0	Register pointer is not affected by RESET
FC	Flags	U	U	U	U	U	U	*	*	Only WDT & SMR flags are affected by RESET
FB	Interrupt Mask	0	0	0	0	0	0	0	0	All interrupts masked by $\overline{\text{RESET}}$
FA	Interrupt Request	0	0	0	0	0	0	0	0	All interrupt requests cleared by RESET
F9–F0	Reserved									
EF–E0	Virtual Copy									Virtual Copy of the Current Working Register Set
DF–D8	Reserved									

Z8E001 WATCH-DOG TIMER (WDT)

The WDT is a retriggerable one-shot 16-bit timer that resets the Z8E001 if it reaches its terminal count. The WDT is driven by the XTAL2 clock pin. To provide the longer timeout periods required in applications, the watchdog timer is only updated every 64th clock cycle. When operating in the RUN or HALT Modes, a WDT timeout reset is functionally equivalent to an interrupt vectoring the PC to 0020H and setting the WDT flag to a one state. Coming out of RESET, the WDT is fully enabled with its timeout value set at the maximum value, unless otherwise programmed during the first instruction. Subsequent executions of the WDT instruction, reinitialize the watchdog timer registers (C2H and C3H), to their initial values as defined by bits D6, D5, and D4 of the TCTLHI register. The WDT cannot be disabled except on the first cycle after RESET, and if the device enters Stop mode.

The WDT instruction should be executed often enough to provide some margin before allowing the WDT registers to get near 0. Because the WDT timeout periods are relatively long, a WDT reset will occur in the unlikely event that the WDT times out on exactly the same cycle that the WDT instruction is executed.

The WDT and SMR flags are the only flags that are affected by the external RESET pin. RESET clears both the WDT and SMR flags. A WDT timeout sets the WDT flag. The STOP instruction sets the SMR flag. This behavior enables software to determine whether a pin RESET occurred, or whether a WDT timeout occurred, or whether a return from STOP Mode occurred. Reading the WDT and SMR flags does not reset it to zero, the user must clear it via software.

Note: Failure to clear the SMR flag can result in undefined behavior.

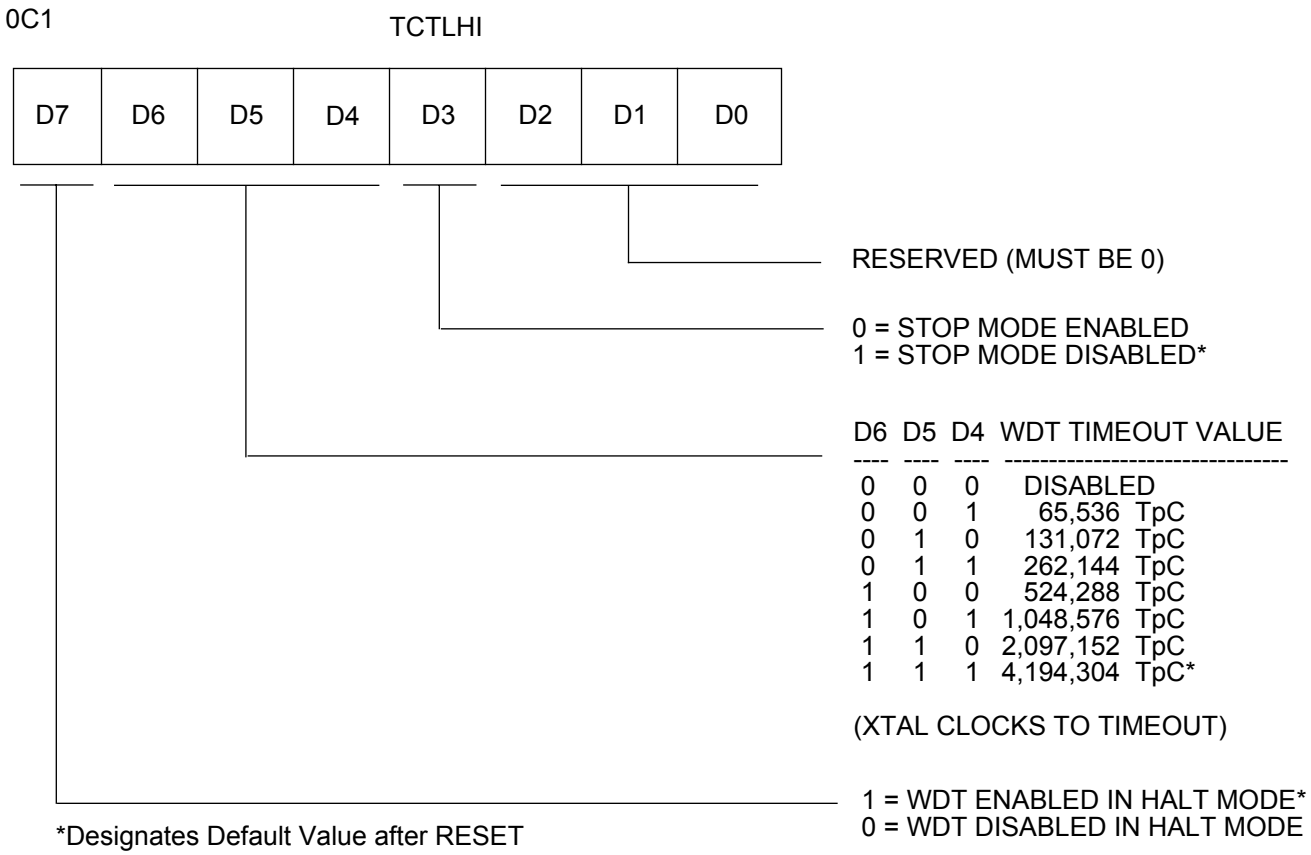


Figure 12. Z8E001 TCTLHI Register for Control of WDT

Note: The WDT can only be disabled via software if the first instruction out of RESET performs this function. Logic within the Z8E001 detects that it is in the process of executing the first instruction after the part leaves RESET. During the execution of this instruction, the upper five bits of the TCTLHI register can be written. After this first instruction, hardware does not allow the upper five bits of this register to be written.

The TCTLHI bits for control of the WDT are described below:

WDT Time Select (D6, D5, D4). Bits 6, 5, and 4 determine the time-out period. Table 6 indicates the range of timeout values that can be obtained. The default values of D6, D5, and D4 are all 1, thus setting the WDT to its maximum timeout period when coming out of RESET.

WDT During HALT (D7). This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. A 0 prevents the WDT from resetting the part while halted.Coming out of reset, the WDT is enabled during HALT Mode.

STOP MODE (D3). Coming out of RESET, the Z8E001 STOP Mode is disabled. If an application requires use of STOP Mode, bit D3 must be cleared immediately upon leaving RESET. If bit D3 is set, the STOP instruction executes as a NOP. If bit D3 is cleared, the STOP instruction enters Stop Mode. Whenever the Z8E001 wakes up after having been in STOP Mode, the STOP Mode is again disabled.

Bits 2, 1 and 0. These bits are reserved and must be 0.

Table 6. WDT Time-Out

D6	D5	D4	Crystal Clocks* to Timeout	Time-Out Using a 10 MHZ Crystal
0	0	0	Disabled	Disabled
0	0	1	65,536 TpC	6.55 ms
0	1	0	131,072 TpC	13.11 ms
0	1	1	262,144 TpC	26.21 ms
1	0	0	524,288 TpC	52.43 ms
1	0	1	1,048,576 TpC	104.86 ms
1	1	0	2,097,152 TpC	209.72 ms
1	1	1	4,194,304 TpC	419.43 ms

Note:
*TpC=XTAL clock cycle. The default on reset is D6=D5=D4=1.

POWER-DOWN MODES

In addition to the standard RUN mode, the Z8E001 MCU supports two Power-Down modes to minimize device current consumption. The two modes supported are HALT and STOP.

HALT MODE OPERATION

The HALT Mode suspends instruction execution and turns off the internal CPU clock. The on-chip oscillator circuit remains active so the internal clock continues to run and is applied to the timers and interrupt logic.

To enter the HALT Mode, the Z8E001 only requires a HALT instruction. It is NOT necessary to execute a NOP instruction immediately before the HALT instruction.

```
7F      HALT            ; enter HALT Mode
```

The HALT Mode can be exited by servicing an interrupt (either externally or internally) generated. Upon completion of the interrupt service routine, the user program continues from the instruction after the HALT instruction.

The HALT Mode can also be exited via a RESET activation or a Watch-Dog Timer (WDT) timeout. In these cases, program execution restarts at the reset restart address 0020H.

OSCILLATOR OPERATION

The Z8E001 MCU uses a Pierce oscillator with an internal feedback resistor (Figure 14). The advantages of this circuit are low-cost, large output signal, low-power level in the crystal, stability with respect to V_{CC} and temperature, and low impedances (not disturbed by stray effects).

One draw back is the requirement for high gain in the amplifier to compensate for feedback path losses. The oscillator amplifies its own noise at start-up until it settles at the frequency that satisfies the gain/phase requirements (A x B = 1; where $A = V_o/V_i$ is the gain of the amplifier and $B = V_i/V_o$ is the gain of the feedback element). The total phase shift around the loop is forced to zero (360 degrees). V_{IN} must be in phase with itself; therefore, the amplifier/inverter provides a 180-degree phase shift, and the feedback element is forced to provide the other 180-degree phase shift.

R1 is a resistive component placed from output to input of the amplifier. The purpose of this feedback is to bias the amplifier in its linear region and provide the start-up transition.

Capacitor C_2, combined with the amplifier output resistance, provides a small phase shift. It also provides some attenuation of overtones.

Capacitor C_1, combined with the crystal resistance, provides an additional phase shift.

C_1 and C_2 can affect the start-up time if they increase dramatically in size. As C_1 and C_2 increase, the start-up time increases until the oscillator reaches a point where it does not start up any more.

It is recommended for fast and reliable oscillator start-up (over the manufacturing process range) that the load capacitors be sized as low as possible without resulting in overtone operation.

Layout

Traces connecting crystal, caps, and the Z8E001 oscillator pins should be as short and wide as possible, to reduce parasitic inductance and resistance. The components (caps, crystal, resistors) should be placed as close as possible to the oscillator pins of the Z8E001.

The traces from the oscillator pins of the IC and the ground side of the lead caps should be guarded from all other traces (clock, V_{CC}, address/data lines, system ground) to reduce cross talk and noise injection. Guarding is usually accomplished by keeping other traces and system ground trace planes away from the oscillator circuit, and by placing a Z8E001 device V_{SS} ground ring around the traces/components. The ground side of the oscillator lead caps should be connected to a single trace to the Z8E001 V_{SS} (GND) pin. It should not be shared with any other system ground trace or components except at the Z8E001 device V_{SS} pin. The objective is to prevent differential system ground noise injection into the oscillator (Figure 15).

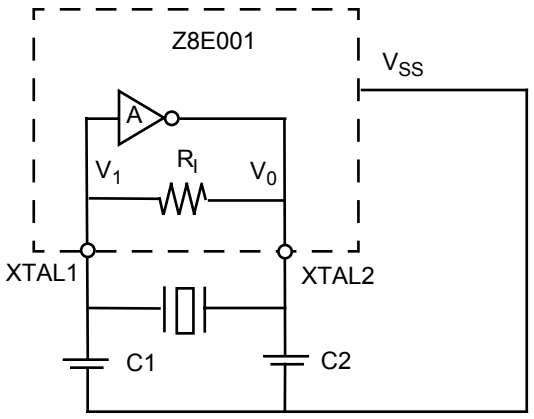


Figure 14. Pierce Oscillator with Internal Feedback Circuit

Indications of an Unreliable Design

There are two major indicators that are used in working designs to determine their reliability over full lot and temperature variations. They are:

Start-up Time. If start-up time is excessive, or varies widely from unit to unit, there is probably a gain problem. To fix the problem, the capacitors C1/C2 require reduction. The amplifier gain is either not adequate at frequency, or the crystal Rs are too large.

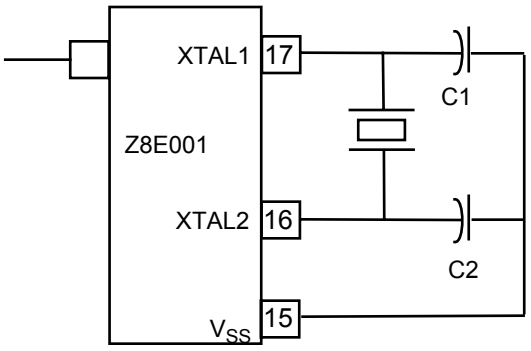
Output Level. The signal at the amplifier output should swing from ground to V_{CC} to indicate adequate gain in the amplifier. As the oscillator starts up, the signal amplitude grows until clipping occurs. At that point, the loop gain is effectively reduced to unity, and constant oscillation is achieved. A signal of less than 2.5 volts peak-to-peak is an indication that low gain can be a problem. Either C_1 or C_2 should be made smaller, or a low-resistance crystal should be used.

Circuit Board Design Rules

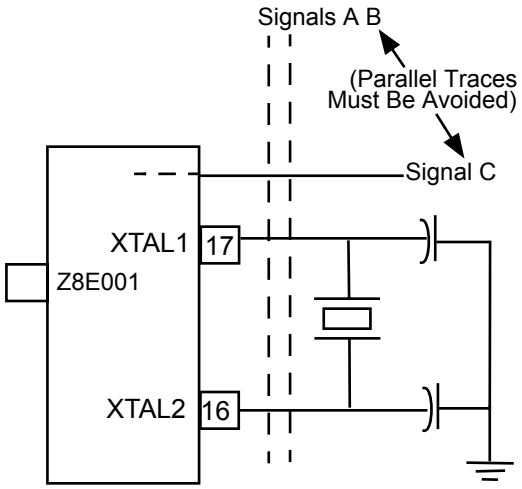
The following circuit board design rules are suggested:

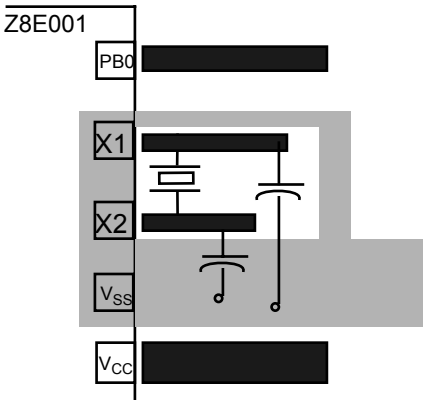
- To prevent induced noise, the crystal and load capacitors should be physically located as close to the Z8E001 as possible.
- Signal lines should not run parallel to the clock oscillator inputs. In particular, the crystal input circuitry and the internal system clock output should be separated as much as possible.

- V_{CC} power lines should be separated from the clock oscillator input circuitry.
- Resistivity between XTAL1 or XTAL2 (and the other pins) should be greater than 10 MΩ.



Clock Generator Circuit





Board Design Example

(Top View)

Figure 15. Circuit Board Design Rules

Crystals and Resonators

Crystals and ceramic resonators (Figure 16) should have the following characteristics to ensure proper oscillation:

Crystal Cut	AT (crystal only)
Mode	Parallel, Fundamental Mode
Crystal Capacitance	<7pF
Load Capacitance	10pF < CL < 220 pF,
	15 typical
Resistance	100 ohms max

Depending on the operation frequency, the oscillator can require additional capacitors, C1 and C2, as shown in Figure 16 and Figure 17. The capacitance values are dependent on the manufacturer's crystal specifications.

OSCILLATOR OPERATION (Continued)

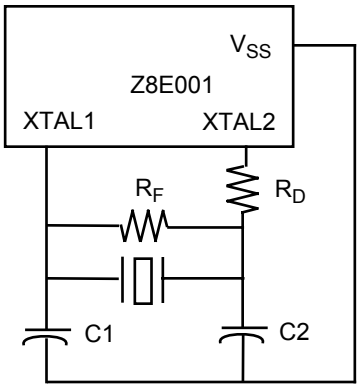


Figure 16. Crystal/Ceramic Resonator Oscillator

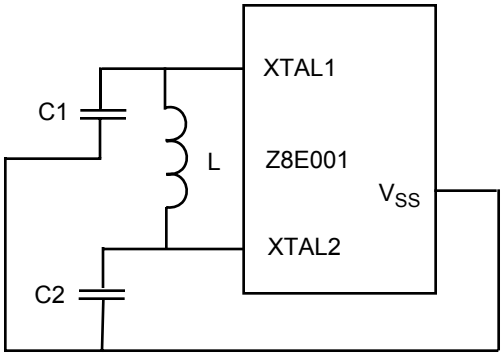


Figure 17. LC Clock

In most cases, the R_D is 0 Ohms and R_F is infinite. These specifications are determined and specified by the crystal/ceramic resonator manufacturer. The R_D can be increased to decrease the amount of drive from the oscillator output to the crystal. It can also be used as an adjustment to avoid clipping of the oscillator signal to reduce noise. The R_F can be used to improve the start-up of the crystal/ceramic resonator. The Z8E001 oscillator already has an internal shunt resistor in parallel to the crystal/ceramic resonator.

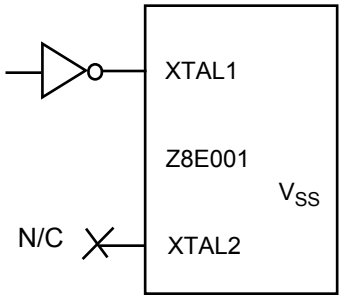


Figure 18. External Clock

Figure 16, Figure 17, and Figure 18 recommend that the load capacitor ground trace connect directly to the V_{SS} (GND) pin of the Z8E001. This requirement assures that no system noise is injected into the Z8E001 clock. This trace should not be shared with any other components except at the V_{SS} pin of the Z8E001.

Note: A parallel resonant crystal or resonator data sheet specifies a load capacitor value that is a series combination of C_1 and C_2, including all parasitics (PCB and holder).

LC OSCILLATOR

The Z8E001 oscillator can use a LC network to generate a XTAL clock (Figure 17).

The frequency stays stable over V_{CC} and temperature. The oscillation frequency is determined by the equation:

$$\text{Frequency} = \frac{1}{2\pi (LC_T)^{1/2}}$$

where L is the total inductance including parasitics, and C_T is the total series capacitance including parasitics.

Simple series capacitance is calculated using the equation at the top of the next column.

$$1/C_T = 1/C_1 + 1/C_2$$

$$\text{If } C_1 = C_2$$

$$1/C_T = 2\,C_1$$

$$C_1 = 2C_T$$

A sample calculation of capacitance C_1 and C_2 for 5.83 MHz frequency and inductance value of 27 µH is displayed as follows:

$$5.83\ (10\text{^}6) = \frac{1}{2\pi\,[2.7\ (10^{-6})\ C_T]\int}$$

$$C_T = 27.6\ \text{pF}$$

Thus C_1 = 55.2 pF and C_2 = 55.2 pF.

TIMERS

For the Z8E001, 8-bit timers (T0 and T1) are available to function as a pair of independent 8-bit standard timers, or they can be cascaded to function as a 16-bit PWM timer.

In addition to T0 and T1, extra 8-bit timers (T2 and T3) are provided, but they can only operate in cascade to function as a 16-bit standard timer.

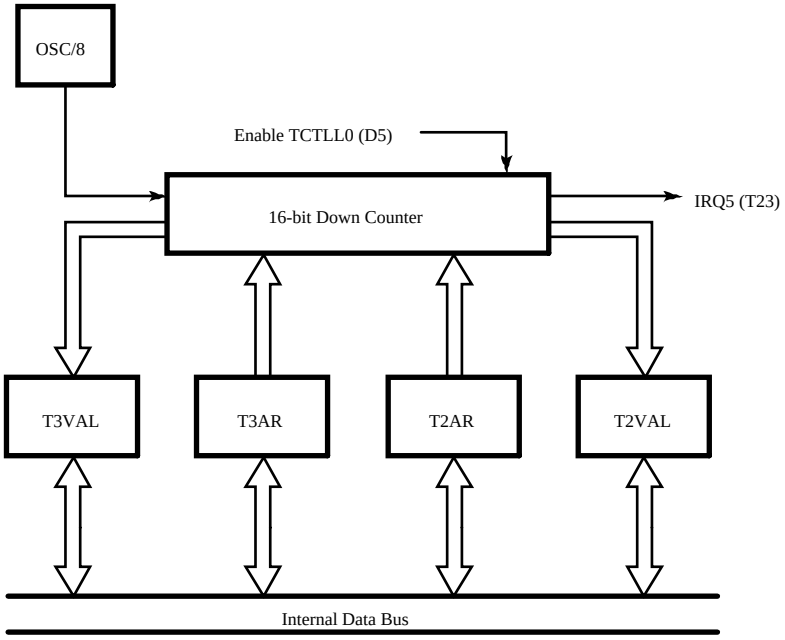


Figure 19. Z8E001 16-Bit Standard Timer

RESET CONDITIONS

After a hardware $\overline{\text{RESET}}$, the timers are disabled. See Table 4 for timer control, value, and auto-initialization register status after RESET.

I/O PORTS

The Z8E001 has 13 lines dedicated to input and output. These lines are grouped into two ports known as Port A and Port B. Port A is an 8-bit port, bit programmable as either inputs or outputs. Port B can be programmed to provide standard input/output or the following special functions: timer0 output, comparator input, SMR input, and external interrupt inputs.

All ports have push-pull CMOS outputs. In addition, the outputs of Port A on a bit-wise basis can be configured for open-drain operation.The ports operate on a bit-wise basis. As such, the register values for/at a given bit position only affect the bit in question.

Each port is defined by a set of four control registers. See Figure 27.

Directional Control and Special Function Registers

Each port on the Z8E001 has a dedicated Directional Control Register that determines (on a bit-wise basis) whether a given port bit operates as either an input or an output.

Each port on the Z8E001 has a Special Function Register that, in conjunction with the Directional Control Register, implements (on a bit-wise basis), any special functionality that can be defined for each particular port bit.

Table 7. Z8E001 I/O Ports Registers

Register	Address	Identifier
Port B Special Function	OD7H	PTBSFR
Port B Directional Control	0D6H	PTBDIR
Port B Output Value	0D5H	PTBOUT
Port B Input Value	0D4H	PTBIN
Port A Special Function	0D3H	PTASFR
Port A Directional Control	0D2H	PTADIR
Port A Output Value	0D1H	PTAOUT
Port A Input Value	0D0H	PTAIN

Input and Output Value Registers

Each port has an Output Value Register and a pF Input Value Register. For port bits configured as an input by means of the Directional Control Register, the Input Value Register for that bit position contains the current synchronized input value.

For port bits configured as an output by means of the Directional Control Register, the value held in the corresponding bit of the Output Value Register is driven directly onto the output pin. The opposite register bit for a given pin (the output register bit for an input pin and the input register bit for an output pin) holds their previous value. These bits are not changed and don't have any effect on the hardware.

READ/WRITE OPERATIONS

The control for each port is done on a bit-wise basis. All bits are capable of operating as inputs or outputs, depending upon the setting of the port's Directional Control Register. If configured as an input, each bit is provided a Schmitt-trigger. The output of the Schmitt-trigger is latched twice to perform a synchronization function, and the output of the synchronizer is fed to the port input register, which can be read by software.

A write to a port input register has the effect of updating the contents of the input register, but subsequent reads do not necessarily return the same value that was written. If the bit in question is defined as an input, the input register for that bit position contains the current synchronized input value. Thus, writes to that bit position is overwritten on the next clock cycle with the newly sampled input data. However, if the particular port bit is programmed as an output, the input register for that bit retains the software-updated value. The port bits that are programmed as outputs do not sample the value being driven out.

Any bit in either port can be defined as an output by setting the appropriate bit in the directional control register. If such is the case, the value held in the appropriate bit of the port output register is driven directly onto the output pin.

Note: The preceding result does not necessarily reflect the actual output value. If an external error is holding an output pin either High or Low against the output driver, the software read returns the *required* value, not the actual state caused by the contention. When a bit is defined as an output, the Schmitt-trigger on the input is disabled to save power.

Updates to the output register takes effect based upon the timing of the internal instruction pipeline, but is referenced to the rising edge of the clock. The output register can be read at any time, and returns the current output value that is held. No restrictions are placed on the timing of reads and/or writes to any of the port registers with respect to the others; however, care should be taken when updating the directional control and special function registers.

When updating a Directional Control Register, the Special Function Register should first be disabled. If this precaution is not taken, spurious events could take place as a result of the change in port I/O status. This precaution is especially important when defining changes in Port B, as the spurious event referred to above could be one or more interrupts. Clearing of the SFR register should be the first step in configuring the port, while setting the SFR register should be the final step in the port configuration process. To ensure deterministic behavior, the SFR register should not be written until the pins are being driven appropriately, and all initialization has been completed.

PORT A

Port A is a general-purpose port. Figure 26 features a block diagram of Port A. Each of its lines can be independently programmed as input or output via the Port A Directional Control Register (PTADIR at 0D2H) as seen in Figure 27. A bit set to a 1 in PTADIR configures the corresponding bit in Port A as an output, while a bit cleared to 0 configures the corresponding bit in Port A as an input.

The input buffers are Schmitt-triggered. Bits programmed as outputs can be individually programmed as either push-pull or open drain by setting the corresponding bit in the Special Function Register (PTASFR, Figure 27).

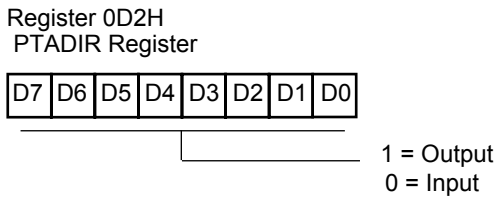


Figure 26. Port A Directional Control Register

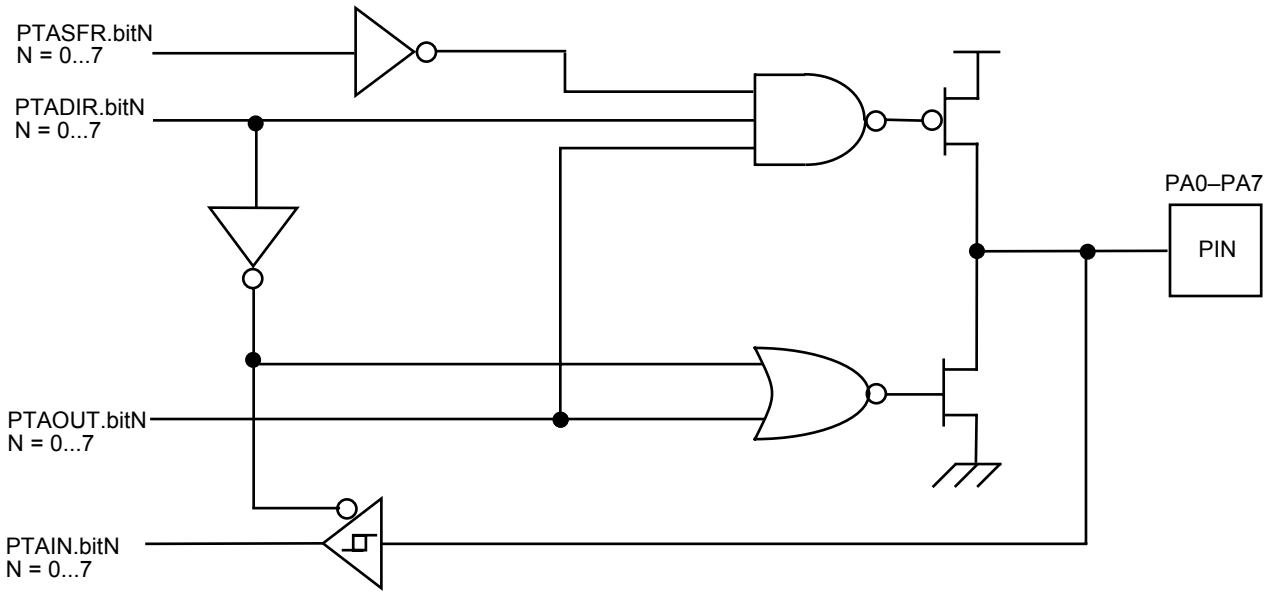


Figure 27. Port A Configuration with Open-Drain Capability and Schmitt-Trigger

PORT A REGISTER DIAGRAMS

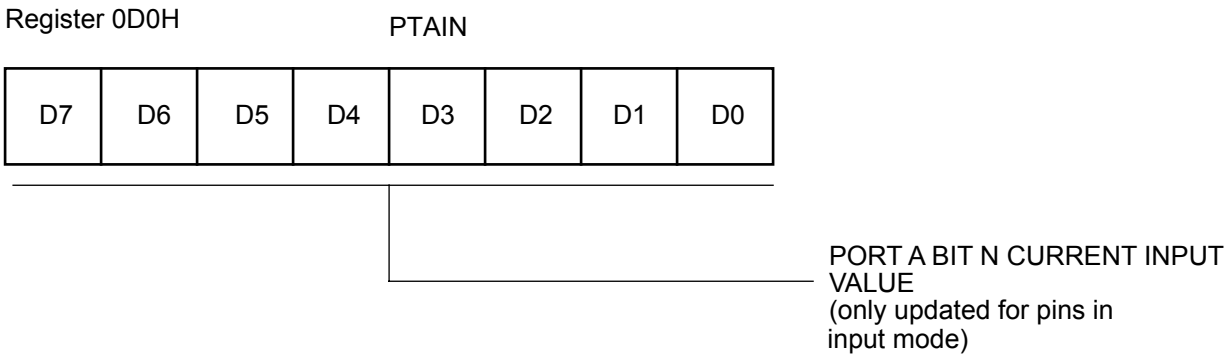


Figure 28. Port A Input Value Register

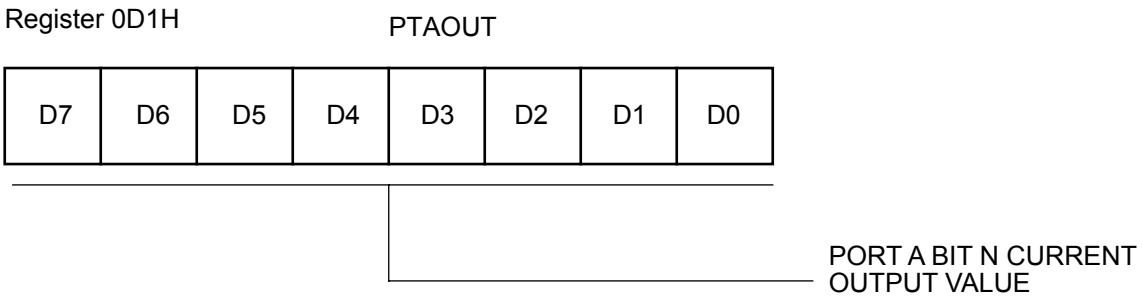


Figure 29. Port A Output Value Register

PORT B—PIN 0 CONFIGURATION

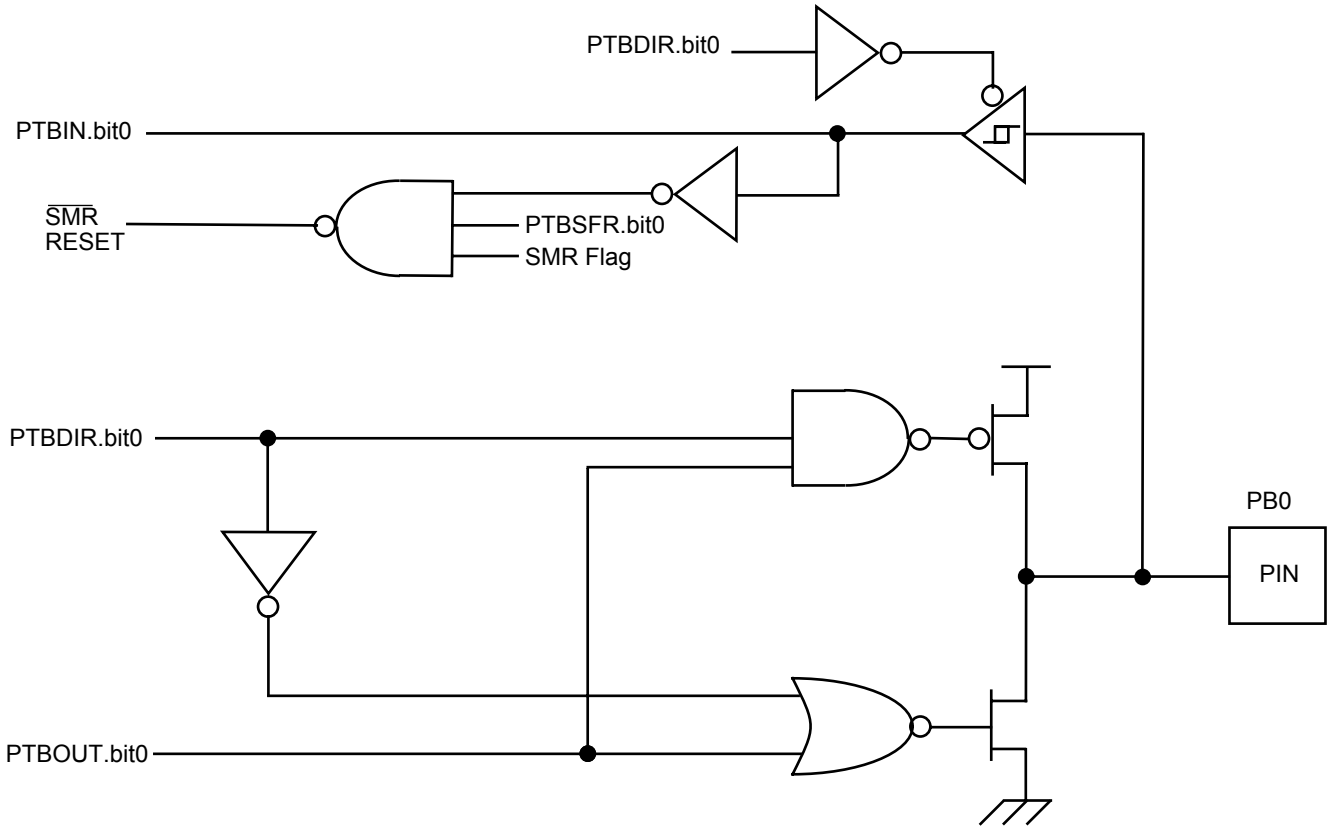


Figure 33. Port B Pin 0 Diagram

PORT B—PINS 3 AND 4 CONFIGURATION

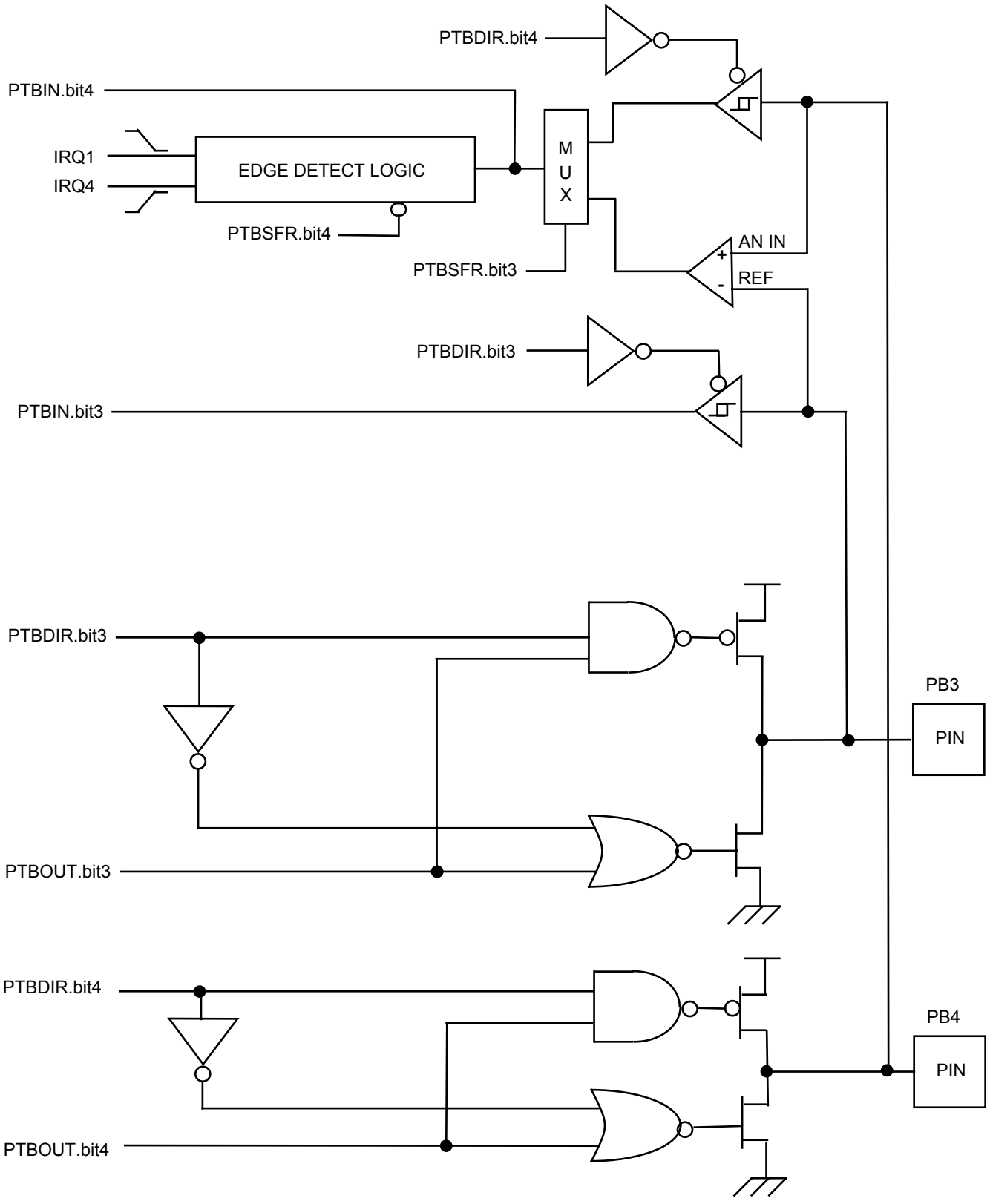


Figure 36. Port B Pins 3 and 4 Diagram

INPUT PROTECTION

All I/O pins on the Z8E001 have diode input protection. There is a diode from the I/O pad to V_{CC} and V_{SS} (Figure 41).

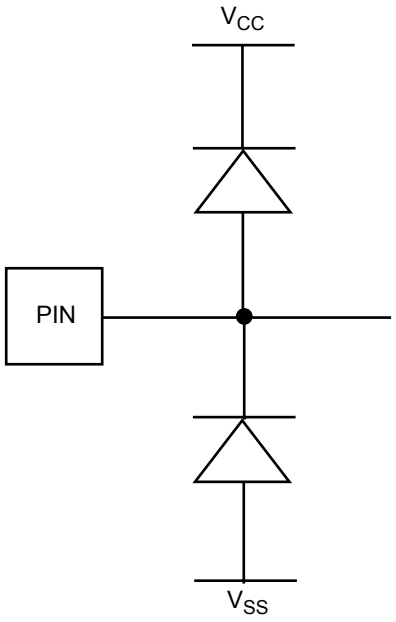


Figure 41. I/O Pin Diode Input Protection

However, on the Z8E001, the $\overline{\text{RESET}}$ pin has only the input protection diode from pad to V_{SS} (Figure 42).

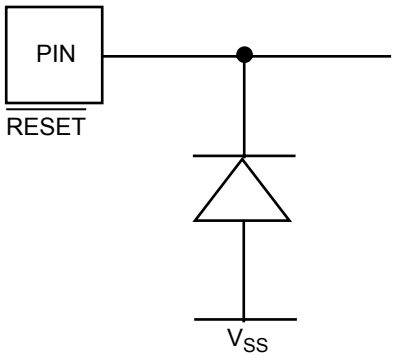


Figure 42. $\overline{\text{RESET}}$ Pin Input Protection

The high-side input protection diode was removed on this pin to allow the application of high voltage during the OTP programming mode.

For better noise immunity in applications that are exposed to system EMI, a clamping diode to V_{CC} from this pin can be required to prevent entering the OTP programming mode or to prevent high voltage from damaging this pin.

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