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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	PWM, WDT
Number of I/O	13
Program Memory Size	1KB (1K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8e00110hsc

PIN DESCRIPTION (Continued)

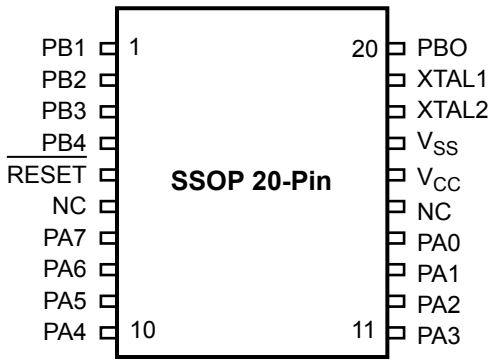


Figure 5. 20-Pin SSOP Pin Identification

Standard Mode

Pin #	Symbol	Function	Direction
1–4	PB1–PB4	Port B, Pins 1,2,3,4	Input/Output
5	RESET	Reset	Input
6	NC	No Connection	
7–10	PA7–PA4	Port A, Pins 7,6,5,4	Input/Output
11–14	PA3–PA0	Port A, Pins 3,2,1,0	Input/Output
15	NC	No Connection	
16	V_{CC}	Power Supply	
17	V_{SS}	Ground	
18	XTAL2	Crystal Osc. Clock	Output
19	XTAL1	Crystal Osc. Clock	Input
20	PB0	Port B, Pin 0	Input/Output

DC ELECTRICAL CHARACTERISTICS

Table 1. DC Electrical Characteristics

			pF T_A = 0°C to +70°C Standard Temperatures					
Sym	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Typical[2] @ 25°C**	**Units**	**Conditions**	**Notes**
V_{CH}	Clock Input High Voltage	3.5V	$0.7V_{CC}$	V_{CC}+0.3	1.3	V	Driven by External Clock Generator	
		5.5V	$0.7V_{CC}$	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.5V	V_{SS}–0.3	$0.2V_{CC}$	0.7	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	$0.2V_{CC}$	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.5V	$0.7V_{CC}$	V_{CC}+0.3	1.3	V		
		5.5V	$0.7V_{CC}$	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	3.5V	V_{SS}–0.3	$0.2V_{CC}$	0.7	V		
		5.5V	V_{SS}–0.3	$0.2V_{CC}$	1.5	V		
V_{OH}	Output High Voltage	3.5V	V_{CC}–0.4		3.1	V	I_{OH} = –2.0 mA	
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	
V_{OL1}	Output Low Voltage	3.5V		0.6	0.2	V	I_{OL} = +4.0 mA	
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	
V_{OL2}	Output Low Voltage	3.5V		1.2	0.5	V	I_{OL} = +6 mA	
		5.5V		1.2	0.5	V	I_{OL} = +12 mA	
V_{RH}	Reset Input High Voltage	3.5V	$0.5V_{CC}$	V_{CC}	1.1	V		
		5.5V	$0.5V_{CC}$	V_{CC}	2.2	V		
V_{RL}	Reset Input Low Voltage	3.5V	V_{SS}–0.3	$0.2V_{CC}$	0.9	V		
		5.5V	V_{SS}–0.3	$0.2V_{CC}$	1.4	V		
V_{OFFSET}	Comparator Input Offset Voltage	3.5V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
I_{IL}	Input Leakage	3.5V	–1.0	2.0	0.064	mA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	0.064	mA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.5V	–1.0	2.0	0.114	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	0.114	µA	V_{IN} = 0V, V_{CC}	
V_{ICR}	Comparator Input Common Mode Voltage Range	3.5V	V_{SS}–0.3	V_{CC}–1.0		V		3
		5.5V	V_{SS}–0.3	V_{CC}–1.0		V		3
I_{IR}	Reset Input Current	3.5V	–10	–60	–30	µA		
		5.5V	–20	–180	–100	µA		

Table 1. DC Electrical Characteristics (Continued)

			pF T_A = 0°C to +70°C Standard Temperatures					
Sym	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Typical[2] @ 25°C**	**Units**	**Conditions**	**Notes**
I_{CC}	Supply Current	3.5V		2.5	2.0	mA	@ 10 MHz	4,5
		5.5V		6.0	3.5	mA	@ 10 MHz	4,5
I_{CC1}	Standby Current	3.5V		2.0	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 10 MHz	4,5
		5.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 10 MHz	4,5
I_{CC2}	Standby Current	3.5V		500	150	nA	STOP Mode V_{IN} = 0V, V_{CC}	6

Notes:
1. The V_{CC} voltage specification of 3.5V guarantees 3.5V and the V_{CC} voltage specification of 5.5 V guarantees 5.0 V ±0.5 V.
2. Typical values are measured at V_{CC} = 3.3V and V_{CC} = 5.0V; V_{SS} = 0V = GND.
3. For analog comparator input when analog comparator is enabled.
4. All outputs unloaded and all inputs are at V_{CC} or V_{SS} level.
5. CL1 = CL2 = 22 pF.
6. Same as note 4 except inputs at V_{CC}.

Z8PLUS CORE

The Z8E001 is based on the ZiLOG Z8Plus Core Architecture. This core is capable of addressing up to 64KBytes of program memory and 4KBytes of RAM. Register RAM is accessed as either 8 or 16 bit registers using a combination of 4, 8, and 12 bit addressing modes. The architecture supports up to 15 vectored interrupts from external and internal sources. The processor decodes 44 CISC instructions using six addressing modes. See the Z8Plus User's Manual for more information.

RESET

This section describes the Z8E001 reset conditions, reset timing, and register initialization procedures. Reset is generated by the Reset Pin, Watch-Dog Timer (WDT), and Stop-Mode Recovery (SMR).

A system reset overrides all other operating conditions and puts the Z8E001 into a known state. To initialize the chip's internal logic, the RESET input must be held Low for at least 30 XTAL clock cycles. The control registers and ports are reset to their default conditions after a reset from the RESET pin. The control registers and ports are not reset to their default conditions after wakeup from Stop Mode or WDT timeout.

During $\overline{\text{RESET}}$, the program counter is loaded with 0020H. I/O ports and control registers are configured to their default reset state. Resetting the Z8E001 does not affect the contents of the general-purpose registers.

RESET PIN OPERATION

The Z8E001 hardware $\overline{\text{RESET}}$ pin initializes the control and peripheral registers, as shown in Table 4. Specific reset values are shown by 1 or 0, while bits whose states are unchanged or unknown from Power-Up are indicated by the letter U.

$\overline{\text{RESET}}$ must be held Low until the oscillator stabilizes, for an additional 30 XTAL clock cycles, in order to be sure that the internal reset is complete. The RESET pin has a Schmitt-Trigger input with a trip point. There is no High side protection diode. The user should place an external diode from $\overline{\text{RESET}}$ to V_{CC}. A pull-up resistor on the $\overline{\text{RESET}}$ pin is approximately 500 KΩ, typical.

Program execution starts 10 XTAL clock cycles after $\overline{\text{RESET}}$ has returned High. The initial instruction fetch is from location 0020H. Figure 9 indicates reset timing.

After a reset, the first routine executed must be one that initializes the TCTLHI control register to the required system configuration, followed by initialization of the remaining control registers.

Table 4. Control and Peripheral Registers

		Bits								
Register (HEX)	**Register Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**
FF	Stack Pointer	0	0	U	U	U	U	U	U	Stack pointer is not affected by RESET
FE	Reserved									
FD	Register Pointer	U	U	U	U	0	0	0	0	Register pointer is not affected by RESET
FC	Flags	U	U	U	U	U	U	*	*	Only WDT & SMR flags are affected by RESET
FB	Interrupt Mask	0	0	0	0	0	0	0	0	All interrupts masked by $\overline{\text{RESET}}$
FA	Interrupt Request	0	0	0	0	0	0	0	0	All interrupt requests cleared by RESET
F9–F0	Reserved									
EF–E0	Virtual Copy									Virtual Copy of the Current Working Register Set
DF–D8	Reserved									

RESET PIN OPERATION (Continued)

Table 4. Control and Peripheral Registers (Continued)

		Bits								
Register (HEX)	**Register Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**
D7	Port B Special Function	0	0	0	0	0	0	0	0	Deactivates all port special functions after RESET
D6	Port B Directional Control	0	0	0	0	0	0	0	0	Defines all bits as inputs in PortB after RESET
D5	Port B Output	U	U	U	U	U	U	U	U	Output register not affected by RESET
D4	Port B Input	U	U	U	U	U	U	U	U	Current sample of the input pin following RESET
D3	Port A Special Function	0	0	0	0	0	0	0	0	Deactivates all port special functions after RESET
D2	Port A Directional Control	0	0	0	0	0	0	0	0	Defines all bits as inputs in PortA after RESET
D1	Port A Output	U	U	U	U	U	U	U	U	Output register not affected by RESET
D0	Port A Input	U	U	U	U	U	U	U	U	Current sample of the input pin following RESET
CF	Reserved									
CE	Reserved									
CD	T1VAL	U	U	U	U	U	U	U	U	
CC	T0VAL	U	U	U	U	U	U	U	U	
CB	T3VAL	U	U	U	U	U	U	U	U	
CA	T2VAL	U	U	U	U	U	U	U	U	
C9	T3AR	U	U	U	U	U	U	U	U	
C8	T2AR	U	U	U	U	U	U	U	U	
C7	T1ARHI	U	U	U	U	U	U	U	U	
C6	T0ARHI	U	U	U	U	U	U	U	U	
C5	T1ARLO	U	U	U	U	U	U	U	U	
C4	T0ARLO	U	U	U	U	U	U	U	U	
C3	WDTHI	1	1	1	1	1	1	1	1	
C2	WDTLO	1	1	1	1	1	1	1	1	
C1	TCTLHI	1	1	1	1	1	0	0	0	WDT Enabled in HALT Mode, WDT timeout at maximum value, STOP Mode disabled
C0	TCTLLO	0	0	0	0	0	0	0	0	All standard timers are disabled

Note: *The SMR and WDT flags are set indicating the source of the $\overline{\text{RESET}}$.

Table 5. Flag Register Bit D1, D0

D1	D0	Reset Source
0	0	RESET Pin
0	1	SMR Recovery
1	0	WDT Reset
1	1	Reserved

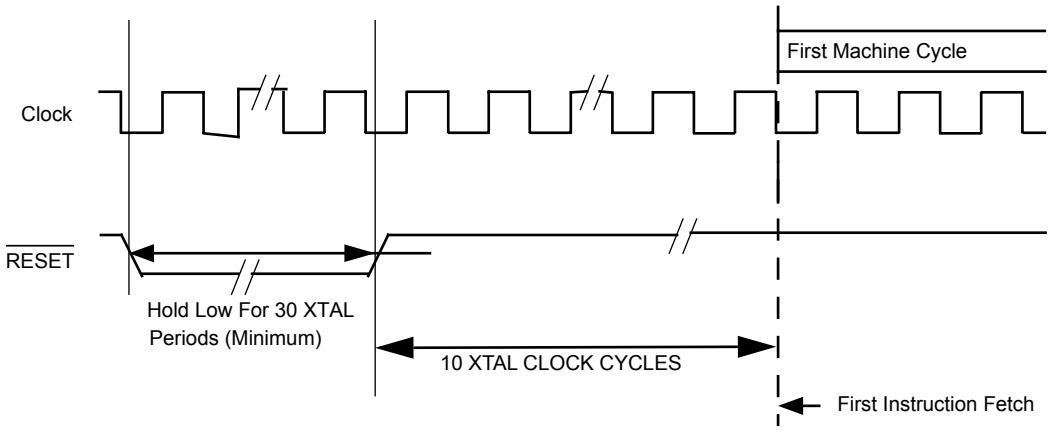


Figure 9. Reset Timing

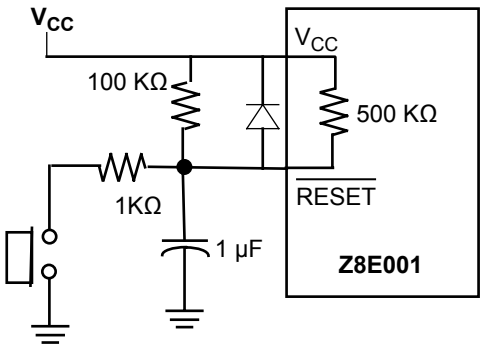


Figure 10. Example of External Power-On Reset (POR) Circuit

Z8E001 WATCH-DOG TIMER (WDT)

The WDT is a retriggerable one-shot 16-bit timer that resets the Z8E001 if it reaches its terminal count. The WDT is driven by the XTAL2 clock pin. To provide the longer timeout periods required in applications, the watchdog timer is only updated every 64th clock cycle. When operating in the RUN or HALT Modes, a WDT timeout reset is functionally equivalent to an interrupt vectoring the PC to 0020H and setting the WDT flag to a one state. Coming out of RESET, the WDT is fully enabled with its timeout value set at the maximum value, unless otherwise programmed during the first instruction. Subsequent executions of the WDT instruction, reinitialize the watchdog timer registers (C2H and C3H), to their initial values as defined by bits D6, D5, and D4 of the TCTLHI register. The WDT cannot be disabled except on the first cycle after RESET, and if the device enters Stop mode.

The WDT instruction should be executed often enough to provide some margin before allowing the WDT registers to get near 0. Because the WDT timeout periods are relatively long, a WDT reset will occur in the unlikely event that the WDT times out on exactly the same cycle that the WDT instruction is executed.

The WDT and SMR flags are the only flags that are affected by the external RESET pin. RESET clears both the WDT and SMR flags. A WDT timeout sets the WDT flag. The STOP instruction sets the SMR flag. This behavior enables software to determine whether a pin RESET occurred, or whether a WDT timeout occurred, or whether a return from STOP Mode occurred. Reading the WDT and SMR flags does not reset it to zero, the user must clear it via software.

Note: Failure to clear the SMR flag can result in undefined behavior.

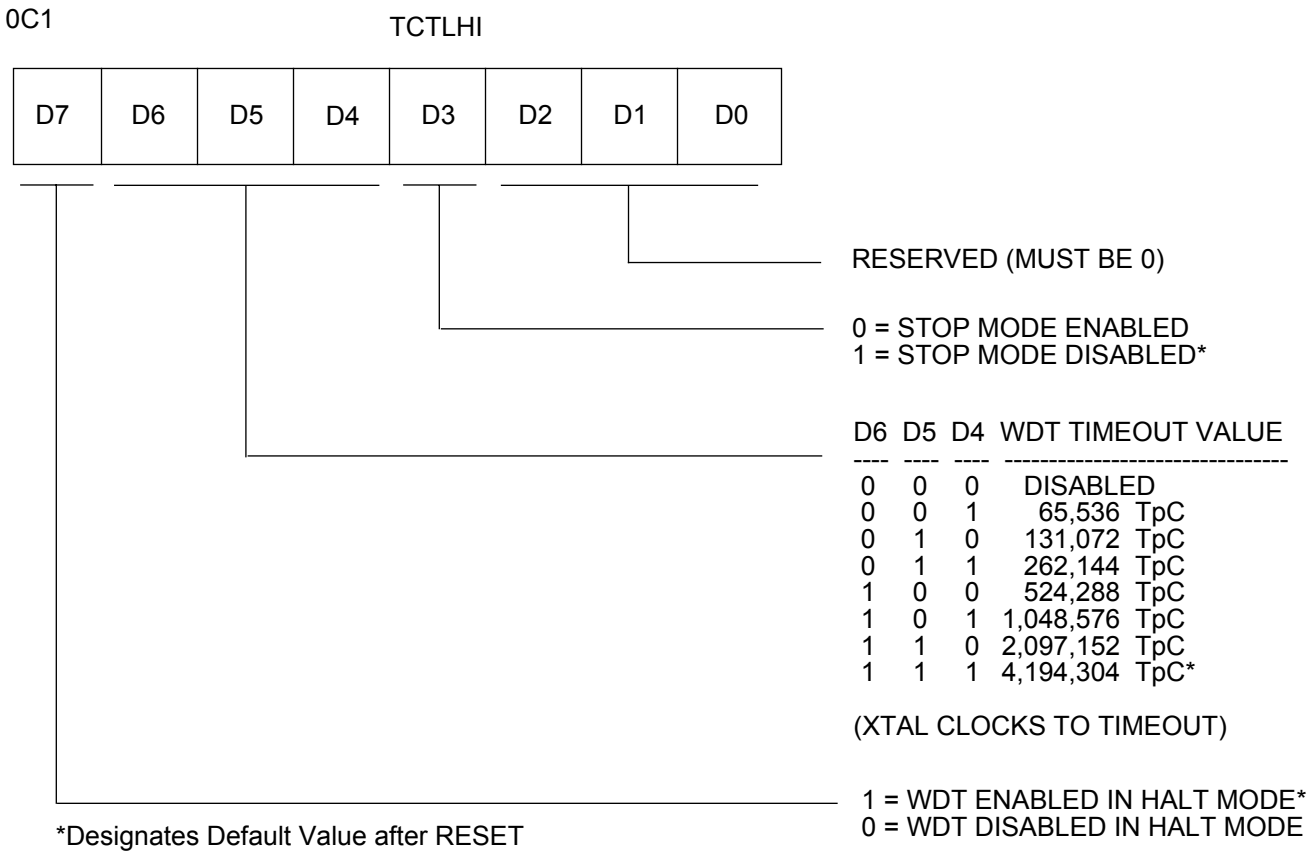


Figure 12. Z8E001 TCTLHI Register for Control of WDT

OSCILLATOR OPERATION

The Z8E001 MCU uses a Pierce oscillator with an internal feedback resistor (Figure 14). The advantages of this circuit are low-cost, large output signal, low-power level in the crystal, stability with respect to V_{CC} and temperature, and low impedances (not disturbed by stray effects).

One draw back is the requirement for high gain in the amplifier to compensate for feedback path losses. The oscillator amplifies its own noise at start-up until it settles at the frequency that satisfies the gain/phase requirements (A x B = 1; where $A = V_o/V_i$ is the gain of the amplifier and $B = V_i/V_o$ is the gain of the feedback element). The total phase shift around the loop is forced to zero (360 degrees). V_{IN} must be in phase with itself; therefore, the amplifier/inverter provides a 180-degree phase shift, and the feedback element is forced to provide the other 180-degree phase shift.

R1 is a resistive component placed from output to input of the amplifier. The purpose of this feedback is to bias the amplifier in its linear region and provide the start-up transition.

Capacitor C_2, combined with the amplifier output resistance, provides a small phase shift. It also provides some attenuation of overtones.

Capacitor C_1, combined with the crystal resistance, provides an additional phase shift.

C_1 and C_2 can affect the start-up time if they increase dramatically in size. As C_1 and C_2 increase, the start-up time increases until the oscillator reaches a point where it does not start up any more.

It is recommended for fast and reliable oscillator start-up (over the manufacturing process range) that the load capacitors be sized as low as possible without resulting in overtone operation.

Layout

Traces connecting crystal, caps, and the Z8E001 oscillator pins should be as short and wide as possible, to reduce parasitic inductance and resistance. The components (caps, crystal, resistors) should be placed as close as possible to the oscillator pins of the Z8E001.

The traces from the oscillator pins of the IC and the ground side of the lead caps should be guarded from all other traces (clock, V_{CC}, address/data lines, system ground) to reduce cross talk and noise injection. Guarding is usually accomplished by keeping other traces and system ground trace planes away from the oscillator circuit, and by placing a Z8E001 device V_{SS} ground ring around the traces/components. The ground side of the oscillator lead caps should be connected to a single trace to the Z8E001 V_{SS} (GND) pin. It should not be shared with any other system ground trace or components except at the Z8E001 device V_{SS} pin. The objective is to prevent differential system ground noise injection into the oscillator (Figure 15).

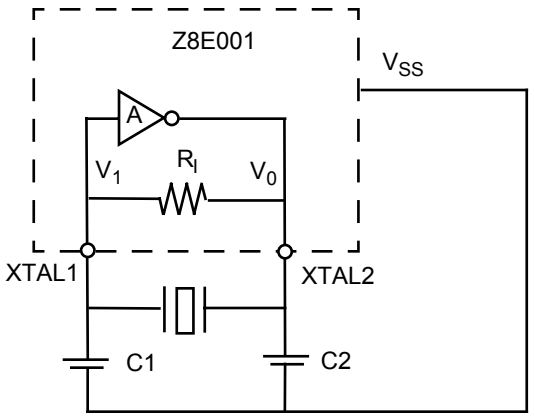


Figure 14. Pierce Oscillator with Internal Feedback Circuit

Indications of an Unreliable Design

There are two major indicators that are used in working designs to determine their reliability over full lot and temperature variations. They are:

Start-up Time. If start-up time is excessive, or varies widely from unit to unit, there is probably a gain problem. To fix the problem, the capacitors C1/C2 require reduction. The amplifier gain is either not adequate at frequency, or the crystal Rs are too large.

Output Level. The signal at the amplifier output should swing from ground to V_{CC} to indicate adequate gain in the amplifier. As the oscillator starts up, the signal amplitude grows until clipping occurs. At that point, the loop gain is effectively reduced to unity, and constant oscillation is achieved. A signal of less than 2.5 volts peak-to-peak is an indication that low gain can be a problem. Either C_1 or C_2 should be made smaller, or a low-resistance crystal should be used.

Circuit Board Design Rules

The following circuit board design rules are suggested:

- To prevent induced noise, the crystal and load capacitors should be physically located as close to the Z8E001 as possible.
- Signal lines should not run parallel to the clock oscillator inputs. In particular, the crystal input circuitry and the internal system clock output should be separated as much as possible.

TIMERS (Continued)

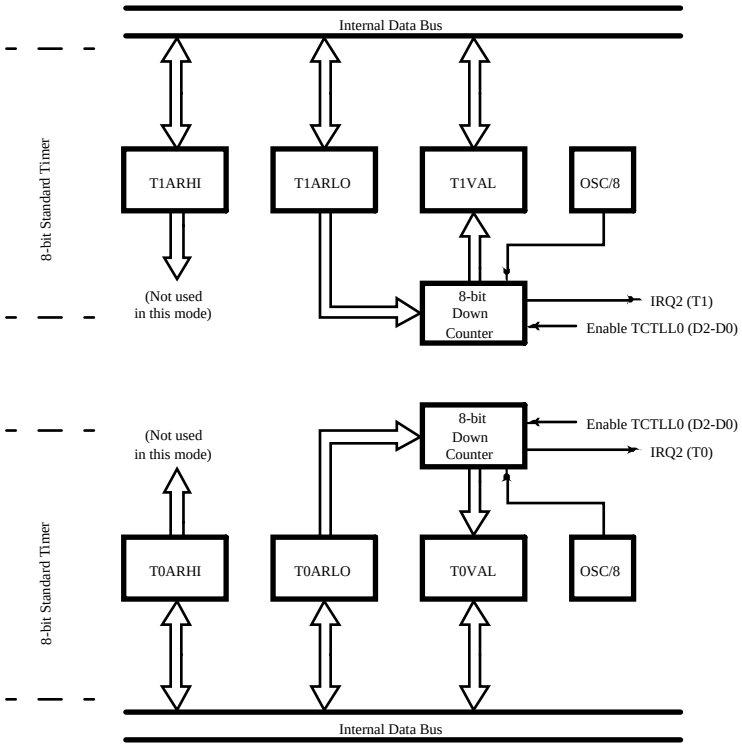


Figure 20. 8-Bit Standard Timers

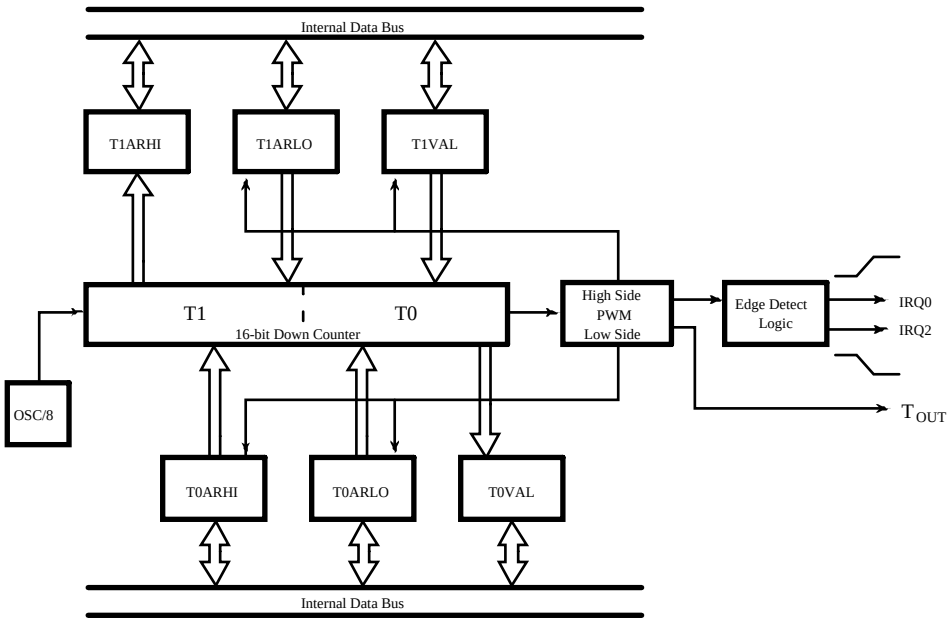


Figure 21. 16-bit Standard PWM Timer

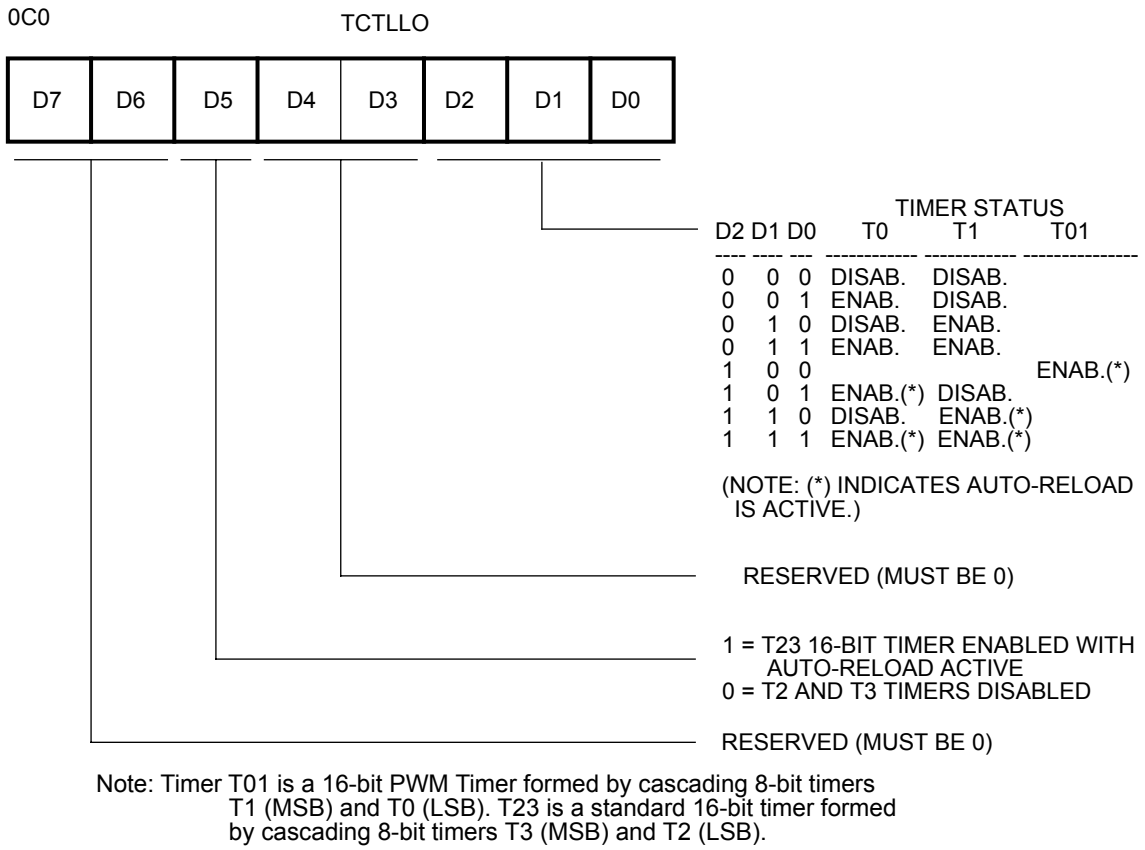


Figure 22. TCTLLO Register

Each 8-bit timer is provided a pair of registers, which are both readable and writable. One of the registers is defined to contain the auto-initialization value for the timer, while the second register contains the current value for the timer. When a timer is enabled, the timer decrements whatever value is currently held in its count register, and then continues decrementing until it reaches 0. At this time, an interrupt is generated and the contents of the auto-initialization register optionally copy into the count value register. If auto-initialization is not enabled, the timer stops counting upon reaching 0, and control logic clears the appropriate control register bit to disable the timer. This operation is referred to as "single-shot". If auto-initialization is enabled, the timer continues counting from the initialization value. Software should not attempt to use registers that are defined as having timer functionality.

Software is allowed to write to any register at any time, but care should be taken if timer registers are updated while the timer is enabled. If software updates the count value while the timer is in operation, the timer continues counting based upon the software-updated value.

Note: Strange behavior can result if the software update occurred at exactly the point that the timer was reaching 0 to trigger an interrupt and/or reload.

Similarly, if software updates the initialization value register while the timer is active, the next time that the timer reaches 0, it initializes using the updated value.

Note: Strange behavior could result if the initialization value register is being written while the timer is in the process of being initialized.

Whether initialization is done with the new or old value is a function of the exact timing of the write operation. In all cases, the Z8E001 prioritizes the software write above that of a decrementer writeback; however, when hardware clears a control register bit for a timer that is configured for single-shot operation, the clearing of the control bit overrides a software write. Reading either register can be done

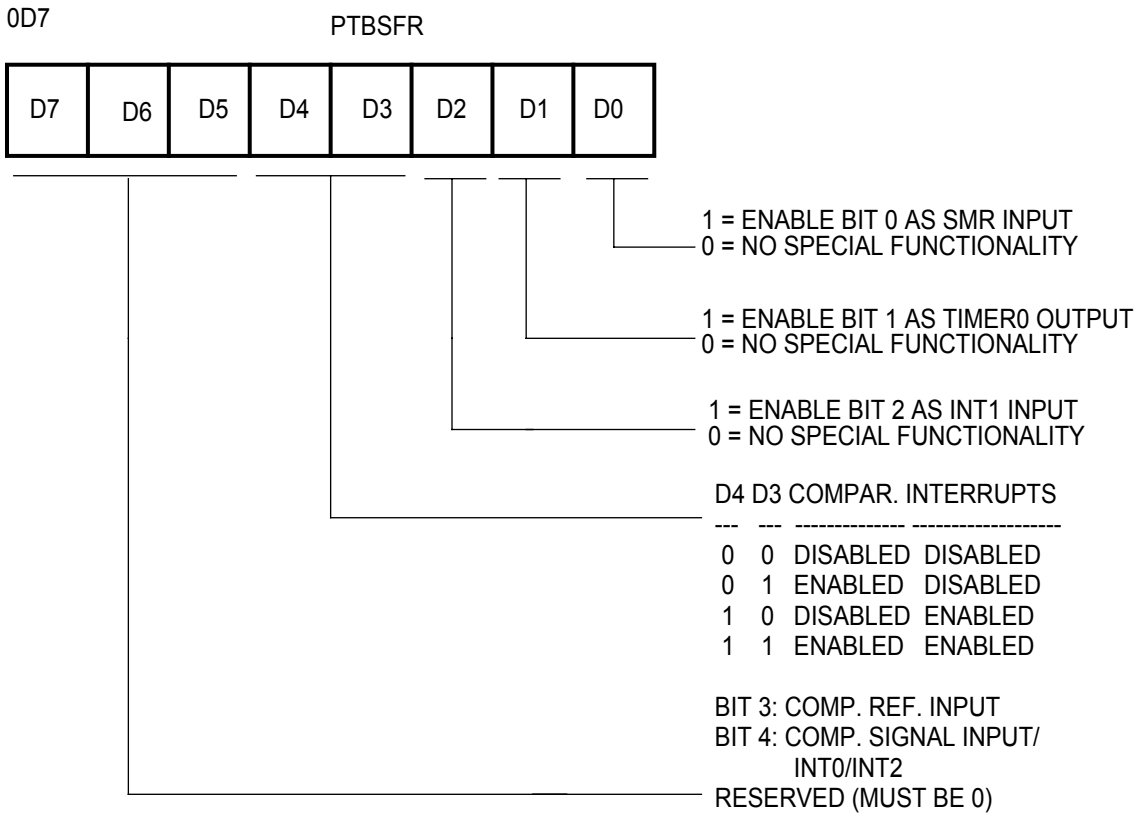


Figure 23. PortB Special Function Register (T_{out} Operation)

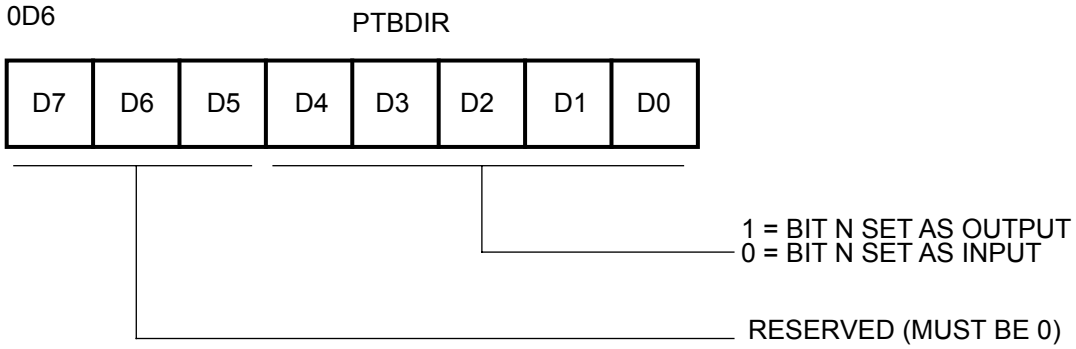


Figure 24. Port B Directional Control Register

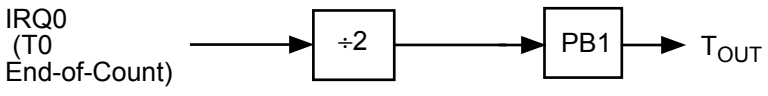


Figure 25. Timer T0 Output Through T_{OUT}

Note: The preceding result does not necessarily reflect the actual output value. If an external error is holding an output pin either High or Low against the output driver, the software read returns the *required* value, not the actual state caused by the contention. When a bit is defined as an output, the Schmitt-trigger on the input is disabled to save power.

Updates to the output register takes effect based upon the timing of the internal instruction pipeline, but is referenced to the rising edge of the clock. The output register can be read at any time, and returns the current output value that is held. No restrictions are placed on the timing of reads and/or writes to any of the port registers with respect to the others; however, care should be taken when updating the directional control and special function registers.

When updating a Directional Control Register, the Special Function Register should first be disabled. If this precaution is not taken, spurious events could take place as a result of the change in port I/O status. This precaution is especially important when defining changes in Port B, as the spurious event referred to above could be one or more interrupts. Clearing of the SFR register should be the first step in configuring the port, while setting the SFR register should be the final step in the port configuration process. To ensure deterministic behavior, the SFR register should not be written until the pins are being driven appropriately, and all initialization has been completed.

PORT A

Port A is a general-purpose port. Figure 26 features a block diagram of Port A. Each of its lines can be independently programmed as input or output via the Port A Directional Control Register (PTADIR at 0D2H) as seen in Figure 27. A bit set to a 1 in PTADIR configures the corresponding bit in Port A as an output, while a bit cleared to 0 configures the corresponding bit in Port A as an input.

The input buffers are Schmitt-triggered. Bits programmed as outputs can be individually programmed as either push-pull or open drain by setting the corresponding bit in the Special Function Register (PTASFR, Figure 27).

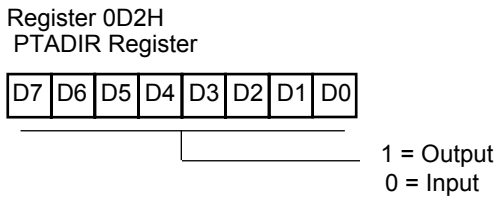


Figure 26. Port A Directional Control Register

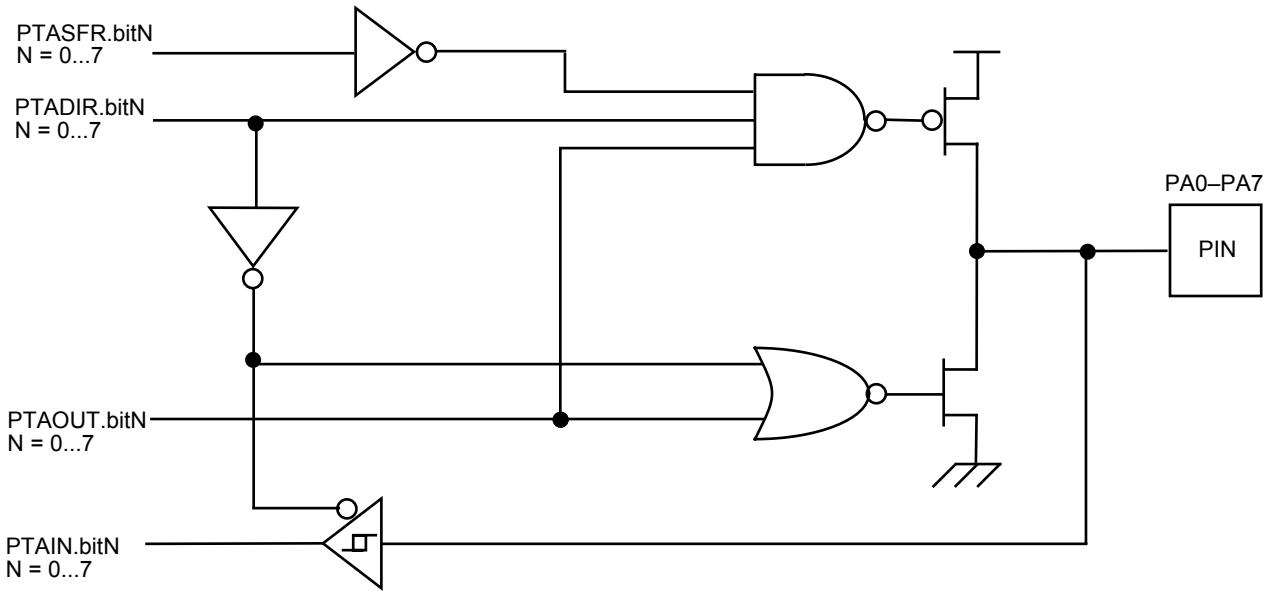


Figure 27. Port A Configuration with Open-Drain Capability and Schmitt-Trigger

PORT A REGISTER DIAGRAMS

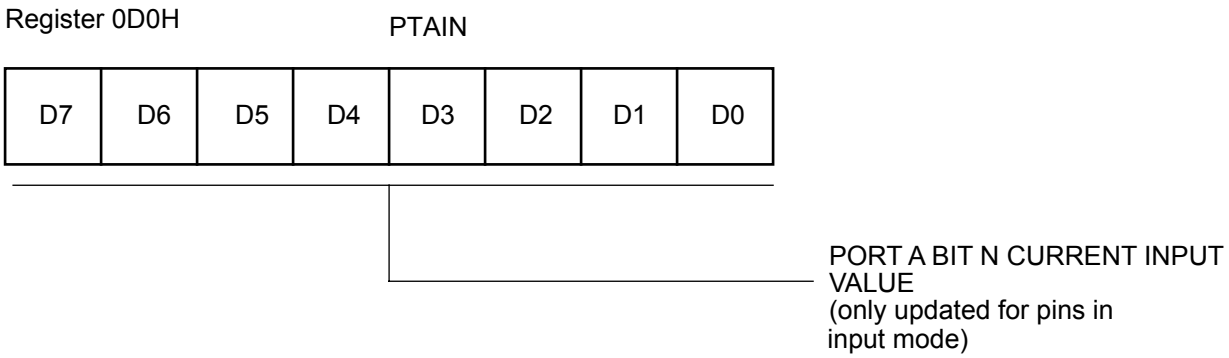


Figure 28. Port A Input Value Register

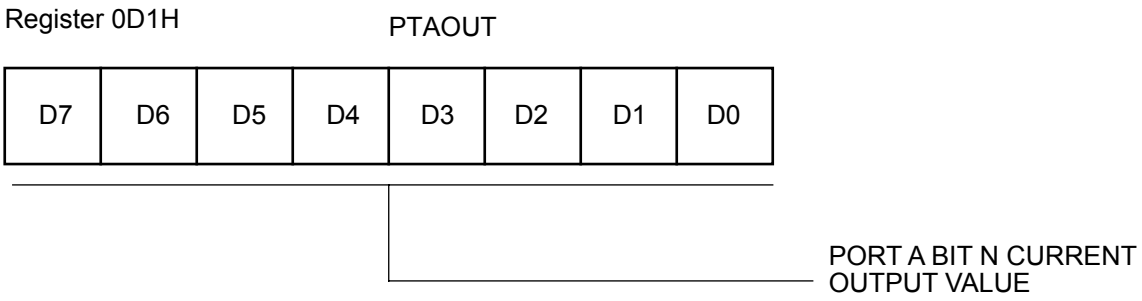


Figure 29. Port A Output Value Register

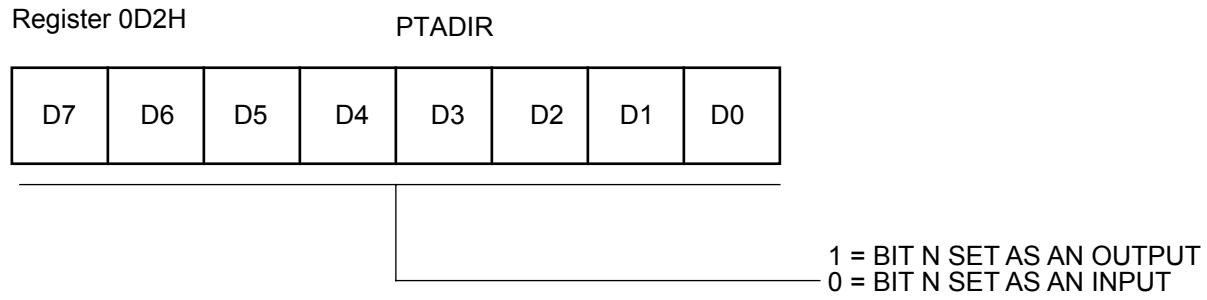


Figure 30. Port A Directional Control Register

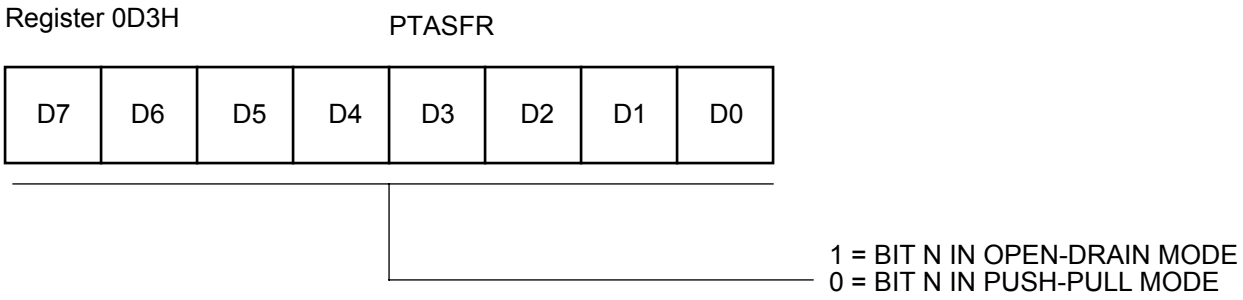


Figure 31. Port A Special Function Register

PORT B

Port B Description

Port B is a 5-bit (bidirectional), CMOS-compatible I/O port. These five I/O lines can be configured under software control to be an input or output, independently. Input buffers are Schmitt-triggered. See Figure 33 through Figure 36 for diagrams of all five Port B pins.

In addition to standard input/output capability on all five pins of Port B, each pin provides special functionality as shown in the following table:

Special functionality is invoked via the Port B Special Function Register. See Figure 32 for the arrangement and control conventions of this register.

Table 8. Port B Special Functions

Port Pin	Input Special Function	Output Special Function
PB0	Stop Mode Recovery Input	None
PB1	None	Timer0 Output
PB2	IRQ3	None
PB3	Comparator Reference Input	None
PB4	Comparator Signal Input/IRQ1/IRQ4	None

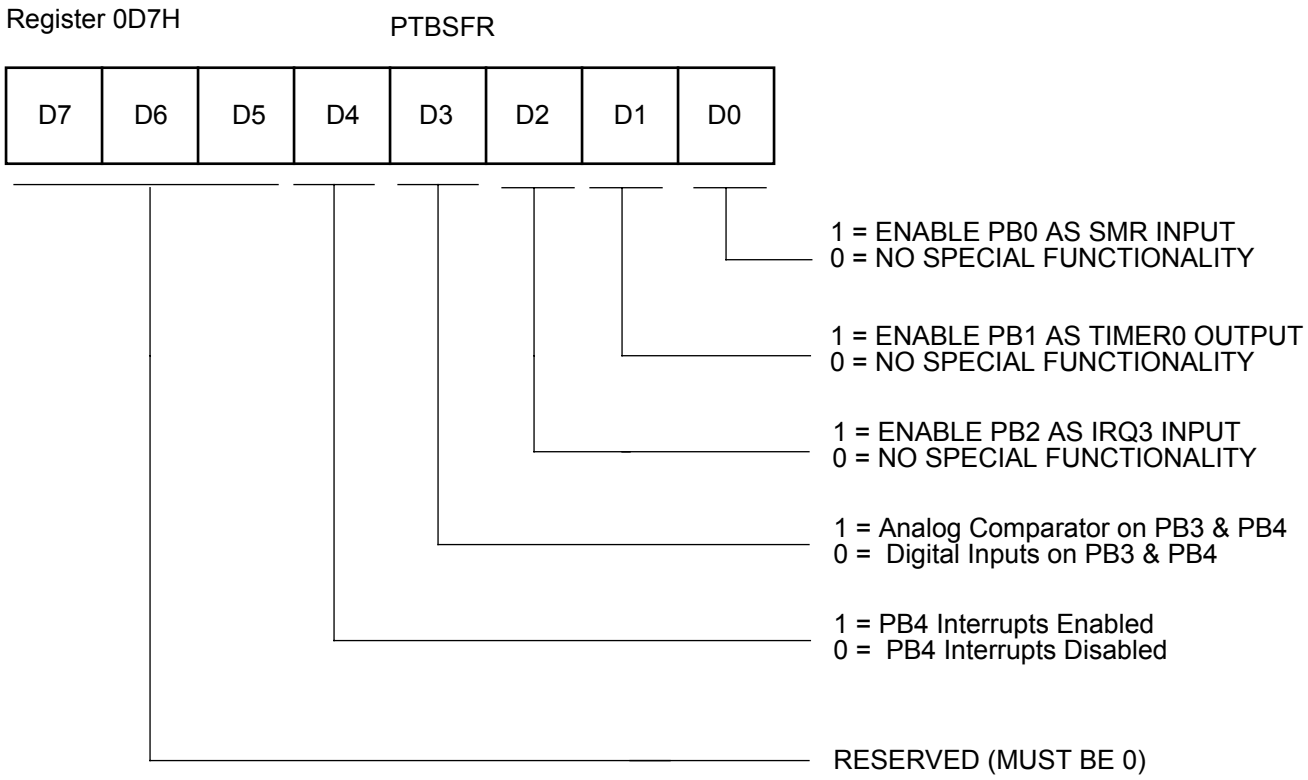


Figure 32. Port B Special Function Register

PORT B—PIN 0 CONFIGURATION

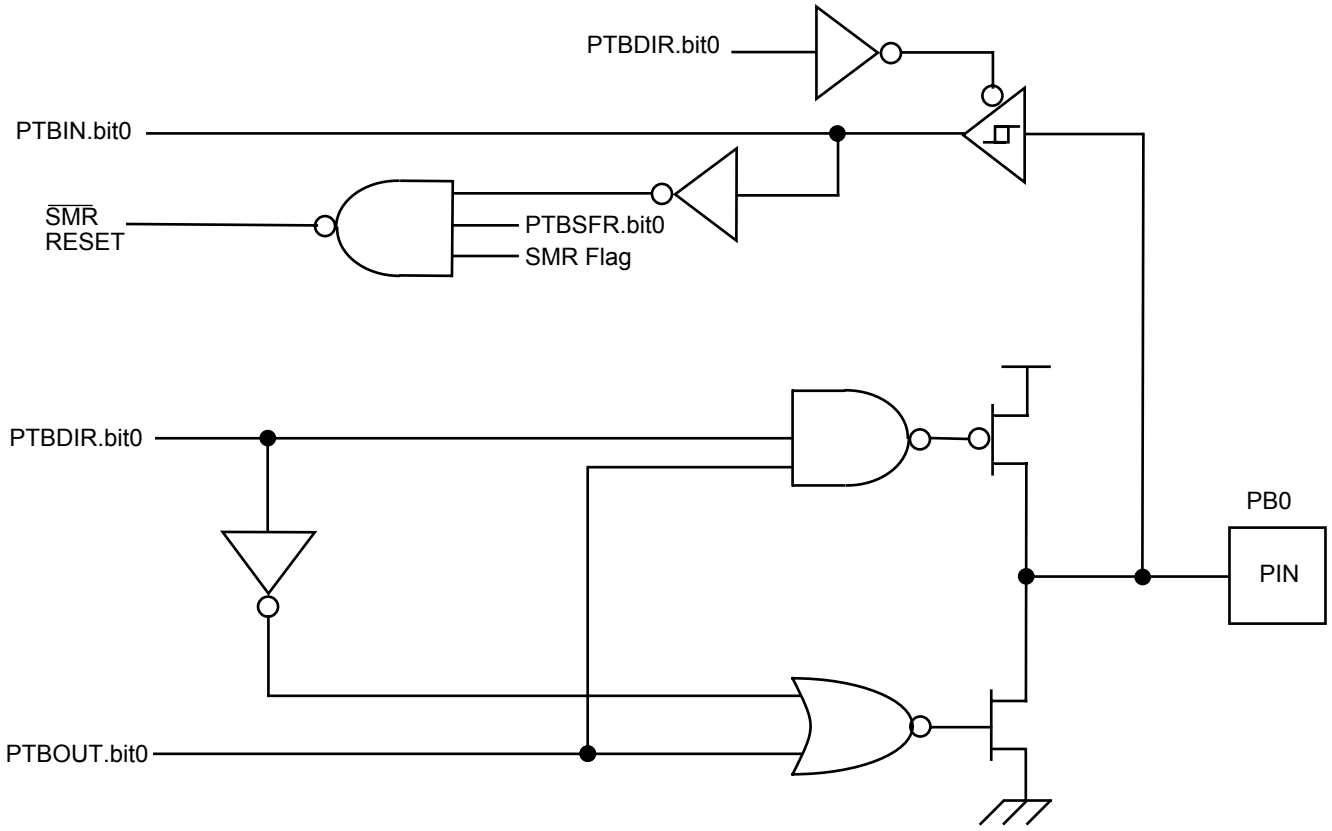


Figure 33. Port B Pin 0 Diagram

PORT B—PIN 2 CONFIGURATION

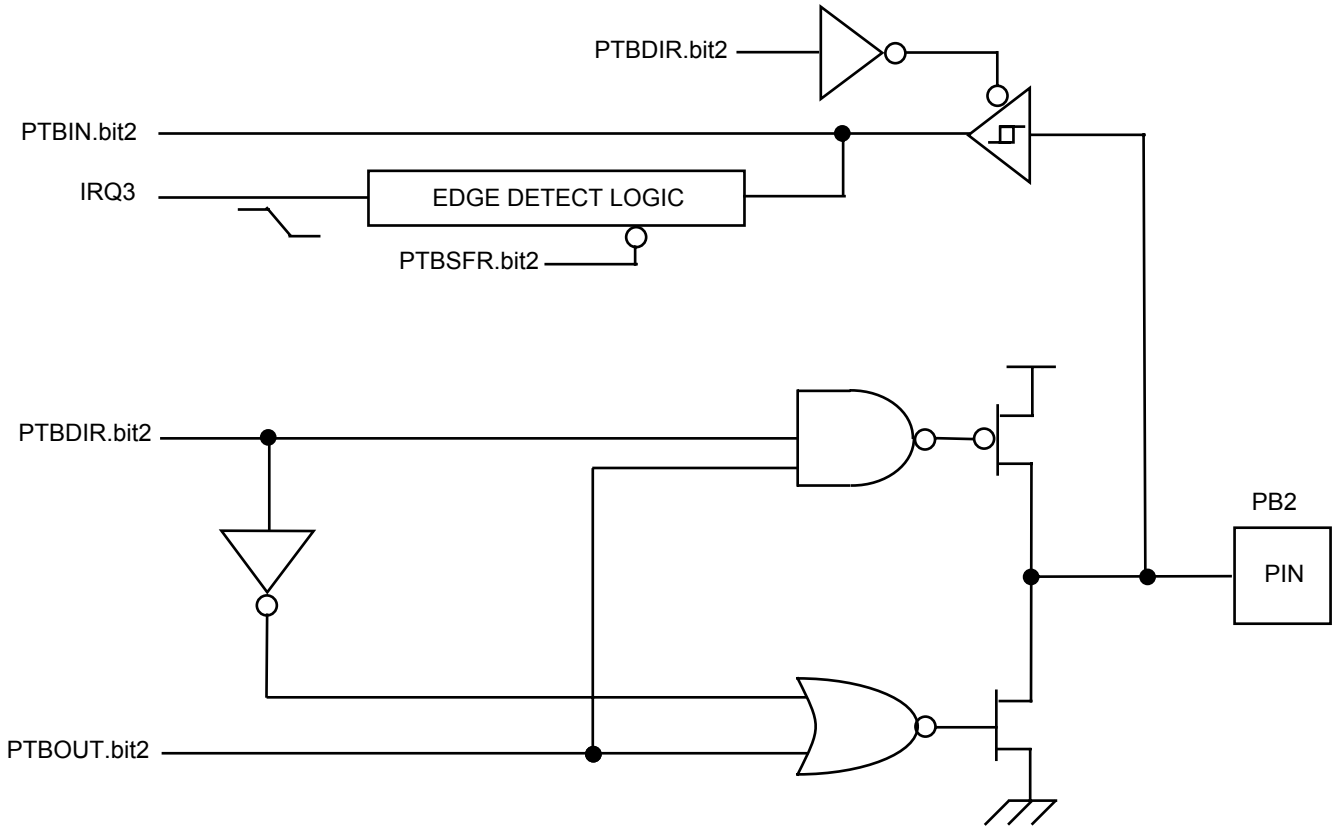


Figure 35. Port B Pin 2 Diagram

PORT B—PINS 3 AND 4 CONFIGURATION

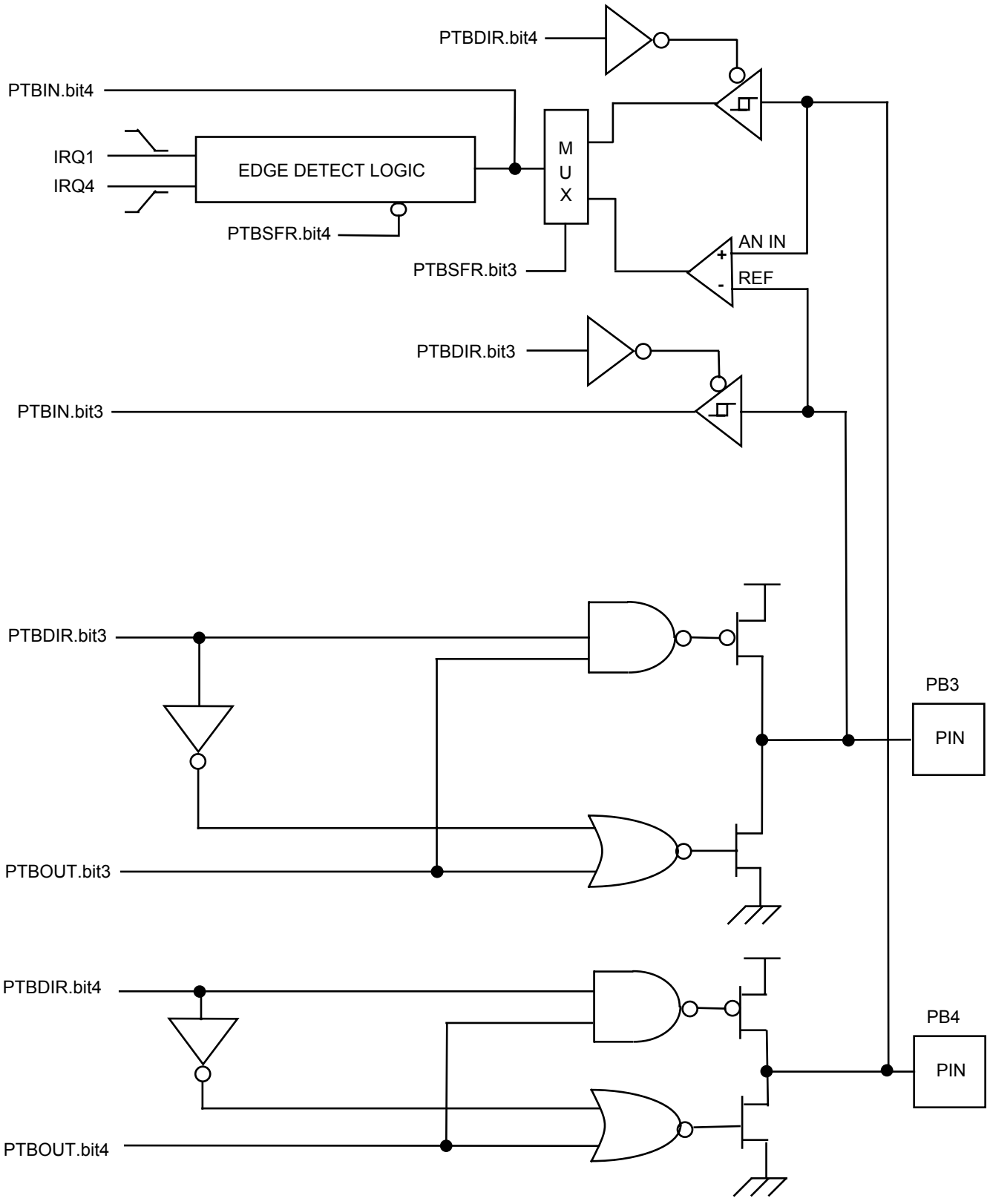
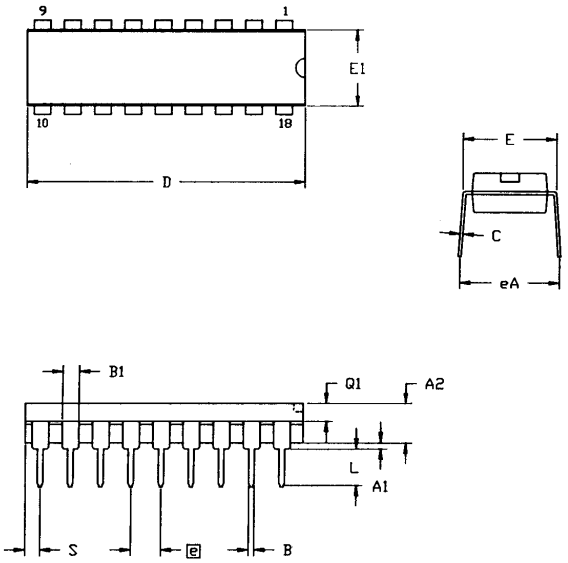


Figure 36. Port B Pins 3 and 4 Diagram

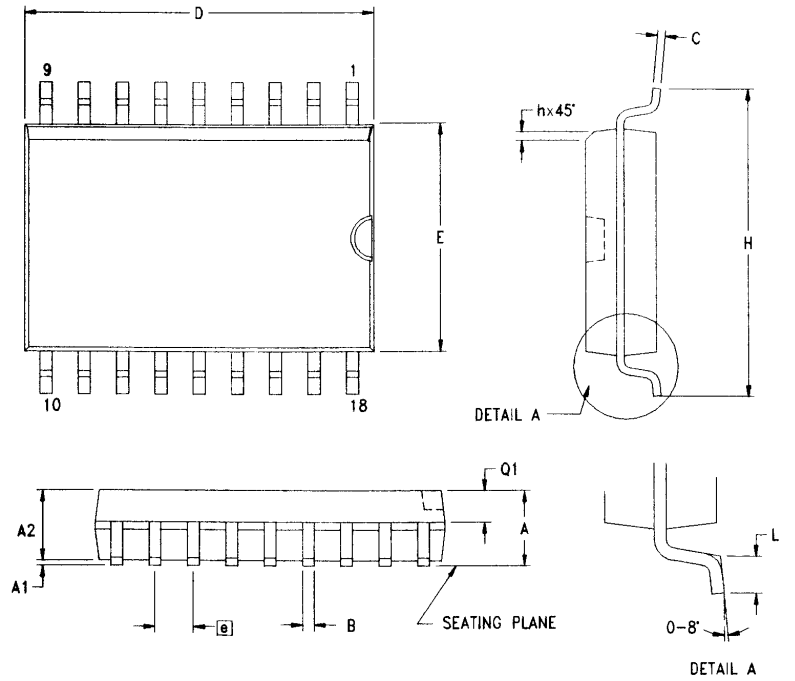
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

Figure 43. 18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
e	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 44. 18-Pin SOIC Package Diagram

Pre-Characterization Product:

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or non-conformance with some aspects of the document may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

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