Zilog - Z8E00110PEG Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	PWM, WDT
Number of I/O	13
Program Memory Size	1KB (1K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8e00110peg

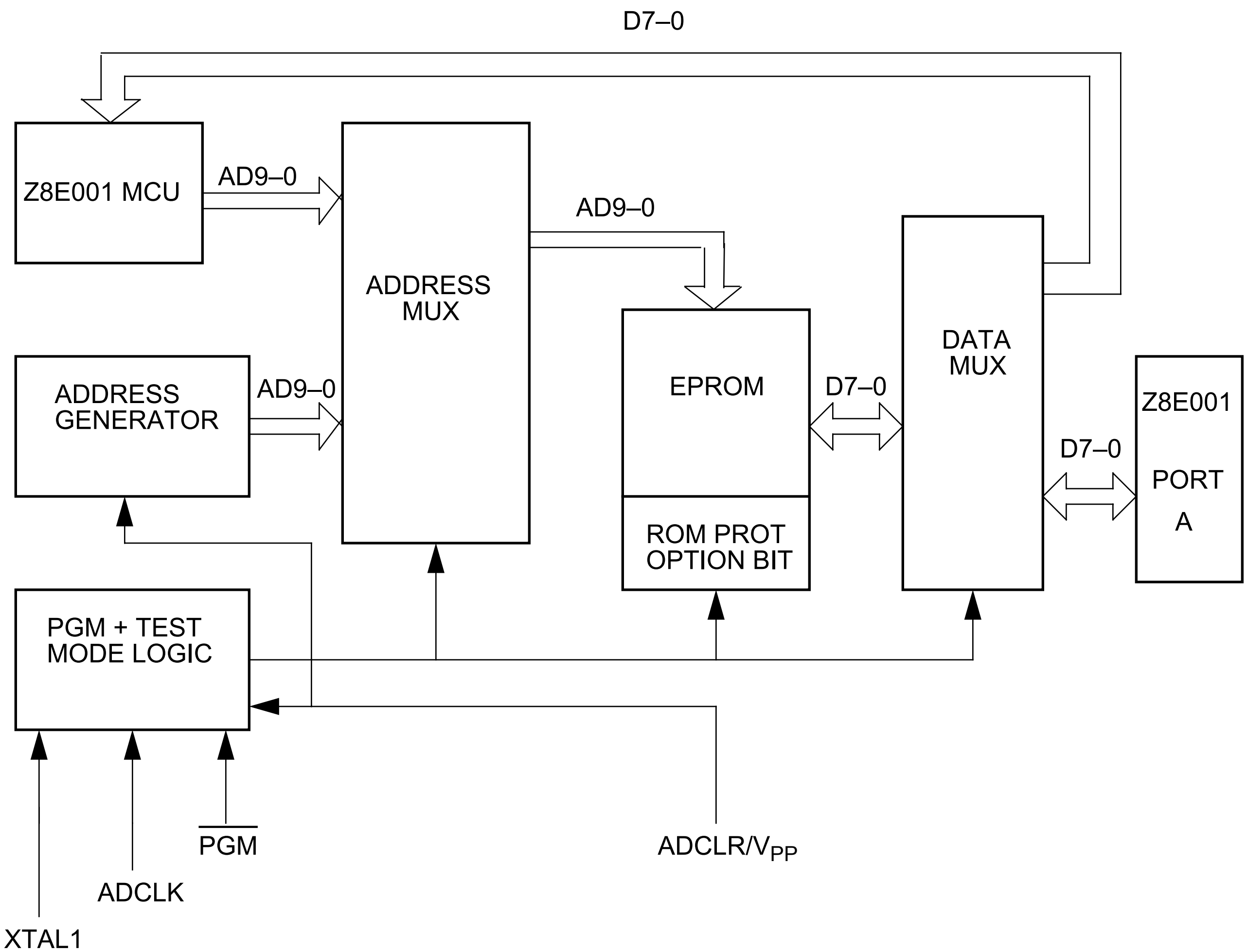


Figure 2. EPROM Programming Mode Block Diagram

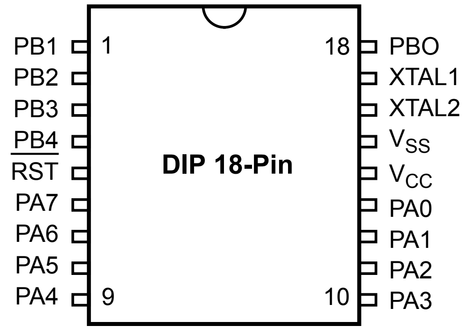


Figure 4. 18-Pin DIP/SOIC Pin Identification

Standard Mode

Pin #	Symbol	Function	Direction
1–4	PB1–PB4	Port B, Pins 1,2,3,4	Input/Output
5	$\overline{\text{RESET}}$	Reset	Input
6-9	PA7–PA4	Port A, Pins 7,6,5,4	Input/Output
10–13	PA3–PA0	Port A, Pins 3,2,1,0	Input/Output
14	V_{CC}	Power Supply	
15	V_{SS}	Ground	
16	XTAL2	Crystal Osc. Clock	Output
17	XTAL1	Crystal Osc. Clock	Input
18	PB0	Port B, Pin 0	Input/Output

PIN DESCRIPTION (Continued)

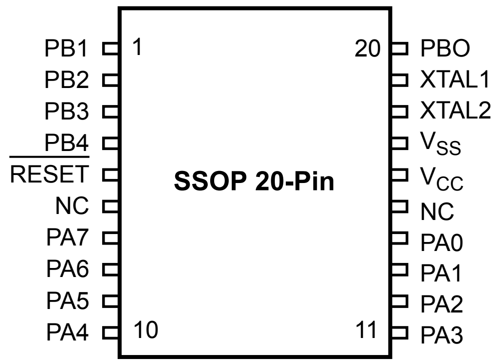


Figure 5. 20-Pin SSOP Pin Identification

Standard Mode

Pin #	Symbol	Function	Direction
1–4	PB1–PB4	Port B, Pins 1,2,3,4	Input/Output
5	RESET	Reset	Input
6	NC	No Connection	
7–10	PA7–PA4	Port A, Pins 7,6,5,4	Input/Output
11–14	PA3–PA0	Port A, Pins 3,2,1,0	Input/Output
15	NC	No Connection	
16	V_{CC}	Power Supply	
17	V_{SS}	Ground	
18	XTAL2	Crystal Osc. Clock	Output
19	XTAL1	Crystal Osc. Clock	Input
20	PB0	Port B, Pin 0	Input/Output

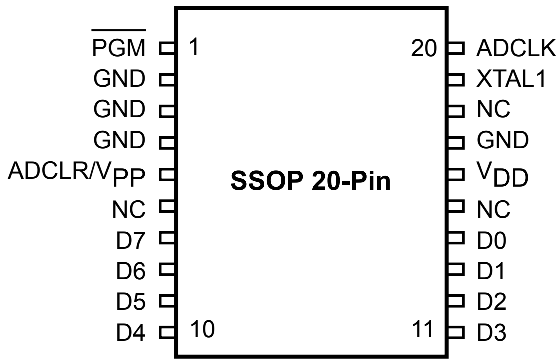


Figure 6. 20-Pin SSOP Pin Identification/EPROM Programming Mode

EPROM Programming Mode

Pin #	Symbol	Function	Direction
1	$\overline{\text{PGM}}$	Prog Mode	Input
2–4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clk./Prog Volt.	Input
6	NC	No Connection	
7–10	D7–D4	Data 7,6,5,4	Input/Output
11–14	D3–D0	Data 3,2,1,0	Input/Output
15	NC	No Connection	
16	V_{DD}	Power Supply	
17	GND	Ground	
18	NC	No Connection	
19	XTAL1	1MHz Clock	Input
20	ADCLK	Address Clock	Input

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units	Note
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on $\overline{RESET}$ Pin with Respect to V_{SS}	–0.6	V_{DD}+1	V	2
Total Power Dissipation		880	mW	
Maximum Allowable Current out of V_{SS}		80	mA	
Maximum Allowable Current into V_{DD}		80	mA	
Maximum Allowable Current into an Input Pin	–600	+600	mA	3
Maximum Allowable Current into an Open-Drain Pin	–600	+600	mA	4
Maximum Allowable Output Current Sunk by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sunk by Port A		40	mA	
Maximum Allowable Output Current Sourced by Port A		40	mA	
Maximum Allowable Output Current Sunk by Port B		40	mA	
Maximum Allowable Output Current Sourced by Port B		40	mA	

Notes:

1. Applies to all pins except the $\overline{RESET}$ pin and where otherwise noted.
2. There is no input protection diode from pin to V_{DD}.
3. Excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings can cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period can affect device reliability. Total power dissipation should not exceed 880 mW for the package. Power dissipation is calculated as follows:

Total Power Dissipation $= V_{DD} \times [I_{DD} - (\text{sum of } I_{OH})]$
$+ \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}]$
$+ \text{sum of } (V_{0L} \times I_{0L})$

Table 1. DC Electrical Characteristics (Continued)

Sym	Parameter	V_{CC}[1]	pF T_A = 0°C to +70°C Standard Temperatures Min	Max	Typical[2] @ 25°C	Units	Conditions	Notes
I_{CC}	Supply Current	3.5V		2.5	2.0	mA	@ 10 MHz	4,5
		5.5V		6.0	3.5	mA	@ 10 MHz	4,5
I_{CC1}	Standby Current	3.5V		2.0	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 10 MHz	4,5
		5.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 10 MHz	4,5
I_{CC2}	Standby Current	3.5V		500	150	nA	STOP Mode V_{IN} = 0V, V_{CC}	6

Notes:
1. The V_{CC} voltage specification of 3.5V guarantees 3.5V and the V_{CC} voltage specification of 5.5 V guarantees 5.0 V ±0.5 V.
2. Typical values are measured at V_{CC} = 3.3V and V_{CC} = 5.0V; V_{SS} = 0V = GND.
3. For analog comparator input when analog comparator is enabled.
4. All outputs unloaded and all inputs are at V_{CC} or V_{SS} level.
5. CL1 = CL2 = 22 pF.
6. Same as note 4 except inputs at V_{CC}.

Z8PLUS CORE

The Z8E001 is based on the ZiLOG Z8Plus Core Architecture. This core is capable of addressing up to 64KBytes of program memory and 4KBytes of RAM. Register RAM is accessed as either 8 or 16 bit registers using a combination of 4, 8, and 12 bit addressing modes. The architecture supports up to 15 vectored interrupts from external and internal sources. The processor decodes 44 CISC instructions using six addressing modes. See the Z8Plus User's Manual for more information.

RESET

This section describes the Z8E001 reset conditions, reset timing, and register initialization procedures. Reset is generated by the Reset Pin, Watch-Dog Timer (WDT), and Stop-Mode Recovery (SMR).

A system reset overrides all other operating conditions and puts the Z8E001 into a known state. To initialize the chip's internal logic, the RESET input must be held Low for at least 30 XTAL clock cycles. The control registers and ports are reset to their default conditions after a reset from the RESET pin. The control registers and ports are not reset to their default conditions after wakeup from Stop Mode or WDT timeout.

During $\overline{\text{RESET}}$, the program counter is loaded with 0020H. I/O ports and control registers are configured to their default reset state. Resetting the Z8E001 does not affect the contents of the general-purpose registers.

RESET PIN OPERATION

The Z8E001 hardware $\overline{\text{RESET}}$ pin initializes the control and peripheral registers, as shown in Table 4. Specific reset values are shown by 1 or 0, while bits whose states are unchanged or unknown from Power-Up are indicated by the letter U.

$\overline{\text{RESET}}$ must be held Low until the oscillator stabilizes, for an additional 30 XTAL clock cycles, in order to be sure that the internal reset is complete. The RESET pin has a Schmitt-Trigger input with a trip point. There is no High side protection diode. The user should place an external diode from $\overline{\text{RESET}}$ to V_{CC}. A pull-up resistor on the $\overline{\text{RESET}}$ pin is approximately 500 KΩ, typical.

Program execution starts 10 XTAL clock cycles after $\overline{\text{RESET}}$ has returned High. The initial instruction fetch is from location 0020H. Figure 9 indicates reset timing.

After a reset, the first routine executed must be one that initializes the TCTLHI control register to the required system configuration, followed by initialization of the remaining control registers.

Table 4. Control and Peripheral Registers

		Bits								
Register (HEX)	**Register Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**
FF	Stack Pointer	0	0	U	U	U	U	U	U	Stack pointer is not affected by RESET
FE	Reserved									
FD	Register Pointer	U	U	U	U	0	0	0	0	Register pointer is not affected by RESET
FC	Flags	U	U	U	U	U	U	*	*	Only WDT & SMR flags are affected by RESET
FB	Interrupt Mask	0	0	0	0	0	0	0	0	All interrupts masked by $\overline{\text{RESET}}$
FA	Interrupt Request	0	0	0	0	0	0	0	0	All interrupt requests cleared by RESET
F9–F0	Reserved									
EF–E0	Virtual Copy									Virtual Copy of the Current Working Register Set
DF–D8	Reserved									

Table 5. Flag Register Bit D1, D0

D1	D0	Reset Source
0	0	RESET Pin
0	1	SMR Recovery
1	0	WDT Reset
1	1	Reserved

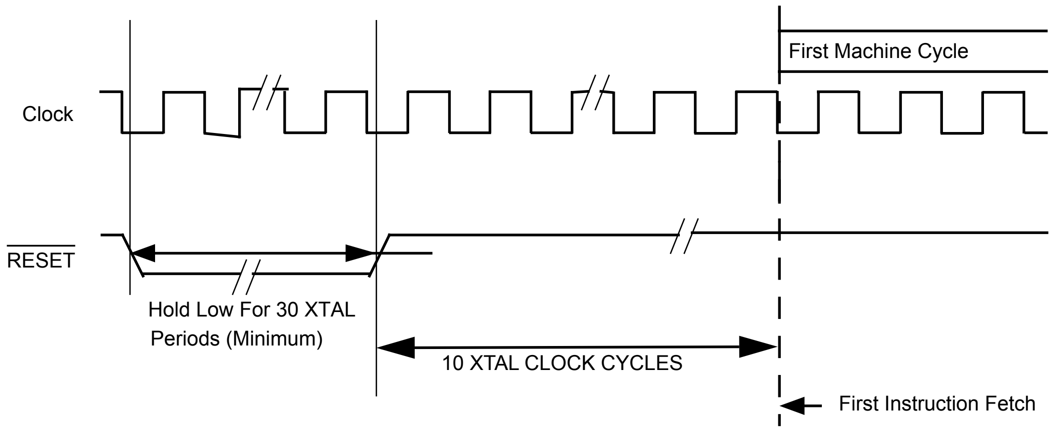


Figure 9. Reset Timing

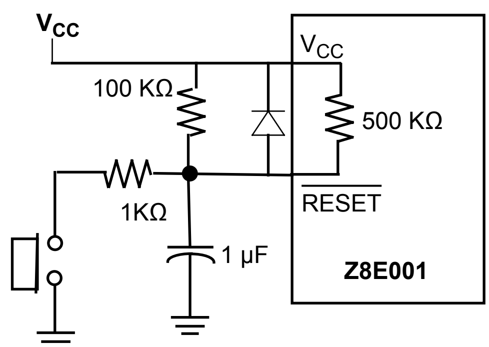


Figure 10. Example of External Power-On Reset (POR) Circuit

STOP MODE OPERATION

The STOP Mode provides the lowest possible device stand-by current. This instruction turns off the on-chip oscillator and internal system clock.

To enter the STOP Mode, the Z8E001 only requires a STOP instruction. It is NOT necessary to execute a NOP instruction immediately before the STOP instruction.

```
6F    STOP    ;enter STOP Mode
```

The STOP Mode is exited by any one of the following resets: RESET pin or a STOP-Mode Recovery source. Upon reset generation, the processor always restarts the application program at address 0020H, and the STOP Mode Flag is set. Reading the STOP Mode Flag does not clear it. The user must clear the STOP Mode Flag with software.

Note: Failure to clear the STOP Mode Flag can result in undefined behavior.

The Z8E001 provides a dedicated STOP-Mode Recovery (SMR) circuit. In this case, a low-level applied to input pin PB0 triggers an SMR. To use this mode, pin PB0 (I/O Port B, bit 0) must be configured as an input before the STOP Mode is entered. The Low level on PB0 must be held for a minimum pulse width T_{WSM} plus any oscillator startup time. Program execution starts at address 20Hex after PB0 is raised back to a high level.

Notes: Use of the PB0 input for the stop mode recovery does not initialize the control registers.

The STOP Mode current (I_{CC2}) is minimized when:

- V_{CC} is at the low end of the devices operating range.
- Output current sourcing is minimized.
- All inputs (digital and analog) are at the Low or High rail voltages.

CLOCK

The Z8E001 MCU derives its timing from on-board clock circuitry connected to pins XTAL1 and XTAL2. The clock circuitry consists of an oscillator, a glitch filter, a divide-by-two shaping circuit, a divide-by-four shaping circuit, and a divide-by-eight shaping circuit. Figure 13 illustrates the clock circuitry. The oscillator's input is XTAL1 and its output is XTAL2. The clock can be driven by a crystal, a ceramic resonator, LC clock, or an external clock source.

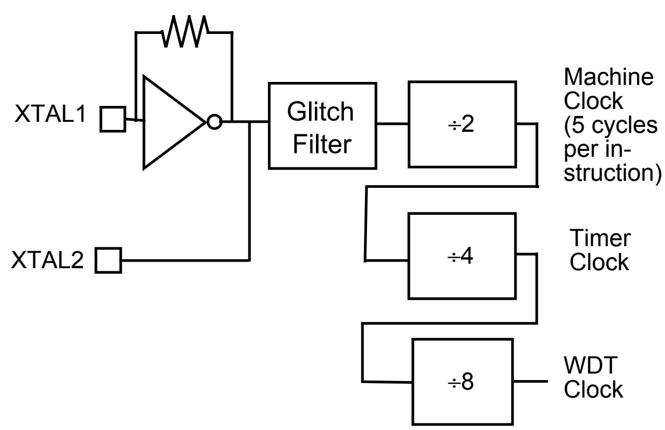


Figure 13. Z8E001 Clock Circuit

OSCILLATOR OPERATION

The Z8E001 MCU uses a Pierce oscillator with an internal feedback resistor (Figure 14). The advantages of this circuit are low-cost, large output signal, low-power level in the crystal, stability with respect to V_{CC} and temperature, and low impedances (not disturbed by stray effects).

One draw back is the requirement for high gain in the amplifier to compensate for feedback path losses. The oscillator amplifies its own noise at start-up until it settles at the frequency that satisfies the gain/phase requirements (A x B = 1; where $A = V_0/V_i$ is the gain of the amplifier and $B = V_i/V_0$ is the gain of the feedback element). The total phase shift around the loop is forced to zero (360 degrees). V_{IN} must be in phase with itself; therefore, the amplifier/inverter provides a 180-degree phase shift, and the feedback element is forced to provide the other 180-degree phase shift.

R1 is a resistive component placed from output to input of the amplifier. The purpose of this feedback is to bias the amplifier in its linear region and provide the start-up transition.

Capacitor C_2, combined with the amplifier output resistance, provides a small phase shift. It also provides some attenuation of overtones.

Capacitor C_1, combined with the crystal resistance, provides an additional phase shift.

C_1 and C_2 can affect the start-up time if they increase dramatically in size. As C_1 and C_2 increase, the start-up time increases until the oscillator reaches a point where it does not start up any more.

It is recommended for fast and reliable oscillator start-up (over the manufacturing process range) that the load capacitors be sized as low as possible without resulting in overtone operation.

Layout

Traces connecting crystal, caps, and the Z8E001 oscillator pins should be as short and wide as possible, to reduce parasitic inductance and resistance. The components (caps, crystal, resistors) should be placed as close as possible to the oscillator pins of the Z8E001.

The traces from the oscillator pins of the IC and the ground side of the lead caps should be guarded from all other traces (clock, V_{CC}, address/data lines, system ground) to reduce cross talk and noise injection. Guarding is usually accomplished by keeping other traces and system ground trace planes away from the oscillator circuit, and by placing a Z8E001 device V_{SS} ground ring around the traces/components. The ground side of the oscillator lead caps should be connected to a single trace to the Z8E001 V_{SS} (GND) pin. It should not be shared with any other system ground trace or components except at the Z8E001 device V_{SS} pin. The objective is to prevent differential system ground noise injection into the oscillator (Figure 15).

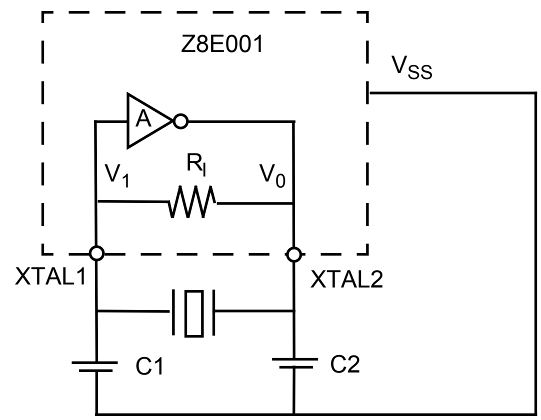


Figure 14. Pierce Oscillator with Internal Feedback Circuit

Indications of an Unreliable Design

There are two major indicators that are used in working designs to determine their reliability over full lot and temperature variations. They are:

Start-up Time. If start-up time is excessive, or varies widely from unit to unit, there is probably a gain problem. To fix the problem, the capacitors C1/C2 require reduction. The amplifier gain is either not adequate at frequency, or the crystal Rs are too large.

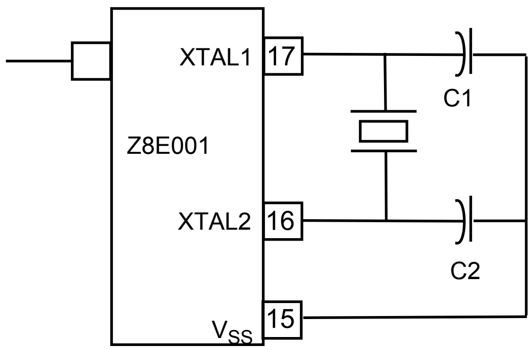
Output Level. The signal at the amplifier output should swing from ground to V_{CC} to indicate adequate gain in the amplifier. As the oscillator starts up, the signal amplitude grows until clipping occurs. At that point, the loop gain is effectively reduced to unity, and constant oscillation is achieved. A signal of less than 2.5 volts peak-to-peak is an indication that low gain can be a problem. Either C_1 or C_2 should be made smaller, or a low-resistance crystal should be used.

Circuit Board Design Rules

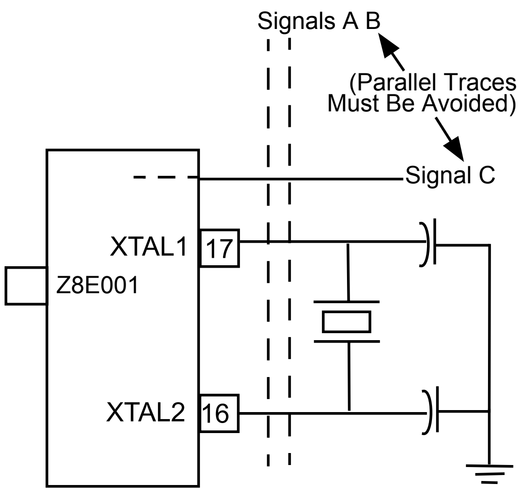
The following circuit board design rules are suggested:

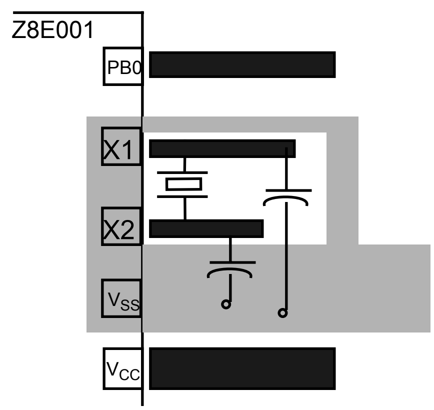
- To prevent induced noise, the crystal and load capacitors should be physically located as close to the Z8E001 as possible.
- Signal lines should not run parallel to the clock oscillator inputs. In particular, the crystal input circuitry and the internal system clock output should be separated as much as possible.

- V_{CC} power lines should be separated from the clock oscillator input circuitry.
- Resistivity between XTAL1 or XTAL2 (and the other pins) should be greater than 10 MΩ.



Clock Generator Circuit





Board Design Example
(Top View)

Figure 15. Circuit Board Design Rules

Crystals and Resonators

Crystals and ceramic resonators (Figure 16) should have the following characteristics to ensure proper oscillation:

Crystal Cut	AT (crystal only)
Mode	Parallel, Fundamental Mode
Crystal Capacitance	<7pF
Load Capacitance	10pF < CL < 220 pF,
	15 typical
Resistance	100 ohms max

Depending on the operation frequency, the oscillator can require additional capacitors, C1 and C2, as shown in Figure 16 and Figure 17. The capacitance values are dependent on the manufacturerÕs crystal specifications.

Note: The preceding result does not necessarily reflect the actual output value. If an external error is holding an output pin either High or Low against the output driver, the software read returns the *required* value, not the actual state caused by the contention. When a bit is defined as an output, the Schmitt-trigger on the input is disabled to save power.

Updates to the output register takes effect based upon the timing of the internal instruction pipeline, but is referenced to the rising edge of the clock. The output register can be read at any time, and returns the current output value that is held. No restrictions are placed on the timing of reads and/or writes to any of the port registers with respect to the others; however, care should be taken when updating the directional control and special function registers.

When updating a Directional Control Register, the Special Function Register should first be disabled. If this precaution is not taken, spurious events could take place as a result of the change in port I/O status. This precaution is especially important when defining changes in Port B, as the spurious event referred to above could be one or more interrupts. Clearing of the SFR register should be the first step in configuring the port, while setting the SFR register should be the final step in the port configuration process. To ensure deterministic behavior, the SFR register should not be written until the pins are being driven appropriately, and all initialization has been completed.

PORT A

Port A is a general-purpose port. Figure 26 features a block diagram of Port A. Each of its lines can be independently programmed as input or output via the Port A Directional Control Register (PTADIR at 0D2H) as seen in Figure 27. A bit set to a 1 in PTADIR configures the corresponding bit in Port A as an output, while a bit cleared to 0 configures the corresponding bit in Port A as an input.

The input buffers are Schmitt-triggered. Bits programmed as outputs can be individually programmed as either push-pull or open drain by setting the corresponding bit in the Special Function Register (PTASFR, Figure 27).

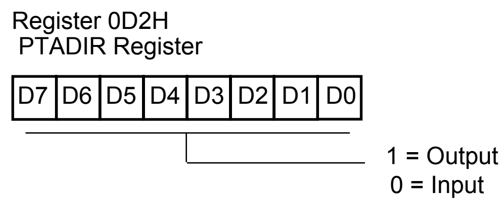


Figure 26. Port A Directional Control Register

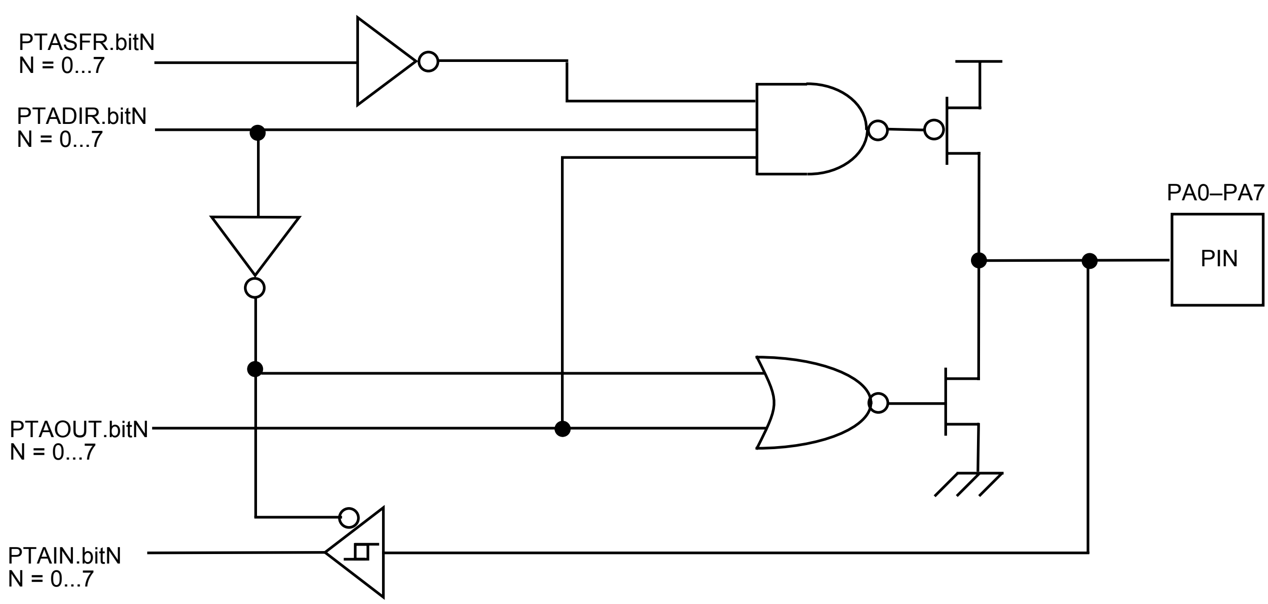


Figure 27. Port A Configuration with Open-Drain Capability and Schmitt-Trigger

PORT A REGISTER DIAGRAMS

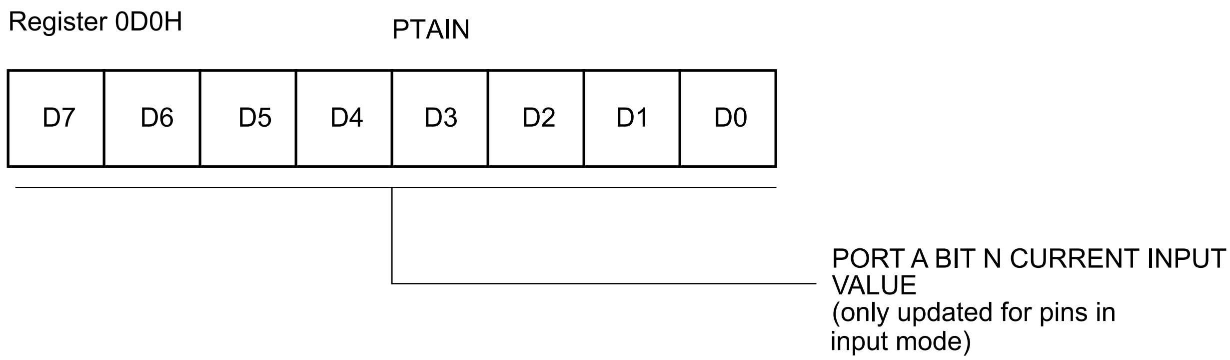


Figure 28. Port A Input Value Register

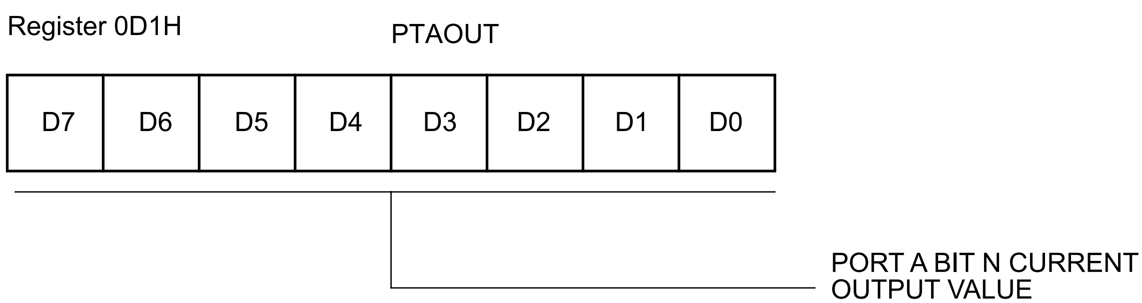


Figure 29. Port A Output Value Register

PORT B

Port B Description

Port B is a 5-bit (bidirectional), CMOS-compatible I/O port. These five I/O lines can be configured under software control to be an input or output, independently. Input buffers are Schmitt-triggered. See Figure 33 through Figure 36 for diagrams of all five Port B pins.

In addition to standard input/output capability on all five pins of Port B, each pin provides special functionality as shown in the following table:

Special functionality is invoked via the Port B Special Function Register. See Figure 32 for the arrangement and control conventions of this register.

Table 8. Port B Special Functions

Port Pin	Input Special Function	Output Special Function
PB0	Stop Mode Recovery Input	None
PB1	None	Timer0 Output
PB2	IRQ3	None
PB3	Comparator Reference Input	None
PB4	Comparator Signal Input/IRQ1/IRQ4	None

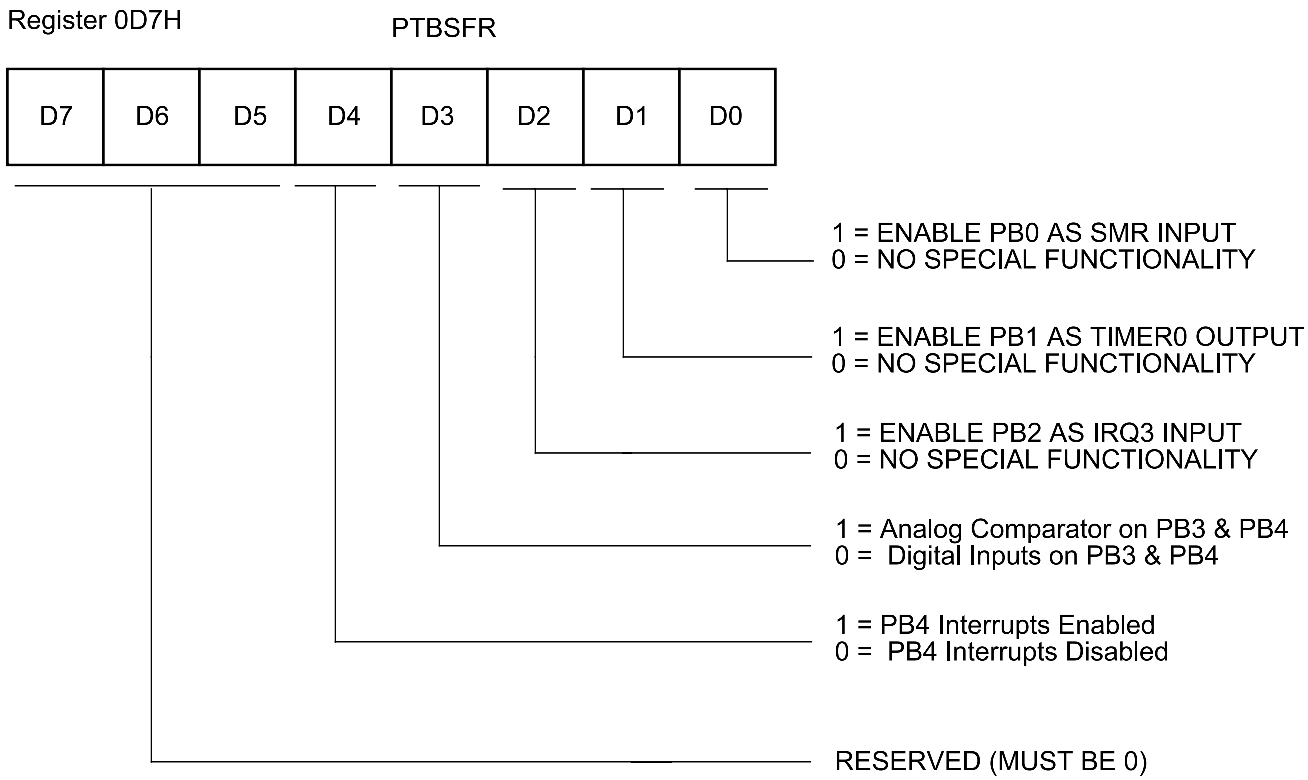


Figure 32. Port B Special Function Register

PORT B CONTROL REGISTERS (Continued)

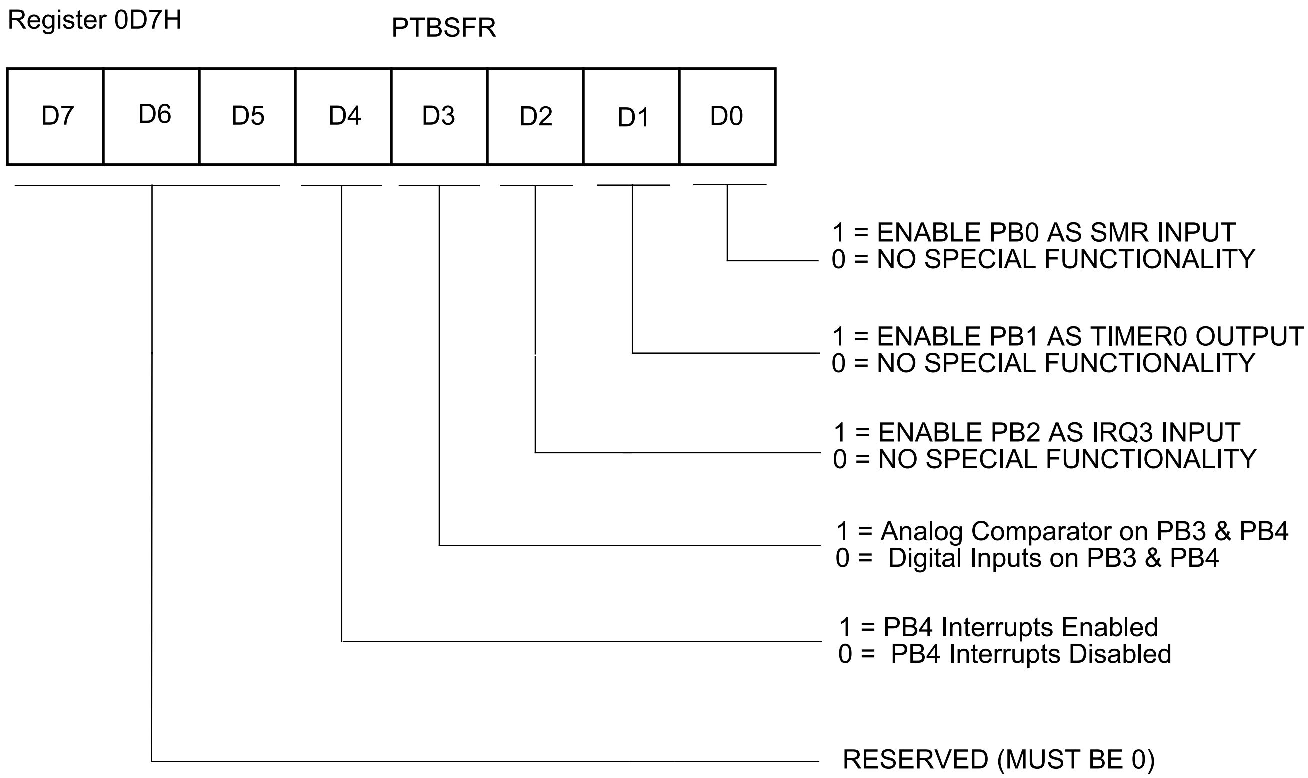


Figure 40. Port B Special Function Register

INPUT PROTECTION

All I/O pins on the Z8E001 have diode input protection. There is a diode from the I/O pad to V_{CC} and V_{SS} (Figure 41).

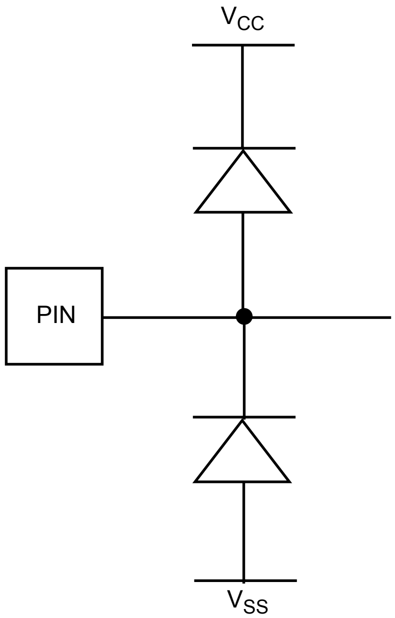


Figure 41. I/O Pin Diode Input Protection

However, on the Z8E001, the $\overline{\text{RESET}}$ pin has only the input protection diode from pad to V_{SS} (Figure 42).

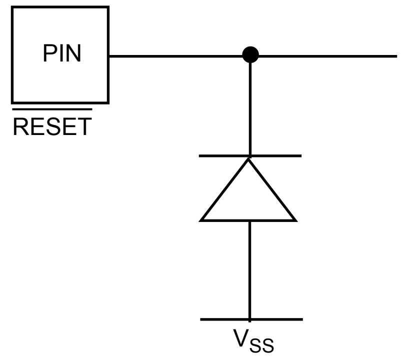
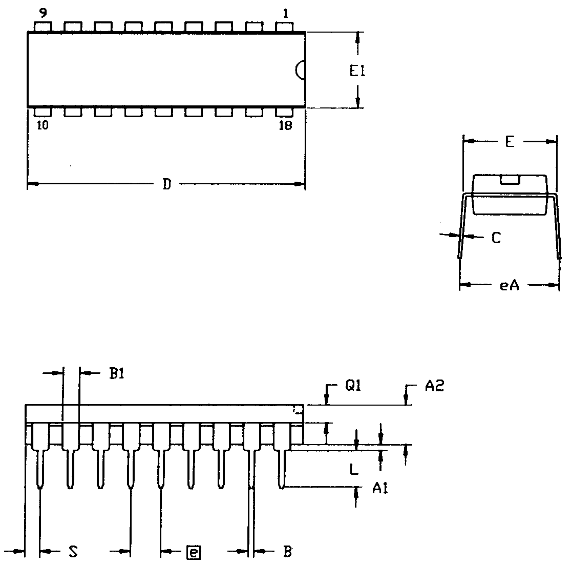


Figure 42. $\overline{\text{RESET}}$ Pin Input Protection

The high-side input protection diode was removed on this pin to allow the application of high voltage during the OTP programming mode.

For better noise immunity in applications that are exposed to system EMI, a clamping diode to V_{CC} from this pin can be required to prevent entering the OTP programming mode or to prevent high voltage from damaging this pin.

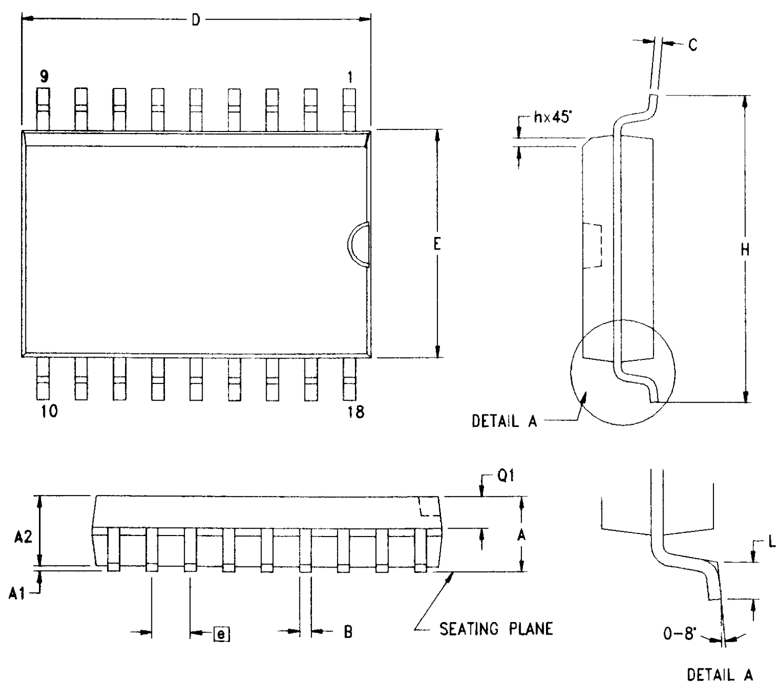
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

Figure 43. 18-Pin DIP Package Diagram

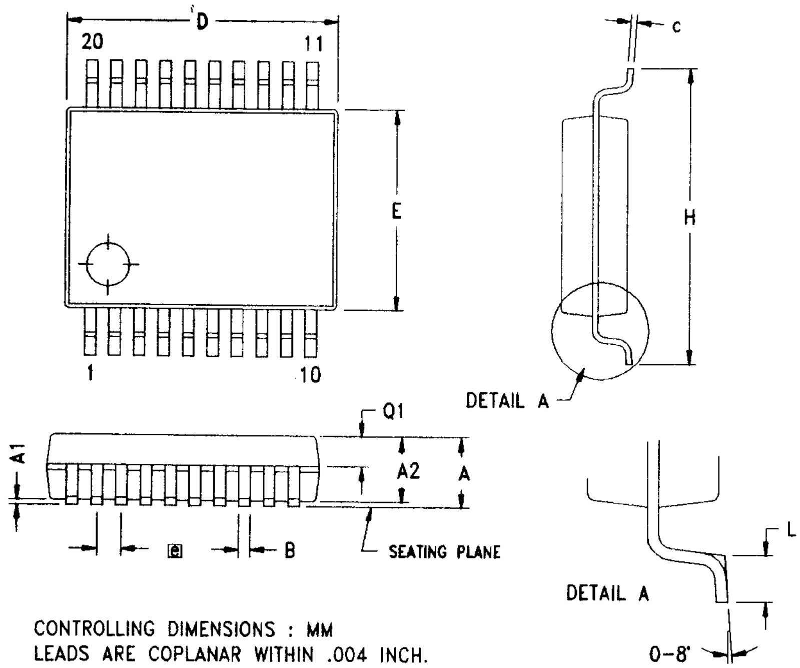


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
e	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 44. 18-Pin SOIC Package Diagram

PACKAGE INFORMATION (Continued)



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.85	1.98	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.83	0.066	0.068	0.072
B	0.25	0.30	0.38	0.010	0.012	0.015
C	0.13	0.15	0.22	0.005	0.006	0.009
D	7.07	7.20	7.33	0.278	0.283	0.289
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 TYP			0.0256 TYP		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.56	0.75	0.94	0.022	0.030	0.037
Q1	0.74	0.78	0.82	0.029	0.031	0.032

Figure 45. 20-Pin SSOP Package Diagram

ORDERING INFORMATION

Standard Temperature	
18-Pin DIP	Z8E00110SSC
18-Pin SOIC	Z8E00110HSC
20-Pin SSOP	Z8E00110PSC
Extended Temperature	
18-Pin DIP	Z8E00110PEC
18-Pin SOIC	Z8E00110SEC
20-Pin SSOP	Z8E00110HEC

For fast results, contact your local ZiLOG sales office for assistance in ordering the part(s) required.

Codes	
Preferred Package	P = Plastic DIP
Longer Lead Time	S = SOIC
	H = SSOP
Preferred Temperature	S = 0°C to +70°C
	E = –40°C to +105°C
Speed	10 = 10 MHz
Environmental	C = Plastic Standard

Example:

Z 8E001 10 P S C is a Z86E001, 10 MHz, DIP, 0° to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 10 — Speed
- 8E001 — Product Number
- Z — ZiLOG Prefix

Pre-Characterization Product:

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or non-conformance with some aspects of the document may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

Development Projects:

Customer is cautioned that while reasonable efforts will be employed to meet performance objectives and milestone dates, development is subject to unanticipated problems and delays. No production release is authorized or committed until the Customer and ZiLOG have agreed upon a Product Specification for this project.

Low Margin:

Customer is advised that this product does not meet ZiLOG's internal guardbanded test policies for the specification requested and is supplied on an exception basis. Customer is cautioned that delivery may be uncertain and that, in addition to all other limitations on ZiLOG liability stated on the front and back of the acknowledgement, ZiLOG makes no claim as to quality and reliability under the document. The product remains subject to standard warranty for replacement due to defects in materials and workmanship.

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