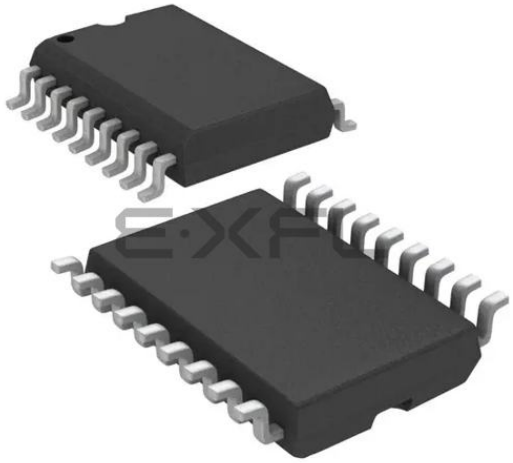


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	PWM, WDT
Number of I/O	13
Program Memory Size	1KB (1K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8e00110sec00tr

GENERAL DESCRIPTION (Continued)

ing real-time tasks such as counting/timing and I/O data communications.

Note: All signals with an overline, " ", are active Low. For example, B/W (WORD is active Low, only); B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

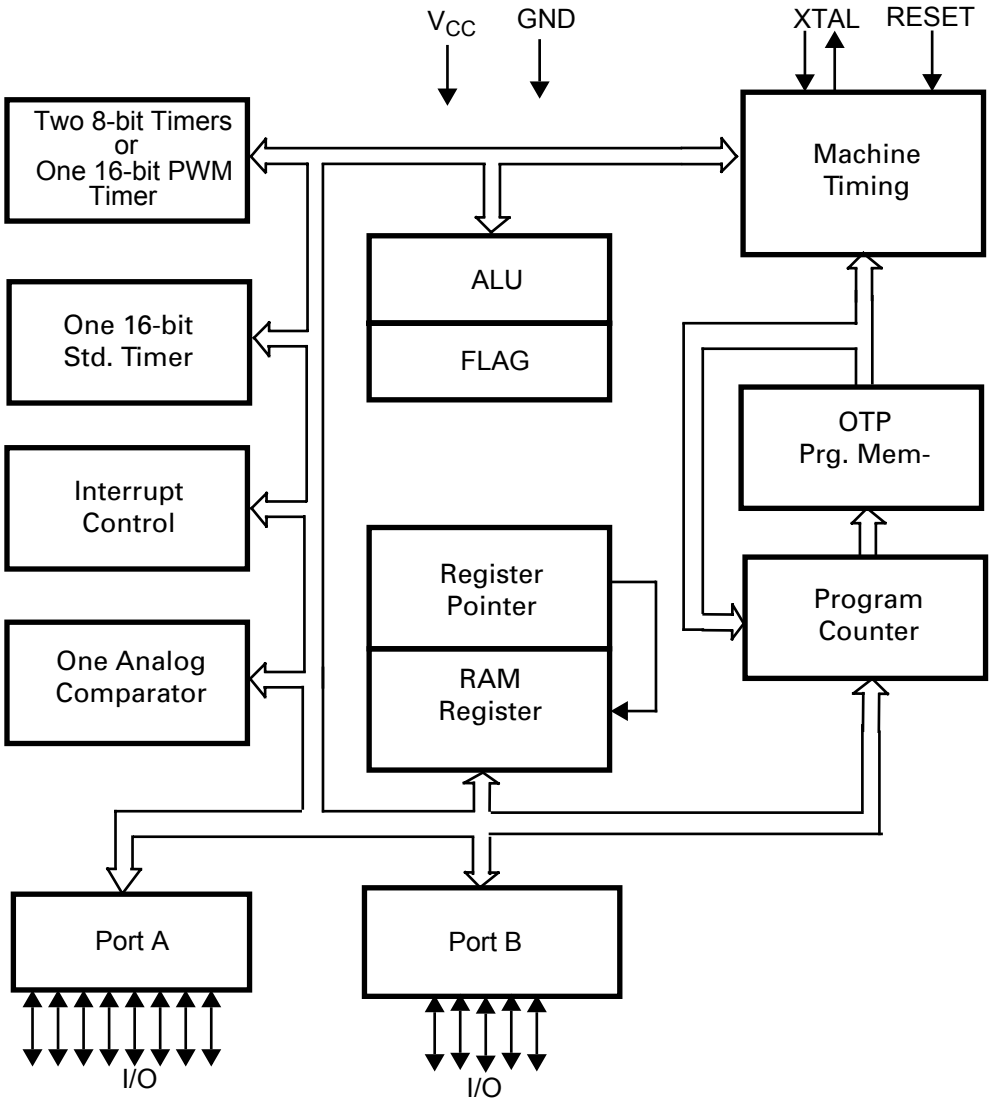


Figure 1. Functional Block Diagram

PIN DESCRIPTION (Continued)

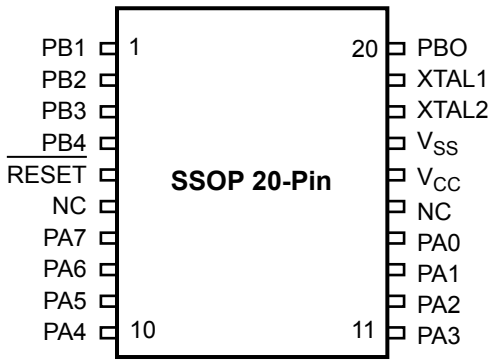


Figure 5. 20-Pin SSOP Pin Identification

Standard Mode

Pin #	Symbol	Function	Direction
1–4	PB1–PB4	Port B, Pins 1,2,3,4	Input/Output
5	RESET	Reset	Input
6	NC	No Connection	
7–10	PA7–PA4	Port A, Pins 7,6,5,4	Input/Output
11–14	PA3–PA0	Port A, Pins 3,2,1,0	Input/Output
15	NC	No Connection	
16	V_{CC}	Power Supply	
17	V_{SS}	Ground	
18	XTAL2	Crystal Osc. Clock	Output
19	XTAL1	Crystal Osc. Clock	Input
20	PB0	Port B, Pin 0	Input/Output

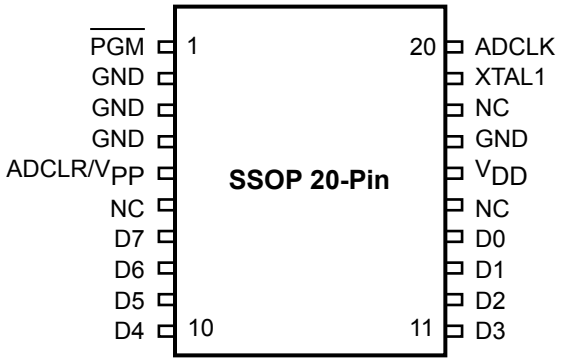


Figure 6. 20-Pin SSOP Pin Identification/EPROM Programming Mode

EPROM Programming Mode

Pin #	Symbol	Function	Direction
1	$\overline{PGM}$	Prog Mode	Input
2–4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clk./Prog Volt.	Input
6	NC	No Connection	
7–10	D7–D4	Data 7,6,5,4	Input/Output
11–14	D3–D0	Data 3,2,1,0	Input/Output
15	NC	No Connection	
16	V_{DD}	Power Supply	
17	GND	Ground	
18	NC	No Connection	
19	XTAL1	1MHz Clock	Input
20	ADCLK	Address Clock	Input

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units	Note
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on $\overline{\text{RESET}}$ Pin with Respect to V_{SS}	–0.6	V_{DD}+1	V	2
Total Power Dissipation		880	mW	
Maximum Allowable Current out of V_{SS}		80	mA	
Maximum Allowable Current into V_{DD}		80	mA	
Maximum Allowable Current into an Input Pin	–600	+600	mA	3
Maximum Allowable Current into an Open-Drain Pin	–600	+600	mA	4
Maximum Allowable Output Current Sunk by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sunk by Port A		40	mA	
Maximum Allowable Output Current Sourced by Port A		40	mA	
Maximum Allowable Output Current Sunk by Port B		40	mA	
Maximum Allowable Output Current Sourced by Port B		40	mA	

Notes:
1. Applies to all pins except the $\overline{\text{RESET}}$ pin and where otherwise noted.
2. There is no input protection diode from pin to V_{DD}.
3. Excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings can cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period can affect device reliability. Total power dissipation should not exceed 880 mW for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [I_{DD} - (\text{sum of } I_{OH})] + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{0L} \times I_{0L})$$

Table 1. DC Electrical Characteristics (Continued)

			pF T_A = 0°C to +70°C Standard Temperatures					
Sym	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Typical[2] @ 25°C**	**Units**	**Conditions**	**Notes**
I_{CC}	Supply Current	3.5V		2.5	2.0	mA	@ 10 MHz	4,5
		5.5V		6.0	3.5	mA	@ 10 MHz	4,5
I_{CC1}	Standby Current	3.5V		2.0	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 10 MHz	4,5
		5.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 10 MHz	4,5
I_{CC2}	Standby Current	3.5V		500	150	nA	STOP Mode V_{IN} = 0V, V_{CC}	6

Notes:
1. The V_{CC} voltage specification of 3.5V guarantees 3.5V and the V_{CC} voltage specification of 5.5 V guarantees 5.0 V ±0.5 V.
2. Typical values are measured at V_{CC} = 3.3V and V_{CC} = 5.0V; V_{SS} = 0V = GND.
3. For analog comparator input when analog comparator is enabled.
4. All outputs unloaded and all inputs are at V_{CC} or V_{SS} level.
5. CL1 = CL2 = 22 pF.
6. Same as note 4 except inputs at V_{CC}.

Z8PLUS CORE

The Z8E001 is based on the ZiLOG Z8Plus Core Architecture. This core is capable of addressing up to 64KBytes of program memory and 4KBytes of RAM. Register RAM is accessed as either 8 or 16 bit registers using a combination of 4, 8, and 12 bit addressing modes. The architecture supports up to 15 vectored interrupts from external and internal sources. The processor decodes 44 CISC instructions using six addressing modes. See the Z8Plus User's Manual for more information.

RESET

This section describes the Z8E001 reset conditions, reset timing, and register initialization procedures. Reset is generated by the Reset Pin, Watch-Dog Timer (WDT), and Stop-Mode Recovery (SMR).

A system reset overrides all other operating conditions and puts the Z8E001 into a known state. To initialize the chip's internal logic, the RESET input must be held Low for at least 30 XTAL clock cycles. The control registers and ports are reset to their default conditions after a reset from the RESET pin. The control registers and ports are not reset to their default conditions after wakeup from Stop Mode or WDT timeout.

During $\overline{\text{RESET}}$, the program counter is loaded with 0020H. I/O ports and control registers are configured to their default reset state. Resetting the Z8E001 does not affect the contents of the general-purpose registers.

RESET PIN OPERATION

The Z8E001 hardware $\overline{\text{RESET}}$ pin initializes the control and peripheral registers, as shown in Table 4. Specific reset values are shown by 1 or 0, while bits whose states are unchanged or unknown from Power-Up are indicated by the letter U.

$\overline{\text{RESET}}$ must be held Low until the oscillator stabilizes, for an additional 30 XTAL clock cycles, in order to be sure that the internal reset is complete. The RESET pin has a Schmitt-Trigger input with a trip point. There is no High side protection diode. The user should place an external diode from $\overline{\text{RESET}}$ to V_{CC}. A pull-up resistor on the $\overline{\text{RESET}}$ pin is approximately 500 KΩ, typical.

Program execution starts 10 XTAL clock cycles after $\overline{\text{RESET}}$ has returned High. The initial instruction fetch is from location 0020H. Figure 9 indicates reset timing.

After a reset, the first routine executed must be one that initializes the TCTLHI control register to the required system configuration, followed by initialization of the remaining control registers.

Table 4. Control and Peripheral Registers

		Bits								
Register (HEX)	**Register Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**
FF	Stack Pointer	0	0	U	U	U	U	U	U	Stack pointer is not affected by RESET
FE	Reserved									
FD	Register Pointer	U	U	U	U	0	0	0	0	Register pointer is not affected by RESET
FC	Flags	U	U	U	U	U	U	*	*	Only WDT & SMR flags are affected by RESET
FB	Interrupt Mask	0	0	0	0	0	0	0	0	All interrupts masked by $\overline{\text{RESET}}$
FA	Interrupt Request	0	0	0	0	0	0	0	0	All interrupt requests cleared by RESET
F9–F0	Reserved									
EF–E0	Virtual Copy									Virtual Copy of the Current Working Register Set
DF–D8	Reserved									

Note: The WDT can only be disabled via software if the first instruction out of RESET performs this function. Logic within the Z8E001 detects that it is in the process of executing the first instruction after the part leaves RESET. During the execution of this instruction, the upper five bits of the TCTLHI register can be written. After this first instruction, hardware does not allow the upper five bits of this register to be written.

The TCTLHI bits for control of the WDT are described below:

WDT Time Select (D6, D5, D4). Bits 6, 5, and 4 determine the time-out period. Table 6 indicates the range of timeout values that can be obtained. The default values of D6, D5, and D4 are all 1, thus setting the WDT to its maximum timeout period when coming out of RESET.

WDT During HALT (D7). This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. A 0 prevents the WDT from resetting the part while halted.Coming out of reset, the WDT is enabled during HALT Mode.

STOP MODE (D3). Coming out of RESET, the Z8E001 STOP Mode is disabled. If an application requires use of STOP Mode, bit D3 must be cleared immediately upon leaving RESET. If bit D3 is set, the STOP instruction executes as a NOP. If bit D3 is cleared, the STOP instruction enters Stop Mode. Whenever the Z8E001 wakes up after having been in STOP Mode, the STOP Mode is again disabled.

Bits 2, 1 and 0. These bits are reserved and must be 0.

Table 6. WDT Time-Out

D6	D5	D4	Crystal Clocks* to Timeout	Time-Out Using a 10 MHZ Crystal
0	0	0	Disabled	Disabled
0	0	1	65,536 TpC	6.55 ms
0	1	0	131,072 TpC	13.11 ms
0	1	1	262,144 TpC	26.21 ms
1	0	0	524,288 TpC	52.43 ms
1	0	1	1,048,576 TpC	104.86 ms
1	1	0	2,097,152 TpC	209.72 ms
1	1	1	4,194,304 TpC	419.43 ms

Note:
*TpC=XTAL clock cycle. The default on reset is D6=D5=D4=1.

POWER-DOWN MODES

In addition to the standard RUN mode, the Z8E001 MCU supports two Power-Down modes to minimize device current consumption. The two modes supported are HALT and STOP.

HALT MODE OPERATION

The HALT Mode suspends instruction execution and turns off the internal CPU clock. The on-chip oscillator circuit remains active so the internal clock continues to run and is applied to the timers and interrupt logic.

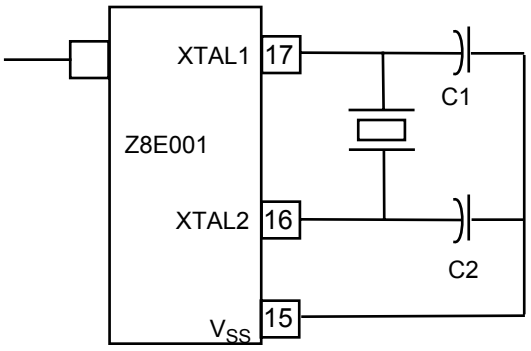
To enter the HALT Mode, the Z8E001 only requires a HALT instruction. It is NOT necessary to execute a NOP instruction immediately before the HALT instruction.

```
7F      HALT            ; enter HALT Mode
```

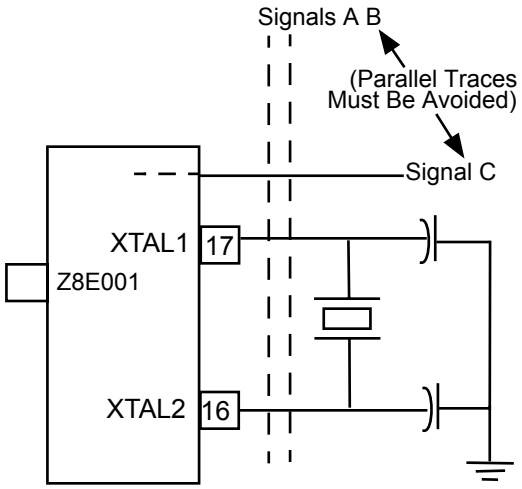
The HALT Mode can be exited by servicing an interrupt (either externally or internally) generated. Upon completion of the interrupt service routine, the user program continues from the instruction after the HALT instruction.

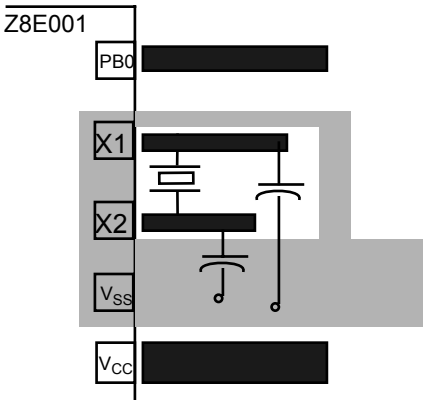
The HALT Mode can also be exited via a RESET activation or a Watch-Dog Timer (WDT) timeout. In these cases, program execution restarts at the reset restart address 0020H.

- V_{CC} power lines should be separated from the clock oscillator input circuitry.
- Resistivity between XTAL1 or XTAL2 (and the other pins) should be greater than 10 MΩ.



Clock Generator Circuit





Board Design Example

(Top View)

Figure 15. Circuit Board Design Rules

Crystals and Resonators

Crystals and ceramic resonators (Figure 16) should have the following characteristics to ensure proper oscillation:

Crystal Cut	AT (crystal only)
Mode	Parallel, Fundamental Mode
Crystal Capacitance	<7pF
Load Capacitance	10pF < CL < 220 pF,
	15 typical
Resistance	100 ohms max

Depending on the operation frequency, the oscillator can require additional capacitors, C1 and C2, as shown in Figure 16 and Figure 17. The capacitance values are dependent on the manufacturer's crystal specifications.

TIMERS (Continued)

at any time, and will have no effect on the functionality of the timer.

If a timer pair is defined to operate as a single 16-bit entity, the entire 16-bit value must reach 0 before an interrupt is generated. In this case, a single interrupt is generated, and the interrupt corresponds to the even 8-bit timer.

Example: Timers T2 and T3 are cascaded to form a single 16-bit timer, so the interrupt for the combined timer is defined to be that of timer T2 rather than T3. When a timer pair is specified to act as a single 16-bit timer, the even timer registers in the pair (timer T0 or T2) is defined to hold the timer's least significant byte. In contrast, the odd timer in the pair holds the timer's most significant byte.

In parallel with the posting of the interrupt request, the interrupting timer's count value is initialized by copying the contents of the auto-initialization value register to the count value register. It should be noted that any time that a timer pair is defined to act as a single 16-bit timer, that the autoreload function is performed automatically. All 16-bit timers continue counting while their interrupt requests are active, and each operates in a free-running manner.

If interrupts are disabled for a long period of time, it is possible for the timer to decrement to 0 again before its initial interrupt has been responded to. This condition is termed a degenerate case, and hardware is not required to detect it.

When the timer control register is written, all timers that are enabled by the write begins counting using the value that is held in the count register. In this case, an auto-initialization is not performed. All timers can receive an internal clock source only. Each timer that is enabled is updated every 8th XTAL clock cycle.

If T0 and T1 are defined to work independently, then each works as an 8-bit timer with a single auto-initialization register (T0ARLO for T0, and T1ARLO for T1). Each timer asserts its predefined interrupt when it times out, optionally performing the auto-initialization function. If T0 and T1 are cascaded to form a single 16-bit timer, then the single 16-bit timer is capable of performing as a Pulse-Width Modulator (PWM). This timer is referred to as T01 to distinguish it as having special functionality that is not available when T0 and T1 act independently.

When T01 is enabled, it can use a pair of 16-bit auto-initialization registers. In this mode, one 16-bit auto-initialization value is composed of the concatenation of T1ARLO and T0ARLO. The second auto-initialization value is composed of the concatenation of T1ARHI and T0ARHI. When T01 times out, it alternately initializes its count value using the LO auto-init pair, followed by the HI auto-init pair. This functionality corresponds to a PWM, where the T1 interrupt defines the end of the HI section of the waveform, and the T0 interrupt marks the end of the LO portion of the PWM waveform.

To use the cascaded timers as a PWM, one must initialize the T0 and T1 count registers to work in conjunction with the port pin. The user should initialize the T0 and T1 count registers to the PWM_HI auto-init value to obtain the required PWM behavior. The PWM is arbitrarily defined to use the LO autoreload registers first, implying that it had just timed out after beginning in the HI portion of the PWM waveform. As such, the PWM is defined to assert the T1 interrupt after the first timeout interval.

After the auto-initialization has been completed, decrementing occurs for the number of counts defined by the PWM_LO registers. When decrementing again reaches 0, the T0 interrupt is asserted; and auto-init using the PWM_HI registers occurs. Decrementing occurs for the number of counts defined by the PWM_HI registers until reaching 0. From there, the T1 interrupt is asserted, and the cycle begins again.

The internal timers can be used to trigger external events by toggling the PB1 output when generating an interrupt. This functionality can only be achieved in conjunction with the port unit defining the appropriate pin as an output signal with the timer output special function enabled. In this mode, the appropriate port output is toggled when the timer count reaches 0, and continues toggling each time that the timer times out.

T_{OUT} Mode

The PortB special function register PTBSFR (0D7H) (Figure 23) is used in conjunction with the Port B directional control register PTBDIR (0D6) (Figure 24) to configure PB1 for T_{OUT} operation for timer0. In order for T_{OUT} to function, PB1 must be defined as an output line by setting PTBDIR bit 1 to 1. Configured in this way, PB1 has the capability of being a clock output for timer0, toggling the PB1 output pin on each timer0 timeout.

At end-of-count, the interrupt request line IRQ0, clocks a toggle flip-flop. The output of this flip-flop drives the T_{OUT} line, PB1. In all cases, when timer0 reaches its end-of-count, T_{OUT} toggles to its opposite state (Figure 25). If, for example, timer0 is in Continuous Counting Mode, T_{OUT} has a 50 percent duty cycle output. This duty cycle can easily be controlled by varying the initial values after each end-of-count.

RESET CONDITIONS

After a hardware $\overline{\text{RESET}}$, the timers are disabled. See Table 4 for timer control, value, and auto-initialization register status after RESET.

I/O PORTS

The Z8E001 has 13 lines dedicated to input and output. These lines are grouped into two ports known as Port A and Port B. Port A is an 8-bit port, bit programmable as either inputs or outputs. Port B can be programmed to provide standard input/output or the following special functions: timer0 output, comparator input, SMR input, and external interrupt inputs.

All ports have push-pull CMOS outputs. In addition, the outputs of Port A on a bit-wise basis can be configured for open-drain operation.The ports operate on a bit-wise basis. As such, the register values for/at a given bit position only affect the bit in question.

Each port is defined by a set of four control registers. See Figure 27.

Directional Control and Special Function Registers

Each port on the Z8E001 has a dedicated Directional Control Register that determines (on a bit-wise basis) whether a given port bit operates as either an input or an output.

Each port on the Z8E001 has a Special Function Register that, in conjunction with the Directional Control Register, implements (on a bit-wise basis), any special functionality that can be defined for each particular port bit.

Table 7. Z8E001 I/O Ports Registers

Register	Address	Identifier
Port B Special Function	OD7H	PTBSFR
Port B Directional Control	0D6H	PTBDIR
Port B Output Value	0D5H	PTBOUT
Port B Input Value	0D4H	PTBIN
Port A Special Function	0D3H	PTASFR
Port A Directional Control	0D2H	PTADIR
Port A Output Value	0D1H	PTAOUT
Port A Input Value	0D0H	PTAIN

Input and Output Value Registers

Each port has an Output Value Register and a pF Input Value Register. For port bits configured as an input by means of the Directional Control Register, the Input Value Register for that bit position contains the current synchronized input value.

For port bits configured as an output by means of the Directional Control Register, the value held in the corresponding bit of the Output Value Register is driven directly onto the output pin. The opposite register bit for a given pin (the output register bit for an input pin and the input register bit for an output pin) holds their previous value. These bits are not changed and don't have any effect on the hardware.

READ/WRITE OPERATIONS

The control for each port is done on a bit-wise basis. All bits are capable of operating as inputs or outputs, depending upon the setting of the port's Directional Control Register. If configured as an input, each bit is provided a Schmitt-trigger. The output of the Schmitt-trigger is latched twice to perform a synchronization function, and the output of the synchronizer is fed to the port input register, which can be read by software.

A write to a port input register has the effect of updating the contents of the input register, but subsequent reads do not necessarily return the same value that was written. If the bit in question is defined as an input, the input register for that bit position contains the current synchronized input value. Thus, writes to that bit position is overwritten on the next clock cycle with the newly sampled input data. However, if the particular port bit is programmed as an output, the input register for that bit retains the software-updated value. The port bits that are programmed as outputs do not sample the value being driven out.

Any bit in either port can be defined as an output by setting the appropriate bit in the directional control register. If such is the case, the value held in the appropriate bit of the port output register is driven directly onto the output pin.

Note: The preceding result does not necessarily reflect the actual output value. If an external error is holding an output pin either High or Low against the output driver, the software read returns the *required* value, not the actual state caused by the contention. When a bit is defined as an output, the Schmitt-trigger on the input is disabled to save power.

Updates to the output register takes effect based upon the timing of the internal instruction pipeline, but is referenced to the rising edge of the clock. The output register can be read at any time, and returns the current output value that is held. No restrictions are placed on the timing of reads and/or writes to any of the port registers with respect to the others; however, care should be taken when updating the directional control and special function registers.

When updating a Directional Control Register, the Special Function Register should first be disabled. If this precaution is not taken, spurious events could take place as a result of the change in port I/O status. This precaution is especially important when defining changes in Port B, as the spurious event referred to above could be one or more interrupts. Clearing of the SFR register should be the first step in configuring the port, while setting the SFR register should be the final step in the port configuration process. To ensure deterministic behavior, the SFR register should not be written until the pins are being driven appropriately, and all initialization has been completed.

PORT A

Port A is a general-purpose port. Figure 26 features a block diagram of Port A. Each of its lines can be independently programmed as input or output via the Port A Directional Control Register (PTADIR at 0D2H) as seen in Figure 27. A bit set to a 1 in PTADIR configures the corresponding bit in Port A as an output, while a bit cleared to 0 configures the corresponding bit in Port A as an input.

The input buffers are Schmitt-triggered. Bits programmed as outputs can be individually programmed as either push-pull or open drain by setting the corresponding bit in the Special Function Register (PTASFR, Figure 27).

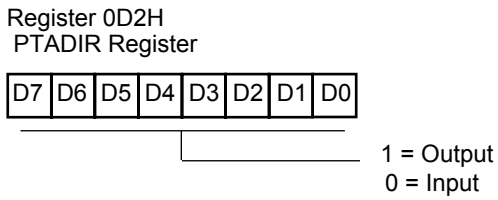


Figure 26. Port A Directional Control Register

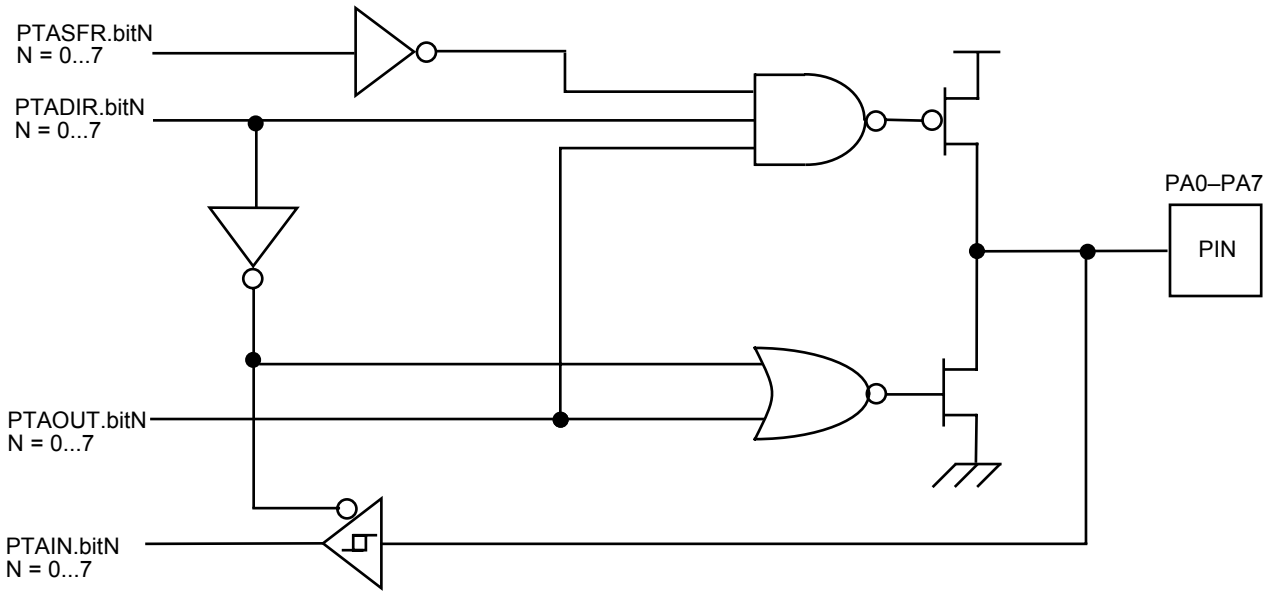


Figure 27. Port A Configuration with Open-Drain Capability and Schmitt-Trigger

PORT B

Port B Description

Port B is a 5-bit (bidirectional), CMOS-compatible I/O port. These five I/O lines can be configured under software control to be an input or output, independently. Input buffers are Schmitt-triggered. See Figure 33 through Figure 36 for diagrams of all five Port B pins.

In addition to standard input/output capability on all five pins of Port B, each pin provides special functionality as shown in the following table:

Special functionality is invoked via the Port B Special Function Register. See Figure 32 for the arrangement and control conventions of this register.

Table 8. Port B Special Functions

Port Pin	Input Special Function	Output Special Function
PB0	Stop Mode Recovery Input	None
PB1	None	Timer0 Output
PB2	IRQ3	None
PB3	Comparator Reference Input	None
PB4	Comparator Signal Input/IRQ1/IRQ4	None

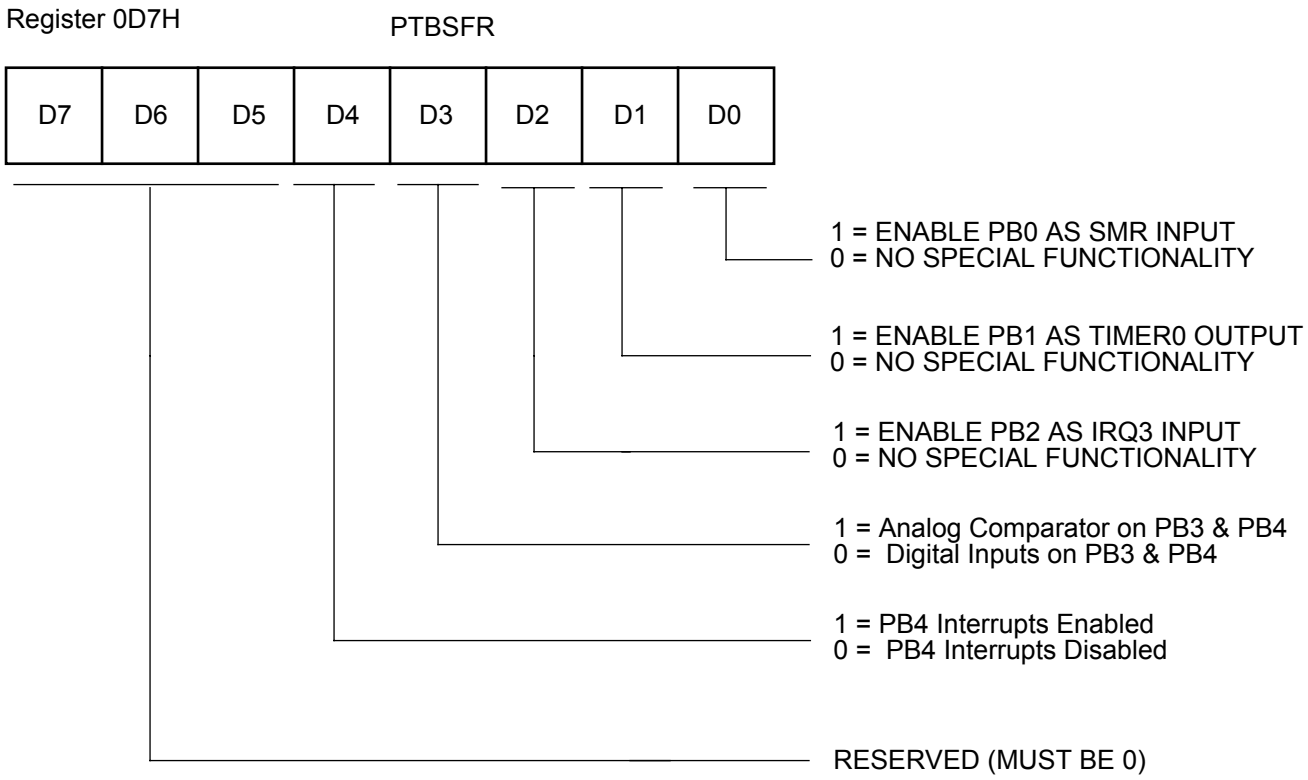


Figure 32. Port B Special Function Register

PORT B—PIN 0 CONFIGURATION

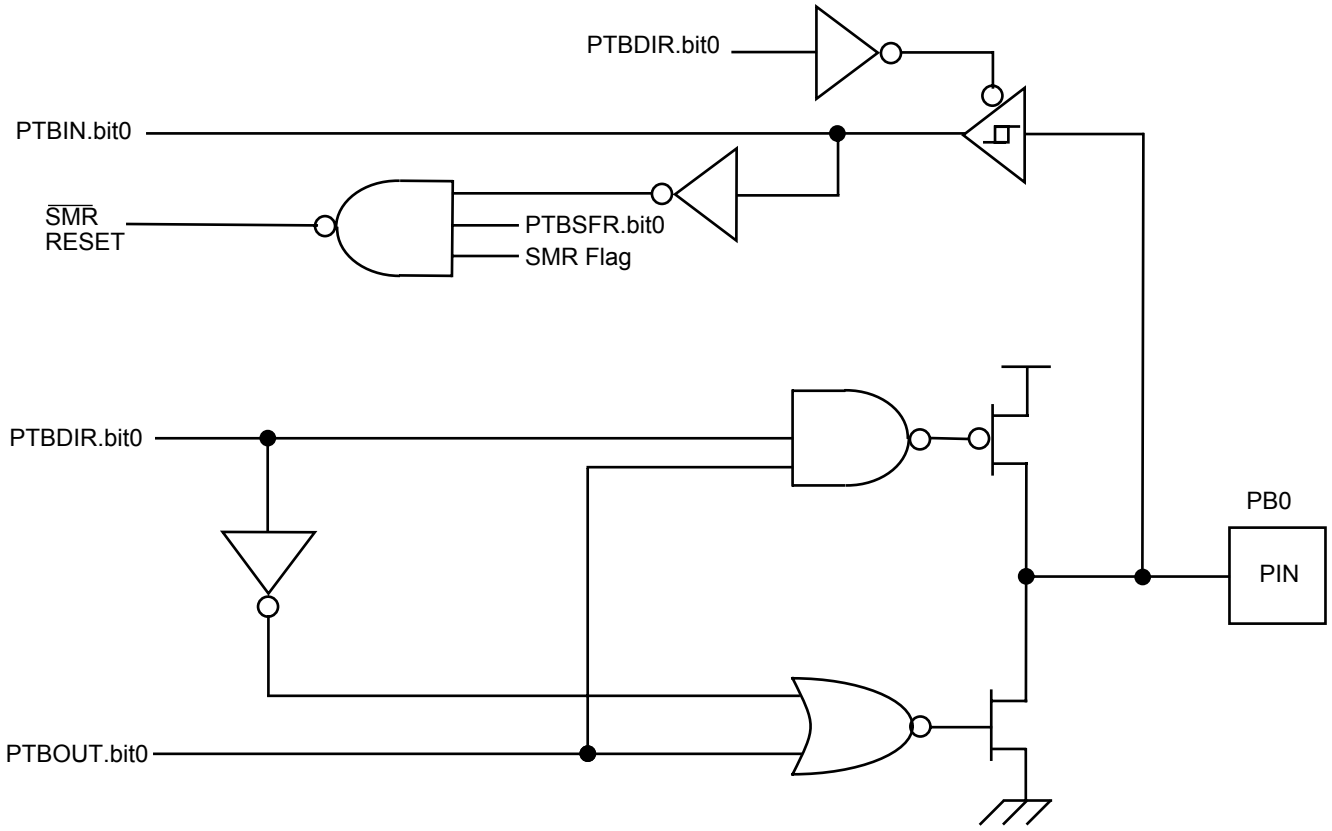


Figure 33. Port B Pin 0 Diagram

PORT B—PIN 2 CONFIGURATION

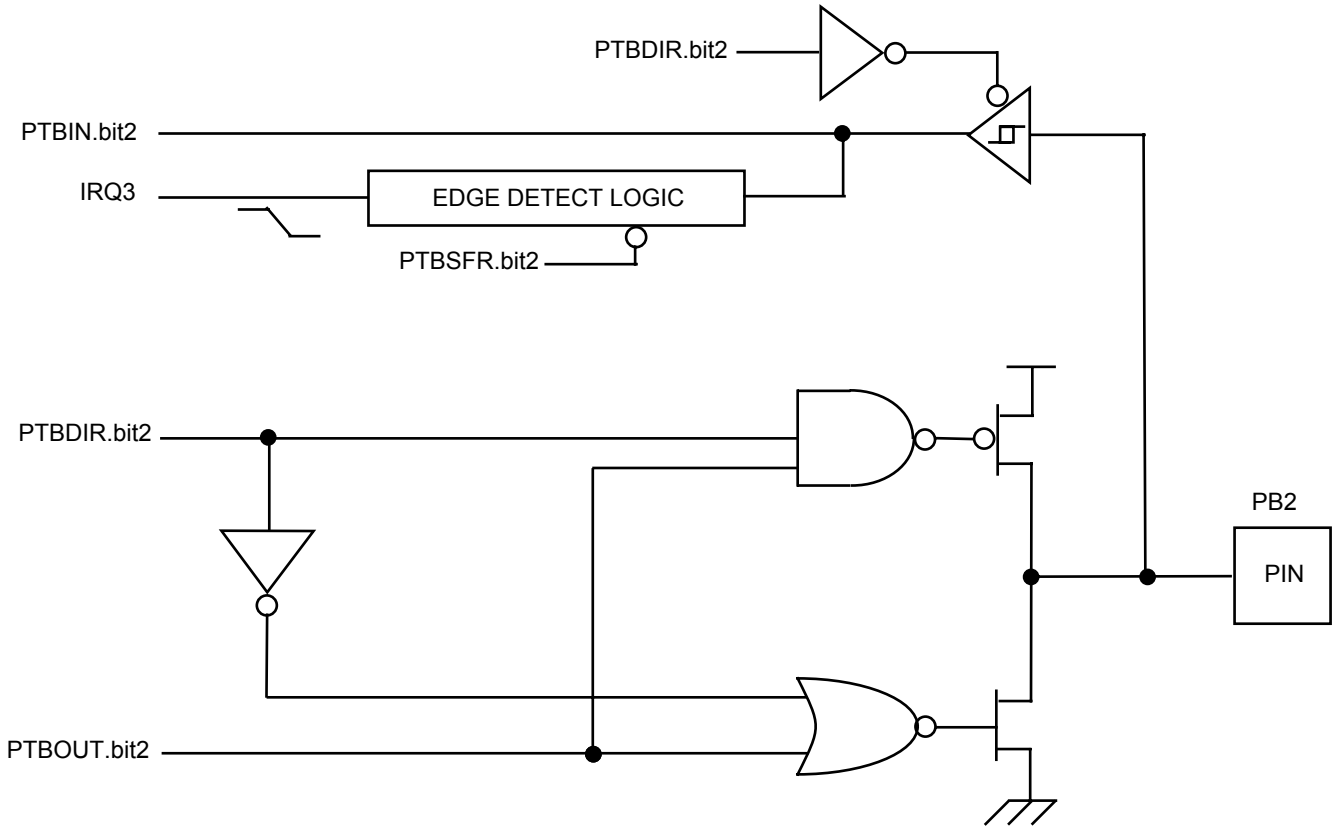


Figure 35. Port B Pin 2 Diagram

PORT B—PINS 3 AND 4 CONFIGURATION

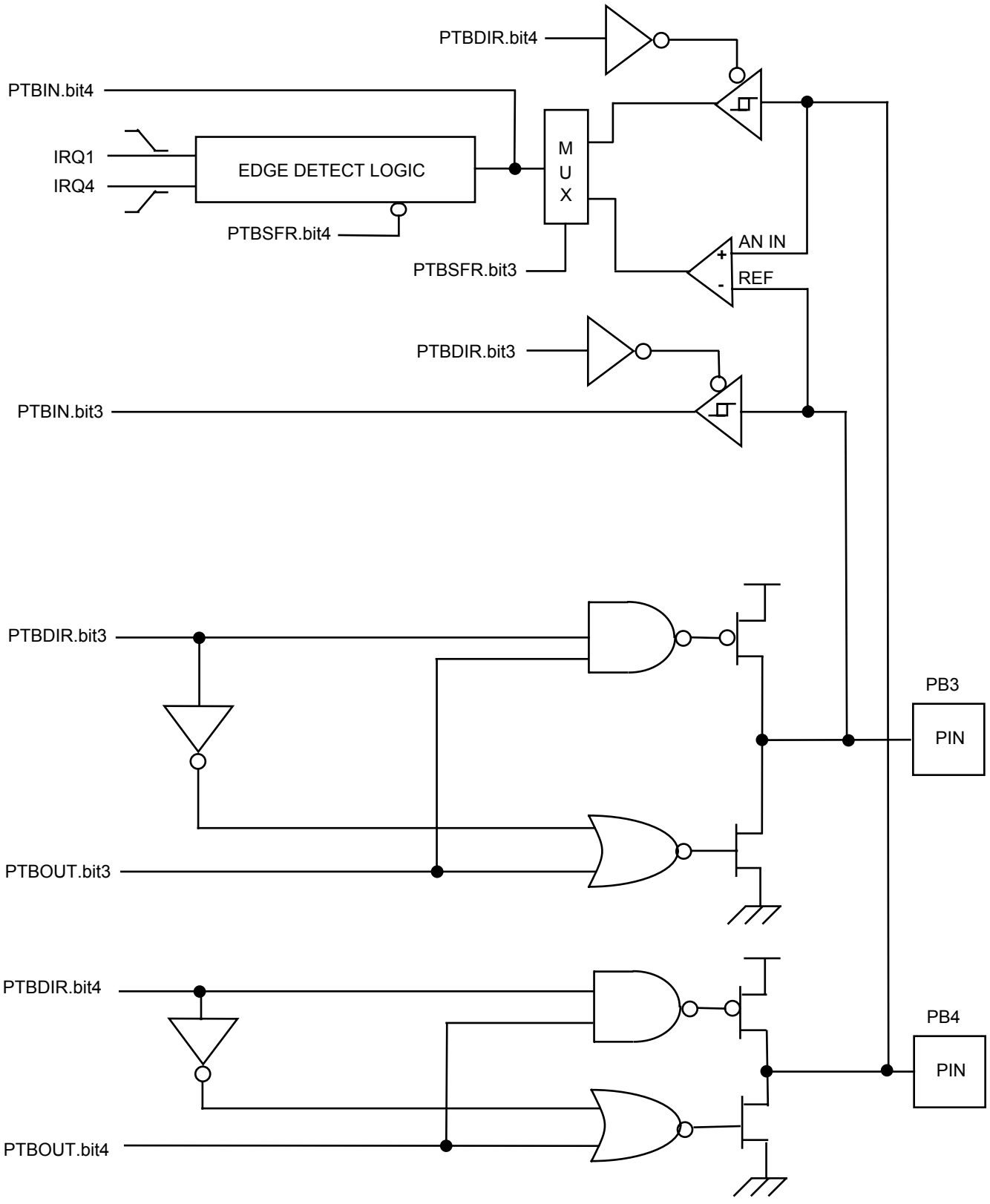


Figure 36. Port B Pins 3 and 4 Diagram

PORT B CONTROL REGISTERS

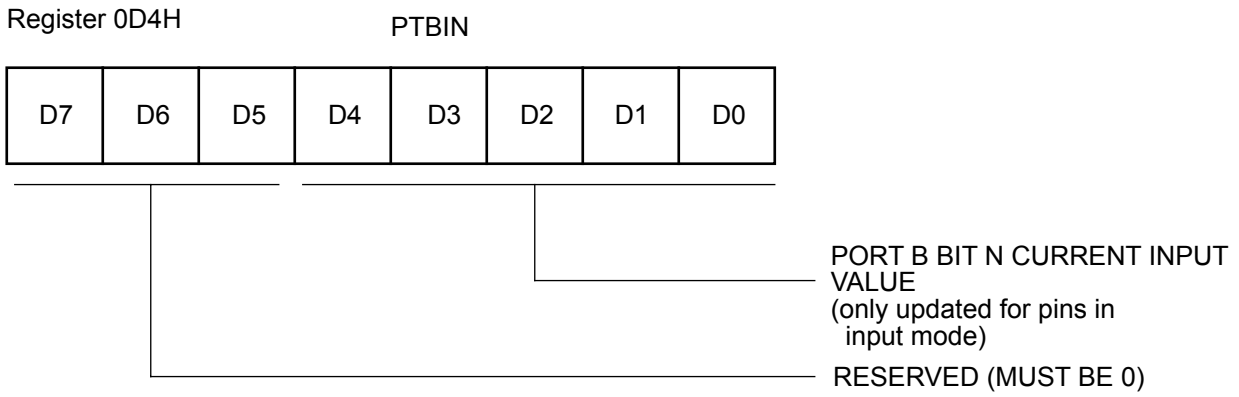


Figure 37. Port B Input Value Register

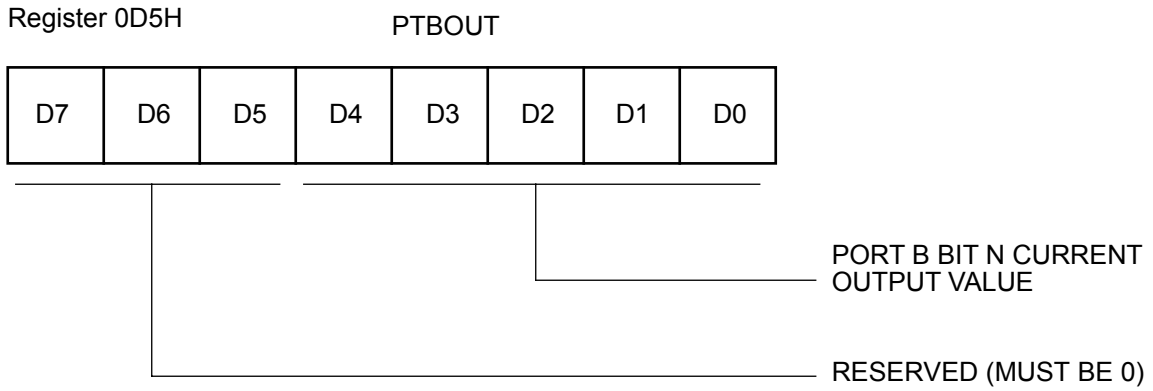


Figure 38. Port B Output Value Register

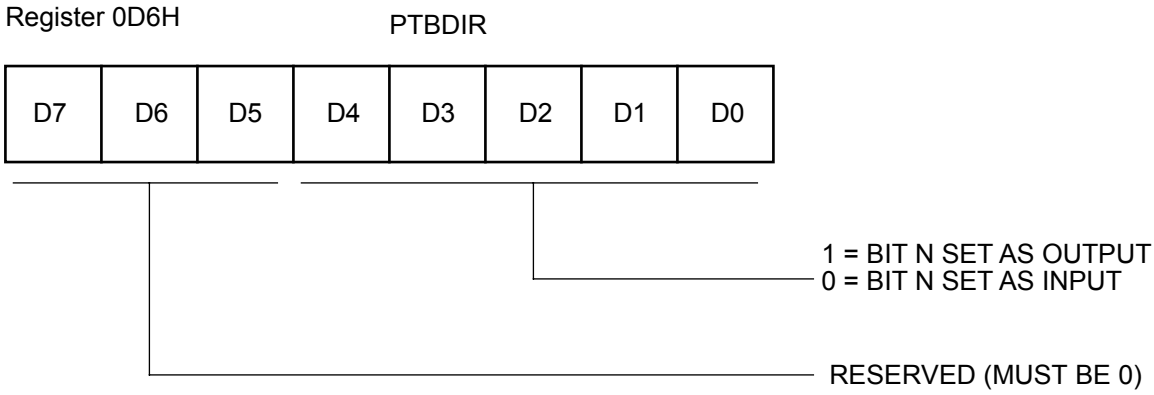


Figure 39. Port B Directional Control Register

PORT B CONTROL REGISTERS (Continued)

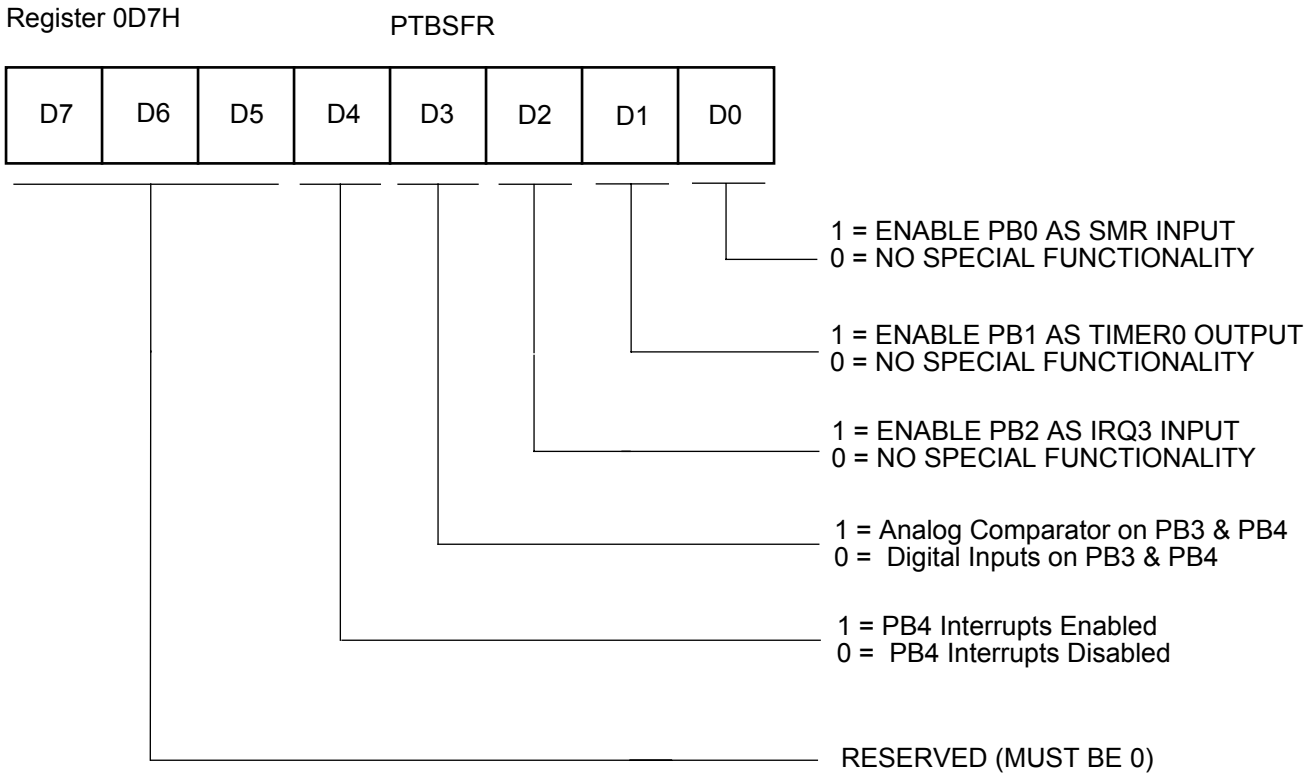


Figure 40. Port B Special Function Register

INPUT PROTECTION

All I/O pins on the Z8E001 have diode input protection. There is a diode from the I/O pad to V_{CC} and V_{SS} (Figure 41).

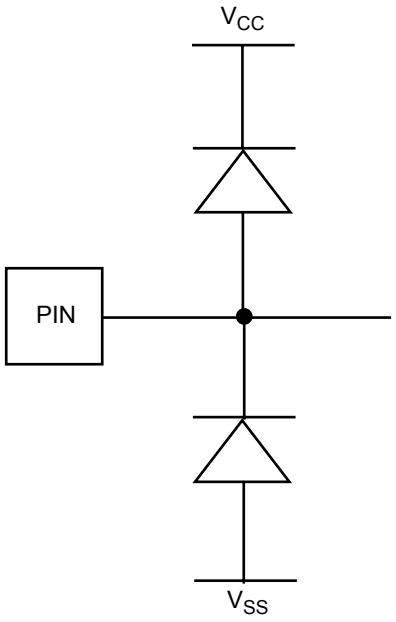


Figure 41. I/O Pin Diode Input Protection

However, on the Z8E001, the $\overline{\text{RESET}}$ pin has only the input protection diode from pad to V_{SS} (Figure 42).

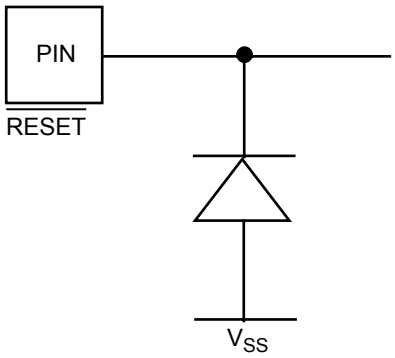


Figure 42. $\overline{\text{RESET}}$ Pin Input Protection

The high-side input protection diode was removed on this pin to allow the application of high voltage during the OTP programming mode.

For better noise immunity in applications that are exposed to system EMI, a clamping diode to V_{CC} from this pin can be required to prevent entering the OTP programming mode or to prevent high voltage from damaging this pin.

ORDERING INFORMATION

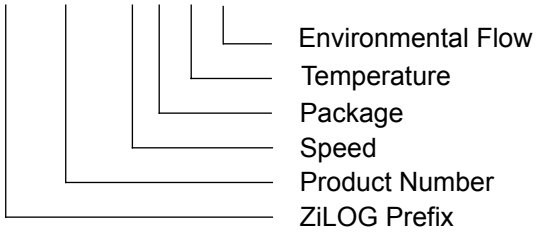
Standard Temperature	
18-Pin DIP	Z8E00110SSC
18-Pin SOIC	Z8E00110HSC
20-Pin SSOP	Z8E00110PSC
Extended Temperature	
18-Pin DIP	Z8E00110PEC
18-Pin SOIC	Z8E00110SEC
20-Pin SSOP	Z8E00110HEC

For fast results, contact your local ZiLOG sales office for assistance in ordering the part(s) required.

Codes	
Preferred Package	P = Plastic DIP
Longer Lead Time	S = SOIC
	H = SSOP
Preferred Temperature	S = 0°C to +70°C
	E = –40°C to +105°C
Speed	10 = 10 MHz
Environmental	C = Plastic Standard

Example:

Z 8E001 10 P S C is a Z86E001, 10 MHz, DIP, 0° to +70°C, Plastic Standard Flow



Pre-Characterization Product:

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or non-conformance with some aspects of the document may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

Development Projects:

Customer is cautioned that while reasonable efforts will be employed to meet performance objectives and milestone dates, development is subject to unanticipated problems and delays. No production release is authorized or committed until the Customer and ZiLOG have agreed upon a Product Specification for this project.

Low Margin:

Customer is advised that this product does not meet ZiLOG's internal guardbanded test policies for the specification requested and is supplied on an exception basis. Customer is cautioned that delivery may be uncertain and that, in addition to all other limitations on ZiLOG liability stated on the front and back of the acknowledgement, ZiLOG makes no claim as to quality and reliability under the document. The product remains subject to standard warranty for replacement due to defects in materials and workmanship.

ZiLOG, Inc.
910 East Hamilton Avenue, Suite 110
Campbell, CA 95008
Telephone (408) 558-8500
FAX 408 558-8300
Internet: http://www.zilog.com