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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	PWM, WDT
Number of I/O	13
Program Memory Size	1KB (1K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8e00110seg

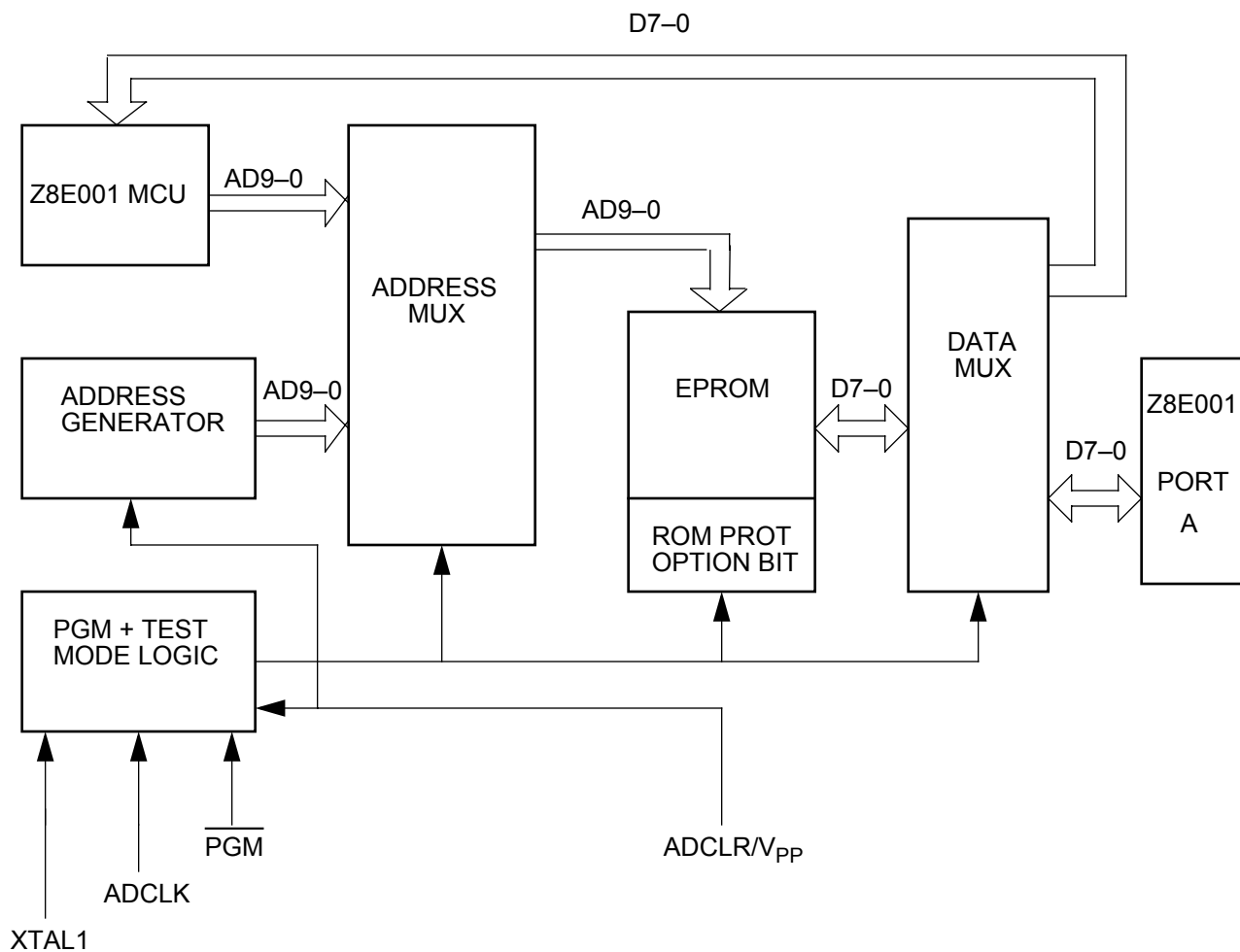


Figure 2. EPROM Programming Mode Block Diagram

PIN DESCRIPTION (Continued)

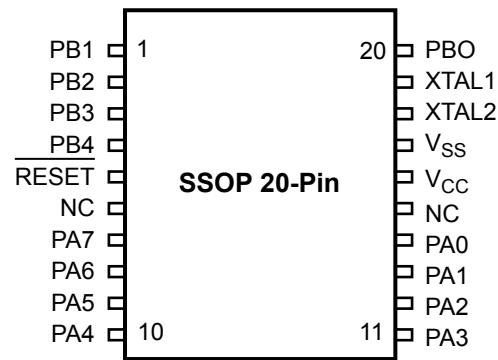


Figure 5. 20-Pin SSOP Pin Identification

Standard Mode			
Pin #	Symbol	Function	Direction
1–4	PB1–PB4	Port B, Pins 1,2,3,4	Input/Output
5	RESET	Reset	Input
6	NC	No Connection	
7–10	PA7–PA4	Port A, Pins 7,6,5,4	Input/Output
11–14	PA3–PA0	Port A, Pins 3,2,1,0	Input/Output
15	NC	No Connection	
16	V _{CC}	Power Supply	
17	V _{SS}	Ground	
18	XTAL2	Crystal Osc. Clock	Output
19	XTAL1	Crystal Osc. Clock	Input
20	PB0	Port B, Pin 0	Input/Output

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units	Note
Ambient Temperature under Bias	−40	+105	C	
Storage Temperature	−65	+150	C	
Voltage on any Pin with Respect to V_{SS}	−0.6	+7	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	−0.3	+7	V	
Voltage on RESET Pin with Respect to V_{SS}	−0.6	$V_{DD}+1$	V	2
Total Power Dissipation		880	mW	
Maximum Allowable Current out of V_{SS}		80	mA	
Maximum Allowable Current into V_{DD}		80	mA	
Maximum Allowable Current into an Input Pin	−600	+600	mA	3
Maximum Allowable Current into an Open-Drain Pin	−600	+600	mA	4
Maximum Allowable Output Current Sunk by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sunk by Port A		40	mA	
Maximum Allowable Output Current Sourced by Port A		40	mA	
Maximum Allowable Output Current Sunk by Port B		40	mA	
Maximum Allowable Output Current Sourced by Port B		40	mA	

Notes:

1. Applies to all pins except the $\overline{\text{RESET}}$ pin and where otherwise noted.
2. There is no input protection diode from pin to V_{DD} .
3. Excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings can cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period can affect device reliability. Total power dissipation should

not exceed 880 mW for the package. Power dissipation is calculated as follows:

$$\begin{aligned} \text{Total Power Dissipation} = & V_{DD} \times [I_{DD} - (\text{sum of } I_{OH})] \\ & + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] \\ & + \text{sum of } (V_{OL} \times I_{OL}) \end{aligned}$$

DC ELECTRICAL CHARACTERISTICS

Table 1. DC Electrical Characteristics

pF T _A = 0°C to +70°C Standard Temperatures								
Sym	Parameter	V _{CC} ¹	Min	Max	Typical ² @ 25°C	Units	Conditions	Notes
V _{CH}	Clock Input High Voltage	3.5V	0.7V _{CC}	V _{CC} +0.3	1.3	V	Driven by External Clock Generator	
		5.5V	0.7V _{CC}	V _{CC} +0.3	2.5	V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	3.5V	V _{SS} -0.3	0.2V _{CC}	0.7	V	Driven by External Clock Generator	
		5.5V	V _{SS} -0.3	0.2V _{CC}	1.5	V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	3.5V	0.7V _{CC}	V _{CC} +0.3	1.3	V		
		5.5V	0.7V _{CC}	V _{CC} +0.3	2.5	V		
V _{IL}	Input Low Voltage	3.5V	V _{SS} -0.3	0.2V _{CC}	0.7	V		
		5.5V	V _{SS} -0.3	0.2V _{CC}	1.5	V		
V _{OH}	Output High Voltage	3.5V	V _{CC} -0.4		3.1	V	I _{OH} = -2.0 mA	
		5.5V	V _{CC} -0.4		4.8	V	I _{OH} = -2.0 mA	
V _{OL1}	Output Low Voltage	3.5V		0.6	0.2	V	I _{OL} = +4.0 mA	
		5.5V		0.4	0.1	V	I _{OL} = +4.0 mA	
V _{OL2}	Output Low Voltage	3.5V		1.2	0.5	V	I _{OL} = +6 mA	
		5.5V		1.2	0.5	V	I _{OL} = +12 mA	
V _{RH}	Reset Input High Voltage	3.5V	0.5V _{CC}	V _{CC}	1.1	V		
		5.5V	0.5V _{CC}	V _{CC}	2.2	V		
V _{RL}	Reset Input Low Voltage	3.5V	V _{SS} -0.3	0.2V _{CC}	0.9	V		
		5.5V	V _{SS} -0.3	0.2V _{CC}	1.4	V		
V _{OFFSET}	Comparator Input Offset Voltage	3.5V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
I _{IL}	Input Leakage	3.5V	-1.0	2.0	0.064	mA	V _{IN} = 0V, V _{CC}	
		5.5V	-1.0	2.0	0.064	mA	V _{IN} = 0V, V _{CC}	
I _{OL}	Output Leakage	3.5V	-1.0	2.0	0.114	μA	V _{IN} = 0V, V _{CC}	
		5.5V	-1.0	2.0	0.114	μA	V _{IN} = 0V, V _{CC}	
V _{ICR}	Comparator Input Common Mode Voltage Range	3.5V	V _{SS} -0.3	V _{CC} -1.0		V		3
		5.5V	V _{SS} -0.3	V _{CC} -1.0		V		3
I _{IR}	Reset Input Current	3.5V	-10	-60	-30	μA		
		5.5V	-20	-180	-100	μA		

DC ELECTRICAL CHARACTERISTICS (Continued)

Table 2. DC Electrical Characteristics

T_A = –40°C to +105°C								
Extended Temperatures								
Sym	Parameter	V_{CC}¹	Min	Max	Typical² @ 25°C	Units	Conditions	Notes
V _{CH}	Clock Input High Voltage	4.5V	0.7 V _{CC}	V _{CC} +0.3	2.5	V	Driven by External Clock Generator	
		5.5V	0.7 V _{CC}	V _{CC} +0.3	2.5	V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	4.5V	V _{SS} –0.3	0.2 V _{CC}	1.5	V	Driven by External Clock Generator	
		5.5V	V _{SS} –0.3	0.2 V _{CC}	1.5	V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	4.5V	0.7 V _{CC}	V _{CC} +0.3	2.5	V		
		5.5V	0.7 V _{CC}	V _{CC} +0.3	2.5	V		
V _{IL}	Input Low Voltage	4.5V	V _{SS} –0.3	0.2 V _{CC}	1.5	V		
		5.5V	V _{SS} –0.3	0.2 V _{CC}	1.5	V		
V _{OH}	Output High Voltage	4.5V	V _{CC} –0.4		4.8	V	I _{OH} = –2.0 mA	
		5.5V	V _{CC} –0.4		4.8	V	I _{OH} = –2.0 mA	
V _{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I _{OL} = +4.0 mA	
		5.5V		0.4	0.1	V	I _{OL} = +4.0 mA	
V _{OL2}	Output Low Voltage	4.5V		1.2	0.5	V	I _{OL} = +12 mA	
		5.5V		1.2	0.5	V	I _{OL} = +12 mA	
V _{RH}	Reset Input High Voltage	4.5V	0.5V _{CC}	V _{CC}	1.1	V		
		5.5V	0.5V _{CC}	V _{CC}	2.2	V		
V _{OFFSET}	Comparator Input Offset Voltage	4.5V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
I _{IL}	Input Leakage	4.5V	–1.0	2.0	<1.0	μA	V _{IN} = 0V, V _{CC}	
		5.5V	–1.0	2.0	<1.0	μA	V _{IN} = 0V, V _{CC}	
I _{OL}	Output Leakage	4.5V	–1.0	2.0	<1.0	μA	V _{IN} = 0V, V _{CC}	
		5.5V	–1.0	2.0	<1.0	μA	V _{IN} = 0V, V _{CC}	
V _{ICR}	Comparator Input Common Mode Voltage Range	4.5V	0	V _{CC} –1.5V		V		3
		5.5V	0	V _{CC} –1.5V		V		3
I _{IR}	Reset Input Current	4.5V	–18	–180	–112	mA		
		5.5V	–18	–180	–112	mA		

Table 2. DC Electrical Characteristics (Continued)

$T_A = -40^{\circ}\text{C to } +105^{\circ}\text{C}$ Extended Temperatures								
Sym	Parameter	V_{CC}^1	Min	Max	Typical ² @ 25°C	Units	Conditions	Notes
I_{CC}	Supply Current	4.5V		7.0	4.0	mA	@ 10 MHz	4,5
		5.5V		7.0	4.0	mA	@ 10 MHz	4,5
I_{CC1}	Standby Current	4.5V		2.0	1.0	mA	HALT Mode $V_{IN} = 0V$, V_{CC} @ 10 MHz	4,5
		5.5V		2.0	1.0	mA	HALT Mode $V_{IN} = 0V$, V_{CC} @ 10 MHz	4,5
I_{CC2}	Standby Current	4.5V		700	250	nA	STOP Mode $V_{IN} = 0V$, V_{CC}	6
		5.5V		700	250	nA	STOP Mode $V_{IN} = 0V$, V_{CC}	6

Notes:

1. The V_{CC} voltage specification of 4.5V and 5.5V guarantees 5.0V $\pm 0.5V$.
2. Typical values are measured at $V_{CC} = 3.3V$ and $V_{CC} = 5.0V$; $V_{SS} = 0V = GND$.
3. For analog comparator input when analog comparator is enabled.
4. All outputs unloaded and all inputs are at V_{CC} or V_{SS} level.
5. CL1 = CL2 = 22 pF.
6. Same as note 4 except inputs at V_{CC} .

RESET PIN OPERATION (Continued)

Table 4. Control and Peripheral Registers (Continued)

Register (HEX)	Register Name	Bits								Comments
		7	6	5	4	3	2	1	0	
D7	Port B Special Function	0	0	0	0	0	0	0	0	Deactivates all port special functions after RESET
D6	Port B Directional Control	0	0	0	0	0	0	0	0	Defines all bits as inputs in PortB after RESET
D5	Port B Output	U	U	U	U	U	U	U	U	Output register not affected by RESET
D4	Port B Input	U	U	U	U	U	U	U	U	Current sample of the input pin following RESET
D3	Port A Special Function	0	0	0	0	0	0	0	0	Deactivates all port special functions after RESET
D2	Port A Directional Control	0	0	0	0	0	0	0	0	Defines all bits as inputs in PortA after RESET
D1	Port A Output	U	U	U	U	U	U	U	U	Output register not affected by RESET
D0	Port A Input	U	U	U	U	U	U	U	U	Current sample of the input pin following RESET
CF	Reserved									
CE	Reserved									
CD	T1VAL	U	U	U	U	U	U	U	U	
CC	T0VAL	U	U	U	U	U	U	U	U	
CB	T3VAL	U	U	U	U	U	U	U	U	
CA	T2VAL	U	U	U	U	U	U	U	U	
C9	T3AR	U	U	U	U	U	U	U	U	
C8	T2AR	U	U	U	U	U	U	U	U	
C7	T1ARHI	U	U	U	U	U	U	U	U	
C6	T0ARHI	U	U	U	U	U	U	U	U	
C5	T1ARLO	U	U	U	U	U	U	U	U	
C4	T0ARLO	U	U	U	U	U	U	U	U	
C3	WDTHI	1	1	1	1	1	1	1	1	
C2	WDTLO	1	1	1	1	1	1	1	1	
C1	TCTLHI	1	1	1	1	1	0	0	0	WDT Enabled in HALT Mode, WDT timeout at maximum value, STOP Mode disabled
C0	TCTLLO	0	0	0	0	0	0	0	0	All standard timers are disabled

Note: *The SMR and WDT flags are set indicating the source of the RESET.

Table 5. Flag Register Bit D1, D0

D1	D0	Reset Source
0	0	RESET Pin
0	1	SMR Recovery
1	0	WDT Reset
1	1	Reserved

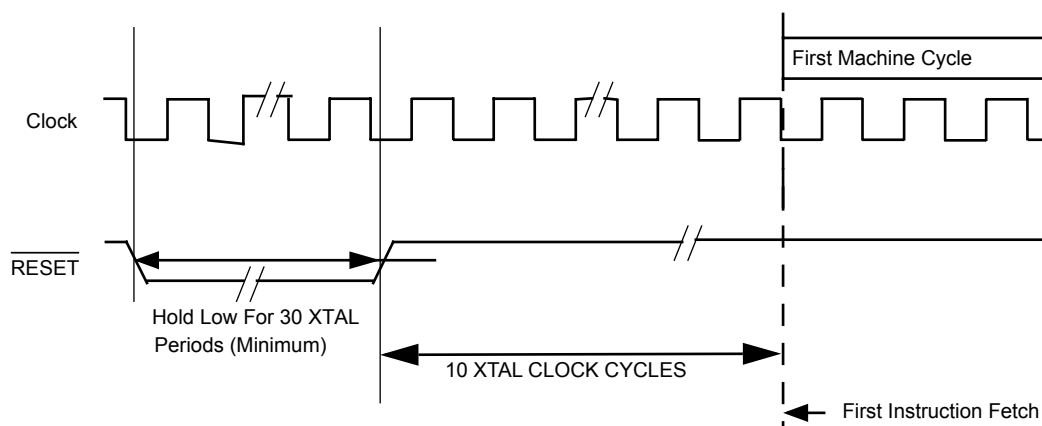


Figure 9. Reset Timing

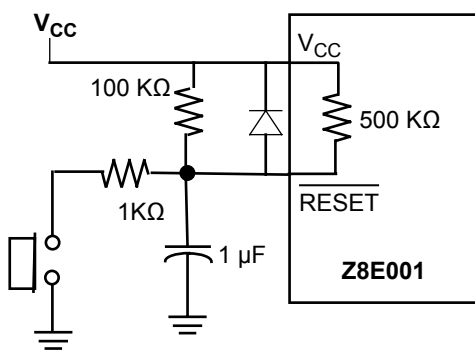


Figure 10. Example of External Power-On Reset (POR) Circuit

Z8E001 WATCH-DOG TIMER (WDT)

The WDT is a retriggerable one-shot 16-bit timer that resets the Z8E001 if it reaches its terminal count. The WDT is driven by the XTAL2 clock pin. To provide the longer timeout periods required in applications, the watchdog timer is only updated every 64th clock cycle. When operating in the RUN or HALT Modes, a WDT timeout reset is functionally equivalent to an interrupt vectoring the PC to 0020H and setting the WDT flag to a one state. Coming out of RESET, the WDT is fully enabled with its timeout value set at the maximum value, unless otherwise programmed during the first instruction. Subsequent executions of the WDT instruction, reinitialize the watchdog timer registers (C2H and C3H), to their initial values as defined by bits D6, D5, and D4 of the TCTLHI register. The WDT cannot be disabled except on the first cycle after RESET, and if the device enters Stop mode.

The WDT instruction should be executed often enough to provide some margin before allowing the WDT registers to

get near 0. Because the WDT timeout periods are relatively long, a WDT reset will occur in the unlikely event that the WDT times out on exactly the same cycle that the WDT instruction is executed.

The WDT and SMR flags are the only flags that are affected by the external RESET pin. RESET clears both the WDT and SMR flags. A WDT timeout sets the WDT flag. The STOP instruction sets the SMR flag. This behavior enables software to determine whether a pin RESET occurred, or whether a WDT timeout occurred, or whether a return from STOP Mode occurred. Reading the WDT and SMR flags does not reset it to zero, the user must clear it via software.

Note: Failure to clear the SMR flag can result in undefined behavior.

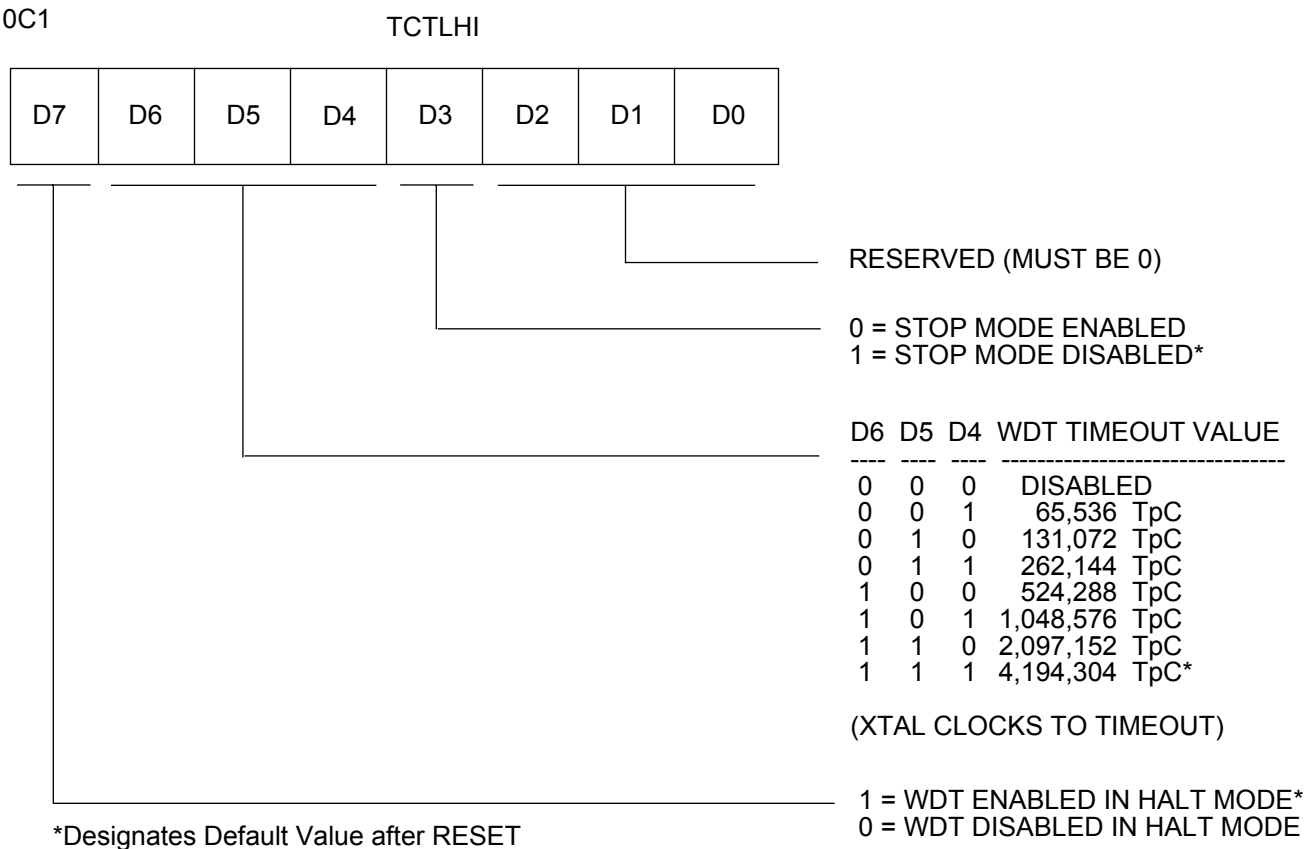


Figure 12. Z8E001 TCTLHI Register for Control of WDT

Note: The WDT can only be disabled via software if the first instruction out of RESET performs this function. Logic within the Z8E001 detects that it is in the process of executing the first instruction after the part leaves RESET. During the execution of this instruction, the upper five bits of the TCTLHI register can be written. After this first instruction, hardware does not allow the upper five bits of this register to be written.

The TCTLHI bits for control of the WDT are described below:

WDT Time Select (D6, D5, D4). Bits 6, 5, and 4 determine the time-out period. Table 6 indicates the range of timeout values that can be obtained. The default values of D6, D5, and D4 are all 1, thus setting the WDT to its maximum time-out period when coming out of RESET.

WDT During HALT (D7). This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. A 0 prevents the WDT from resetting the part while halted. Coming out of reset, the WDT is enabled during HALT Mode.

STOP MODE (D3). Coming out of RESET, the Z8E001 STOP Mode is disabled. If an application requires use of STOP Mode, bit D3 must be cleared immediately upon leaving RESET. If bit D3 is set, the STOP instruction executes as a NOP. If bit D3 is cleared, the STOP instruction enters Stop Mode. Whenever the Z8E001 wakes up after having been in STOP Mode, the STOP Mode is again disabled.

Bits 2, 1 and 0. These bits are reserved and must be 0.

Table 6. WDT Time-Out

D6	D5	D4	Crystal Clocks* to Timeout	Time-Out Using a 10 MHZ Crystal
0	0	0	Disabled	Disabled
0	0	1	65,536 TpC	6.55 ms
0	1	0	131,072 TpC	13.11 ms
0	1	1	262,144 TpC	26.21 ms
1	0	0	524,288 TpC	52.43 ms
1	0	1	1,048,576 TpC	104.86 ms
1	1	0	2,097,152 TpC	209.72 ms
1	1	1	4,194,304 TpC	419.43 ms

Note:
*TpC=XTAL clock cycle. The default on reset is D6=D5=D4=1.

POWER-DOWN MODES

In addition to the standard RUN mode, the Z8E001 MCU supports two Power-Down modes to minimize device current consumption. The two modes supported are HALT and STOP.

HALT MODE OPERATION

The HALT Mode suspends instruction execution and turns off the internal CPU clock. The on-chip oscillator circuit remains active so the internal clock continues to run and is applied to the timers and interrupt logic.

To enter the HALT Mode, the Z8E001 only requires a HALT instruction. It is NOT necessary to execute a NOP instruction immediately before the HALT instruction.

```
7F    HALT    ; enter HALT Mode
```

The HALT Mode can be exited by servicing an interrupt (either externally or internally) generated. Upon completion of the interrupt service routine, the user program continues from the instruction after the HALT instruction.

The HALT Mode can also be exited via a RESET activation or a Watch-Dog Timer (WDT) timeout. In these cases, program execution restarts at the reset restart address 0020H.

STOP MODE OPERATION

The STOP Mode provides the lowest possible device standby current. This instruction turns off the on-chip oscillator and internal system clock.

To enter the STOP Mode, the Z8E001 only requires a STOP instruction. It is NOT necessary to execute a NOP instruction immediately before the STOP instruction.

```
6F  STOP    ;enter STOP Mode
```

The STOP Mode is exited by any one of the following resets: RESET pin or a STOP-Mode Recovery source. Upon reset generation, the processor always restarts the application program at address 0020H, and the STOP Mode Flag is set. Reading the STOP Mode Flag does not clear it. The user must clear the STOP Mode Flag with software.

Note: Failure to clear the STOP Mode Flag can result in undefined behavior.

The Z8E001 provides a dedicated STOP-Mode Recovery (SMR) circuit. In this case, a low-level applied to input pin PB0 triggers an SMR. To use this mode, pin PB0 (I/O Port B, bit 0) must be configured as an input before the STOP Mode is entered. The Low level on PB0 must be held for a minimum pulse width T_{WSM} plus any oscillator startup time. Program execution starts at address 20Hex after PB0 is raised back to a high level.

Notes: Use of the PB0 input for the stop mode recovery does not initialize the control registers.

The STOP Mode current (I_{CC2}) is minimized when:

- V_{CC} is at the low end of the devices operating range.
- Output current sourcing is minimized.
- All inputs (digital and analog) are at the Low or High rail voltages.

CLOCK

The Z8E001 MCU derives its timing from on-board clock circuitry connected to pins XTAL1 and XTAL2. The clock circuitry consists of an oscillator, a glitch filter, a divide-by-two shaping circuit, a divide-by-four shaping circuit, and a divide-by-eight shaping circuit. Figure 13 illustrates the clock circuitry. The oscillator's input is XTAL1 and its output is XTAL2. The clock can be driven by a crystal, a ceramic resonator, LC clock, or an external clock source.

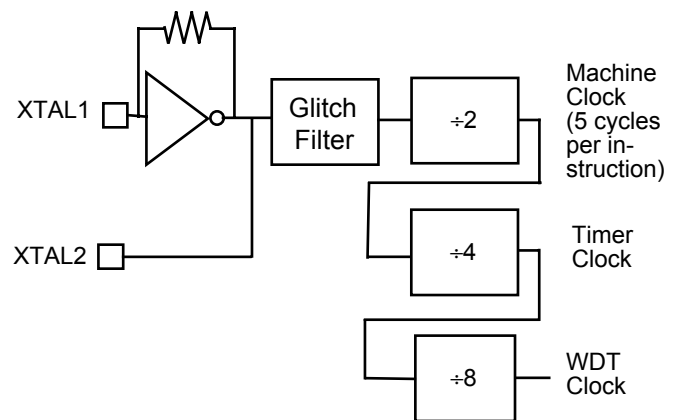


Figure 13. Z8E001 Clock Circuit

OSCILLATOR OPERATION

The Z8E001 MCU uses a Pierce oscillator with an internal feedback resistor (Figure 14). The advantages of this circuit are low-cost, large output signal, low-power level in the crystal, stability with respect to V_{CC} and temperature, and low impedances (not disturbed by stray effects).

One draw back is the requirement for high gain in the amplifier to compensate for feedback path losses. The oscillator amplifies its own noise at start-up until it settles at the frequency that satisfies the gain/phase requirements ($A \times B = 1$; where $A = V_o/V_i$ is the gain of the amplifier and $B = V_i/V_o$ is the gain of the feedback element). The total phase shift around the loop is forced to zero (360 degrees). V_{IN} must be in phase with itself; therefore, the amplifier/inverter provides a 180-degree phase shift, and the feedback element is forced to provide the other 180-degree phase shift.

R_1 is a resistive component placed from output to input of the amplifier. The purpose of this feedback is to bias the amplifier in its linear region and provide the start-up transition.

Capacitor C_2 , combined with the amplifier output resistance, provides a small phase shift. It also provides some attenuation of overtones.

Capacitor C_1 , combined with the crystal resistance, provides an additional phase shift.

C_1 and C_2 can affect the start-up time if they increase dramatically in size. As C_1 and C_2 increase, the start-up time increases until the oscillator reaches a point where it does not start up any more.

It is recommended for fast and reliable oscillator start-up (over the manufacturing process range) that the load capacitors be sized as low as possible without resulting in over-tone operation.

Layout

Traces connecting crystal, caps, and the Z8E001 oscillator pins should be as short and wide as possible, to reduce parasitic inductance and resistance. The components (caps, crystal, resistors) should be placed as close as possible to the oscillator pins of the Z8E001.

The traces from the oscillator pins of the IC and the ground side of the lead caps should be guarded from all other traces (clock, V_{CC} , address/data lines, system ground) to reduce cross talk and noise injection. Guarding is usually accomplished by keeping other traces and system ground trace planes away from the oscillator circuit, and by placing a Z8E001 device V_{SS} ground ring around the traces/components. The ground side of the oscillator lead caps should be connected to a single trace to the Z8E001 V_{SS} (GND) pin. It should not be shared with any other system ground trace

or components except at the Z8E001 device V_{SS} pin. The objective is to prevent differential system ground noise injection into the oscillator (Figure 15).

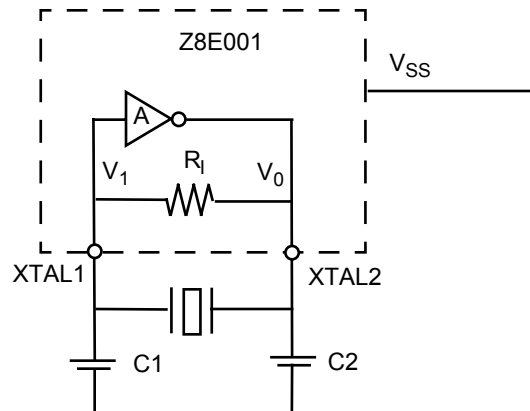


Figure 14. Pierce Oscillator with Internal Feedback Circuit

Indications of an Unreliable Design

There are two major indicators that are used in working designs to determine their reliability over full lot and temperature variations. They are:

Start-up Time. If start-up time is excessive, or varies widely from unit to unit, there is probably a gain problem. To fix the problem, the capacitors C_1/C_2 require reduction. The amplifier gain is either not adequate at frequency, or the crystal R_s are too large.

Output Level. The signal at the amplifier output should swing from ground to V_{CC} to indicate adequate gain in the amplifier. As the oscillator starts up, the signal amplitude grows until clipping occurs. At that point, the loop gain is effectively reduced to unity, and constant oscillation is achieved. A signal of less than 2.5 volts peak-to-peak is an indication that low gain can be a problem. Either C_1 or C_2 should be made smaller, or a low-resistance crystal should be used.

Circuit Board Design Rules

The following circuit board design rules are suggested:

- To prevent induced noise, the crystal and load capacitors should be physically located as close to the Z8E001 as possible.
- Signal lines should not run parallel to the clock oscillator inputs. In particular, the crystal input circuitry and the internal system clock output should be separated as much as possible.

LC OSCILLATOR

The Z8E001 oscillator can use a LC network to generate a XTAL clock (Figure 17).

The frequency stays stable over V_{CC} and temperature. The oscillation frequency is determined by the equation:

$$\text{Frequency} = \frac{1}{2\pi (LC_T)^{1/2}}$$

where L is the total inductance including parasitics, and C_T is the total series capacitance including parasitics.

Simple series capacitance is calculated using the equation at the top of the next column.

$$1/C_T = 1/C_1 + 1/C_2$$

$$\text{If } C_1 = C_2$$

$$1/C_T = 2/C_1$$

$$C_1 = 2C_T$$

A sample calculation of capacitance C_1 and C_2 for 5.83 MHz frequency and inductance value of 27 μ H is displayed as follows:

$$5.83 (10^6) = \frac{1}{2\pi [2.7 (10^{-6}) C_T]^{1/2}}$$

$$C_T = 27.6 \text{ pF}$$

Thus $C_1 = 55.2 \text{ pF}$ and $C_2 = 55.2 \text{ pF}$.

TIMERS

For the Z8E001, 8-bit timers (T0 and T1) are available to function as a pair of independent 8-bit standard timers, or they can be cascaded to function as a 16-bit PWM timer.

In addition to T0 and T1, extra 8-bit timers (T2 and T3) are provided, but they can only operate in cascade to function as a 16-bit standard timer.

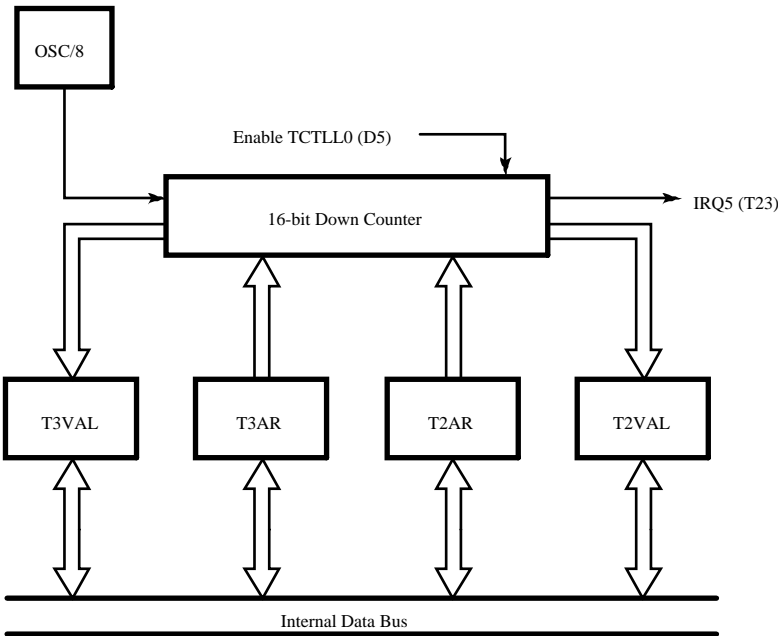


Figure 19. Z8E001 16-Bit Standard Timer

TIMERS (Continued)

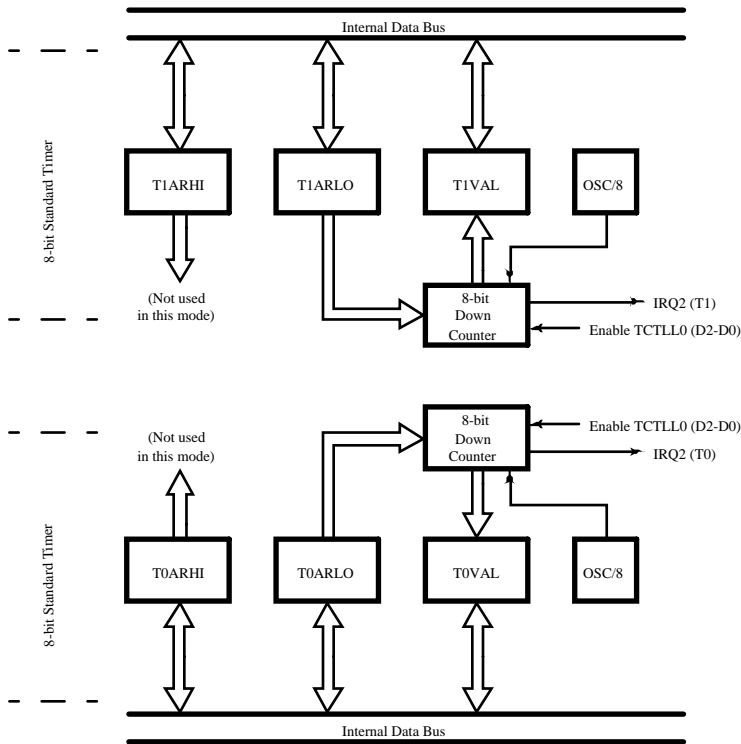


Figure 20. 8-Bit Standard Timers

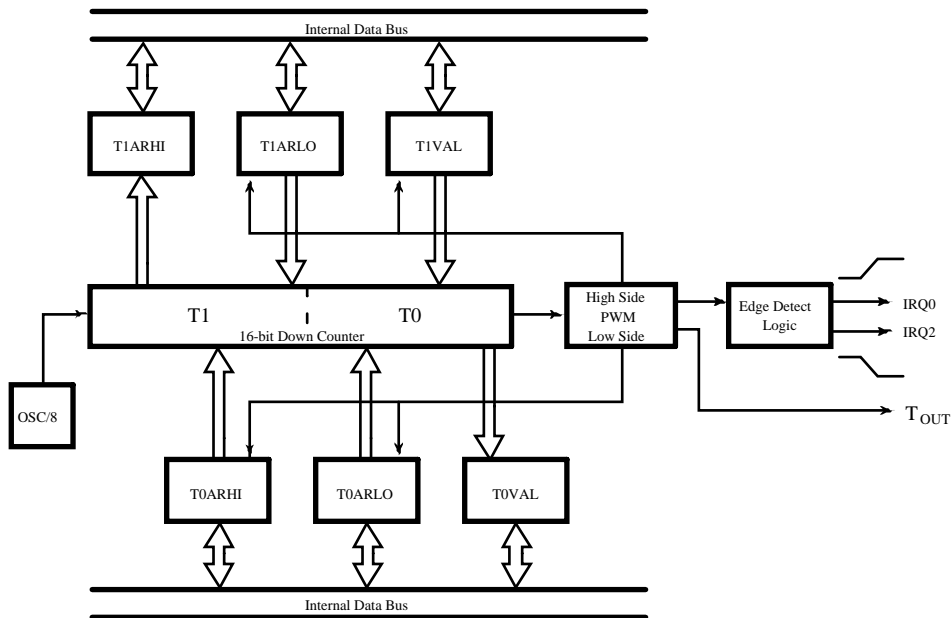


Figure 21. 16-bit Standard PWM Timer

TIMERS (Continued)

at any time, and will have no effect on the functionality of the timer.

If a timer pair is defined to operate as a single 16-bit entity, the entire 16-bit value must reach 0 before an interrupt is generated. In this case, a single interrupt is generated, and the interrupt corresponds to the even 8-bit timer.

Example: Timers T2 and T3 are cascaded to form a single 16-bit timer, so the interrupt for the combined timer is defined to be that of timer T2 rather than T3. When a timer pair is specified to act as a single 16-bit timer, the even timer registers in the pair (timer T0 or T2) is defined to hold the timer's least significant byte. In contrast, the odd timer in the pair holds the timer's most significant byte.

In parallel with the posting of the interrupt request, the interrupting timer's count value is initialized by copying the contents of the auto-initialization value register to the count value register. It should be noted that any time that a timer pair is defined to act as a single 16-bit timer, that the auto-reload function is performed automatically. All 16-bit timers continue counting while their interrupt requests are active, and each operates in a free-running manner.

If interrupts are disabled for a long period of time, it is possible for the timer to decrement to 0 again before its initial interrupt has been responded to. This condition is termed a degenerate case, and hardware is not required to detect it.

When the timer control register is written, all timers that are enabled by the write begins counting using the value that is held in the count register. In this case, an auto-initialization is not performed. All timers can receive an internal clock source only. Each timer that is enabled is updated every 8th XTAL clock cycle.

If T0 and T1 are defined to work independently, then each works as an 8-bit timer with a single auto-initialization register (T0ARLO for T0, and T1ARLO for T1). Each timer asserts its predefined interrupt when it times out, optionally performing the auto-initialization function. If T0 and T1 are cascaded to form a single 16-bit timer, then the single 16-bit timer is capable of performing as a Pulse-Width Modulator (PWM). This timer is referred to as T01 to distinguish it as having special functionality that is not available when T0 and T1 act independently.

When T01 is enabled, it can use a pair of 16-bit auto-initialization registers. In this mode, one 16-bit auto-initialization value is composed of the concatenation of T1ARLO and T0ARLO. The second auto-initialization value is composed of the concatenation of T1ARHI and T0ARHI. When

T01 times out, it alternately initializes its count value using the LO auto-init pair, followed by the HI auto-init pair. This functionality corresponds to a PWM, where the T1 interrupt defines the end of the HI section of the waveform, and the T0 interrupt marks the end of the LO portion of the PWM waveform.

To use the cascaded timers as a PWM, one must initialize the T0 and T1 count registers to work in conjunction with the port pin. The user should initialize the T0 and T1 count registers to the PWM_HI auto-init value to obtain the required PWM behavior. The PWM is arbitrarily defined to use the LO autoreload registers first, implying that it had just timed out after beginning in the HI portion of the PWM waveform. As such, the PWM is defined to assert the T1 interrupt after the first timeout interval.

After the auto-initialization has been completed, decrementing occurs for the number of counts defined by the PWM_LO registers. When decrementing again reaches 0, the T0 interrupt is asserted; and auto-init using the PWM_HI registers occurs. Decrementing occurs for the number of counts defined by the PWM_HI registers until reaching 0. From there, the T1 interrupt is asserted, and the cycle begins again.

The internal timers can be used to trigger external events by toggling the PB1 output when generating an interrupt. This functionality can only be achieved in conjunction with the port unit defining the appropriate pin as an output signal with the timer output special function enabled. In this mode, the appropriate port output is toggled when the timer count reaches 0, and continues toggling each time that the timer times out.

T_{OUT} Mode

The PortB special function register PTBSFR (0D7H) (Figure 23) is used in conjunction with the Port B directional control register PTBDIR (0D6) (Figure 24) to configure PB1 for T_{OUT} operation for timer0. In order for T_{OUT} to function, PB1 must be defined as an output line by setting PTBDIR bit 1 to 1. Configured in this way, PB1 has the capability of being a clock output for timer0, toggling the PB1 output pin on each timer0 timeout.

At end-of-count, the interrupt request line IRQ0, clocks a toggle flip-flop. The output of this flip-flop drives the T_{OUT} line, PB1. In all cases, when timer0 reaches its end-of-count, T_{OUT} toggles to its opposite state (Figure 25). If, for example, timer0 is in Continuous Counting Mode, T_{OUT} has a 50 percent duty cycle output. This duty cycle can easily be controlled by varying the initial values after each end-of-count.

RESET CONDITIONS

After a hardware RESET, the timers are disabled. See Table 4 for timer control, value, and auto-initialization register status after RESET.

I/O PORTS

The Z8E001 has 13 lines dedicated to input and output. These lines are grouped into two ports known as Port A and Port B. Port A is an 8-bit port, bit programmable as either inputs or outputs. Port B can be programmed to provide standard input/output or the following special functions: timer0 output, comparator input, SMR input, and external interrupt inputs.

All ports have push-pull CMOS outputs. In addition, the outputs of Port A on a bit-wise basis can be configured for open-drain operation. The ports operate on a bit-wise basis. As such, the register values for/at a given bit position only affect the bit in question.

Each port is defined by a set of four control registers. See Figure 27.

Directional Control and Special Function Registers

Each port on the Z8E001 has a dedicated Directional Control Register that determines (on a bit-wise basis) whether a given port bit operates as either an input or an output.

Each port on the Z8E001 has a Special Function Register that, in conjunction with the Directional Control Register, implements (on a bit-wise basis), any special functionality that can be defined for each particular port bit.

READ/WRITE OPERATIONS

The control for each port is done on a bit-wise basis. All bits are capable of operating as inputs or outputs, depending upon the setting of the port's Directional Control Register. If configured as an input, each bit is provided a Schmitt-trigger. The output of the Schmitt-trigger is latched twice to perform a synchronization function, and the output of the synchronizer is fed to the port input register, which can be read by software.

A write to a port input register has the effect of updating the contents of the input register, but subsequent reads do not necessarily return the same value that was written. If the bit in question is defined as an input, the input register for

Table 7. Z8E001 I/O Ports Registers

Register	Address	Identifier
Port B Special Function	0D7H	PTBSFR
Port B Directional Control	0D6H	PTBDIR
Port B Output Value	0D5H	PTBOUT
Port B Input Value	0D4H	PTBIN
Port A Special Function	0D3H	PTASFR
Port A Directional Control	0D2H	PTADIR
Port A Output Value	0D1H	PTAOUT
Port A Input Value	0D0H	PTAIN

Input and Output Value Registers

Each port has an Output Value Register and a pF Input Value Register. For port bits configured as an input by means of the Directional Control Register, the Input Value Register for that bit position contains the current synchronized input value.

For port bits configured as an output by means of the Directional Control Register, the value held in the corresponding bit of the Output Value Register is driven directly onto the output pin. The opposite register bit for a given pin (the output register bit for an input pin and the input register bit for an output pin) holds their previous value. These bits are not changed and don't have any effect on the hardware.

that bit position contains the current synchronized input value. Thus, writes to that bit position is overwritten on the next clock cycle with the newly sampled input data. However, if the particular port bit is programmed as an output, the input register for that bit retains the software-updated value. The port bits that are programmed as outputs do not sample the value being driven out.

Any bit in either port can be defined as an output by setting the appropriate bit in the directional control register. If such is the case, the value held in the appropriate bit of the port output register is driven directly onto the output pin.

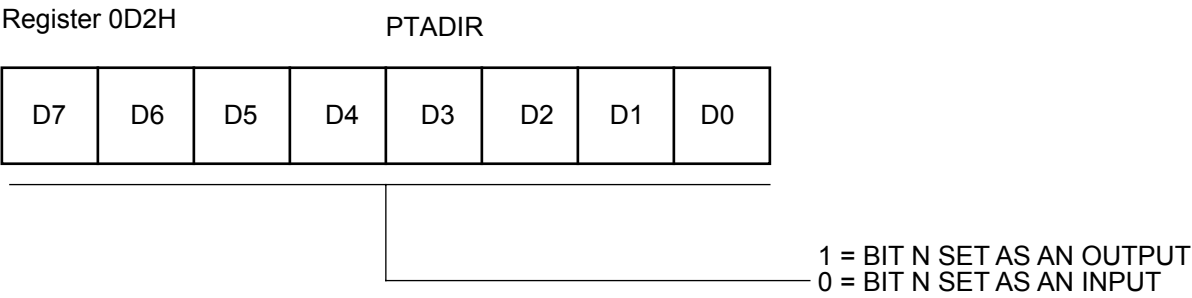


Figure 30. Port A Directional Control Register

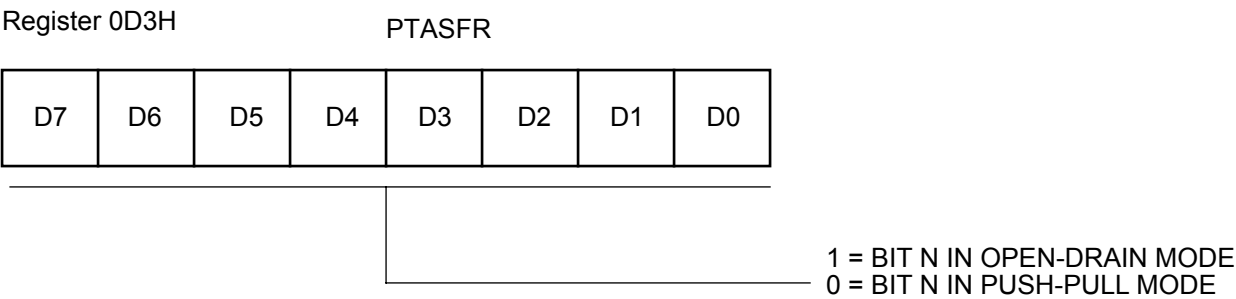


Figure 31. Port A Special Function Register

PORT B—PIN 0 CONFIGURATION

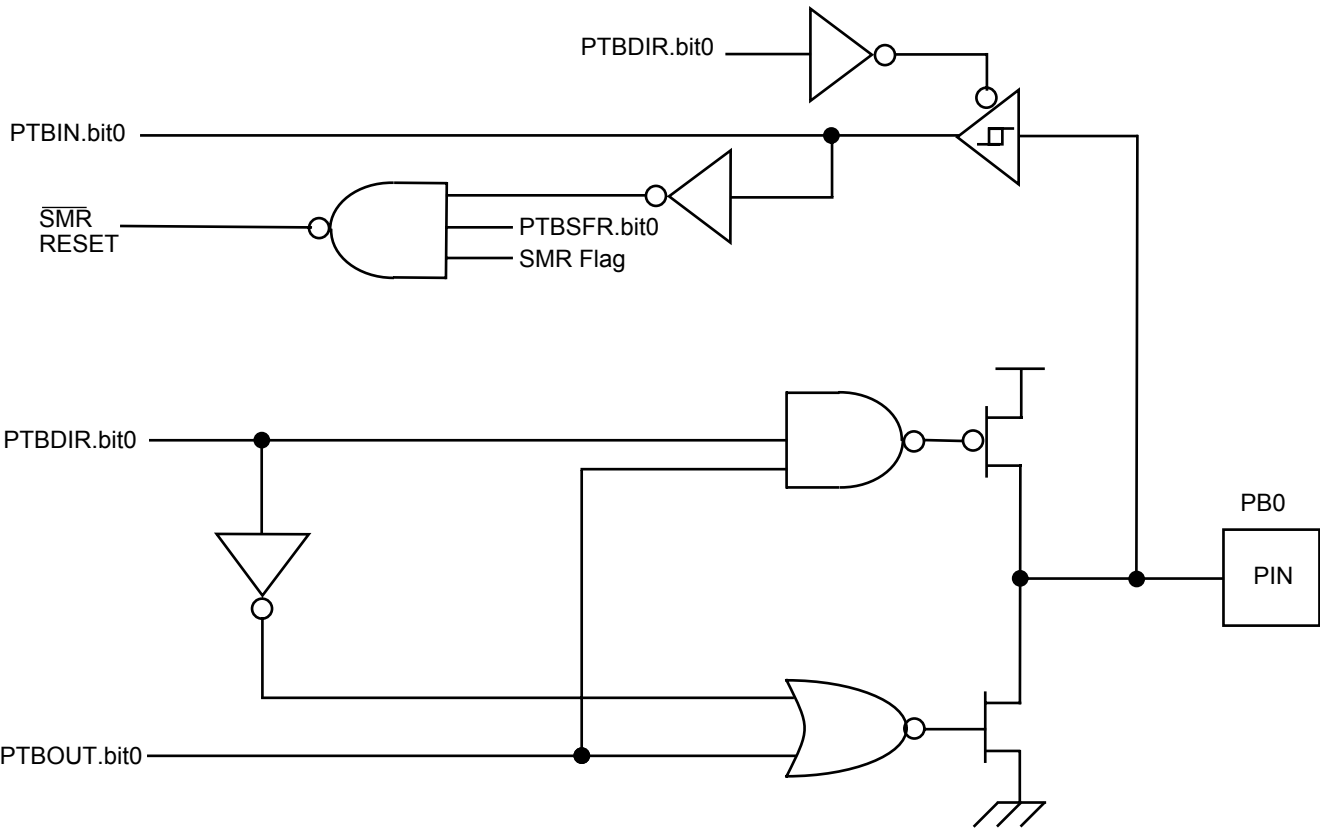


Figure 33. Port B Pin 0 Diagram

I/O PORT RESET CONDITIONS

Full Reset

Port A and Port B output value registers are not affected by RESET.

On RESET, the Port A and Port B directional control registers is cleared to all zeros, which defines all pins in both ports as inputs.

On RESET, the directional control registers redefine all pins as inputs, and the Port A and Port B input value registers

overwrites the previously held data with the current sample of the input pins.

On RESET, the Port A and Port B special function registers is cleared to all zeros, which deactivates all port special functions.

Note: The SMR and WDT timeout events are NOT full device resets. The port control registers are not affected by either of these events.

ANALOG COMPARATOR

The Z8E001 includes one on-chip analog comparator. Pin PB4 has a comparator front end. The comparator reference voltage is on pin PB3.

Comparator Description

The on-chip comparator can process an analog signal on PB4 with reference to the voltage on PB3. The analog function is enabled by programming the Port B Special Function Register bits 3 and 4.

When the analog comparator function is enabled, bit 4 of the input register is defined as holding the synchronized output of the comparator, while bit 3 retains a synchronized sample of the reference input.

If the interrupts for PB4 are enabled when the comparator special function is selected, the output of the comparator generates interrupts.

COMPARATOR OPERATION

The comparator output reflects the relationship between the analog input to the reference input. If the voltage on the analog input is higher than the voltage on the reference input, then the comparator output is at a High state. If the voltage on the analog input is lower than the voltage on the reference input, then the analog output will be at a Low state.

Comparator Definitions

V_{ICR}

The usable voltage range for the positive input and reference input is called the common mode voltage range (V_{ICR}).

Note: The comparator is not guaranteed to work if the input is outside of the V_{ICR} range.

V_{OFFSET}

The absolute value of the voltage between the positive input and the reference input required to make the comparator output voltage switch is the input offset voltage (V_{OFFSET}).

I_{IO}

For the CMOS voltage comparator input, the input offset current (I_{IO}) is the leakage current of the CMOS input gate.

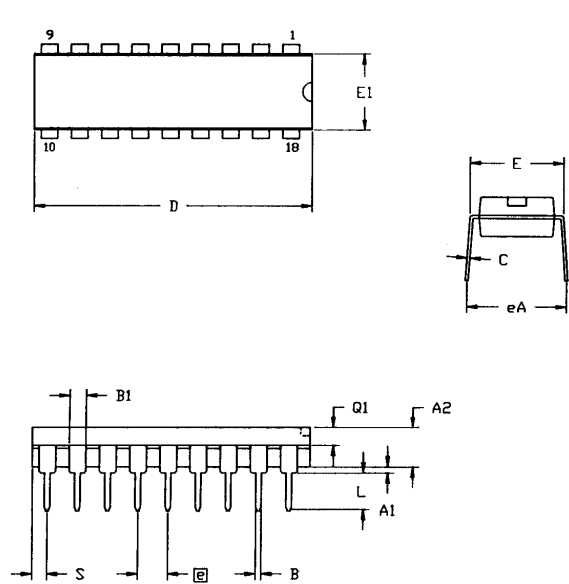
HALT Mode

The analog comparator is functional during HALT Mode. If the interrupts are enabled, an interrupt generated by the comparator will cause a return from HALT Mode.

STOP Mode

The analog comparator is disabled during STOP Mode. The comparator is powered down to prevent it from drawing any current.

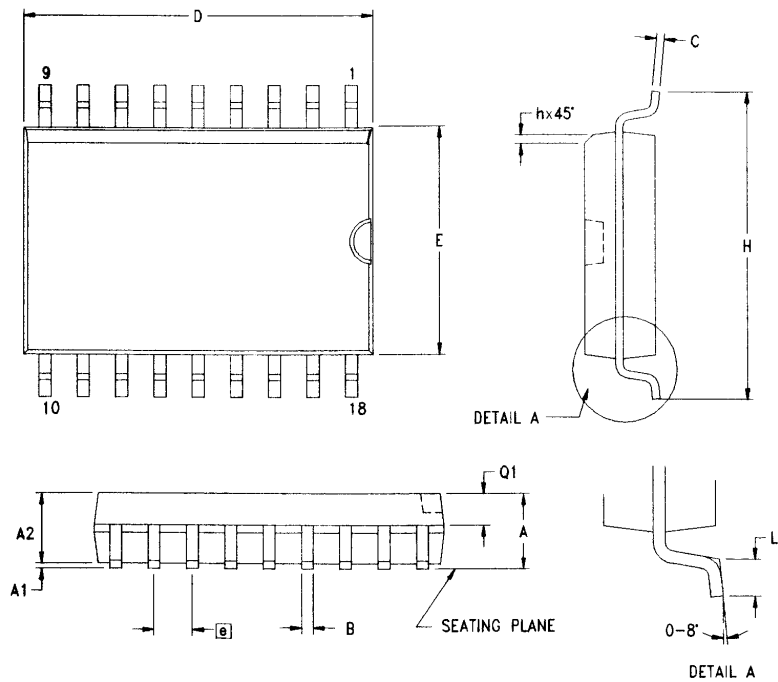
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
⌀	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

Figure 43. 18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
⌀	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 44. 18-Pin SOIC Package Diagram